Enhanced-Boost Z-Source Inverters With Alternate-Cascaded Switched- and Tapped-Inductor Cells

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***Abstract*—In this paper, a number of alternate-cascaded switched-inductor and tapped-inductor networks have been proposed for Z-source inverters. The resulting topologies have enhanced voltage-boost capability while retaining the usual voltage-buck flexibility of a conventional voltage-source inverter. The enhanced capability is achieved by using lower rated components that can more readily be found. These components are assembled without direct series connection and hence avoid unbalanced voltage sharing problems and losses linked to balancing resistive circuits. The component count is, however, high, meaning that the proposed inverters should only be considered when a design requires multiple lower rated components rather than a few higher rated ones. Analysis, simulation, and experimental results have already validated the concepts discussed.**

***Index Terms*—Cascaded inverters, coupled inductors, high frequency magnetic, transformers, Z-source inverters.**

I. Introduction

Z-SOURCE INVERTERS are first proposed in [1] with its voltage-type version shown in Fig. 1(a) (inductive blocks replaced by single-winding inductors). Unlike the traditional voltage-source inverter (VSI) which uses only one dc-link capacitor, Z-source inverters use an input diode and an X-shaped network of capacitors and inductors. Such modifications allow the Z-source inverters to have both voltage-buck and voltage-boost capabilities, which traditional VSI cannot achieve. Because of this flexibility, Z-source inverters have already been investigated for a number of applications like in electric vehicles [2], motor drives [3], photovoltaic generation [4], [5], distributed generation [6], uninterruptible power supplies [7], fuel cell converters [8], and electronic loads [9]. Their modeling [10], operating modes [11], modulation [12], control [13], and parameter sizing [14] have also been widely investigated.

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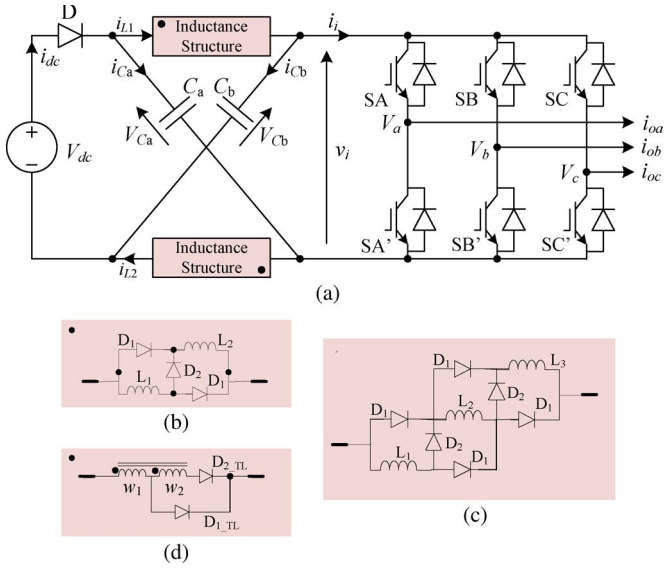

Fig. 1. Voltage-type Z-source inverter (a) overall circuit, (b) SL cell with two inductors, (c) SL cell with three inductors, and (d) TL cell.

Besides those, a few new initiatives have recently been raised for Z-source inverter research, which logically are applicable to other buck–boost inverters too. The first initiative is to raise their gains even further, which might be helpful for tying low-voltage renewable sources to the grid. The second initiative, linked to the first, is to raise the generally low modulation ratio M that a Z-source inverter can produce at high voltage gain. To simultaneously solve both concerns, a number of impedance structures have since been proposed for extending the basic Z-source energy conversion concepts. In [15], a switched-inductor (SL) voltage-type Z-source inverter was proposed, where the inductive blocks shown in Fig. 1(a) were replaced by two SL cells assembled using inductors and diodes. Prior to that, the SL cell has already been applied to various types of dc–dc converters [16] and is thus a well-proven circuit by now. Its dual, the switched-capacitor (SC) cell, has also been applied to the current-type Z-source inverter, as demonstrated in [17].

The trend subsequently drifted toward using two-winding coupled inductors or transformers for even greater voltage boosting. The topologies formed were named as tapped-inductor (TL) [18], T-source [19], and trans-Z-source [20] inverters, whose common feature observed is the use of transformer turns ratio for even higher voltage boosting. Indeed, this

is an attractive feature but unfortunately depends too much on the transformers designed. That means any lack in magnetic coupling of the transformers will definitely cause huge transient overvoltages to occur during switching, which, when unsuppressed, will damage the inverters [18].

Other concerns associated with higher voltage boosting are the flow of high currents and appearance of high voltages across some components. Such stresses, if not lowered, will lead to shorter life span and unexpected damages, which are avoided here by proposing the alternate-cascaded SL and TL Z-source inverters. The proposed inverters use many lower rated components, rather than a few higher rated ones, to tolerate high voltages and currents generated at high gain. The components are assembled based on the alternate-cascading technique presented in [21] after resolving a shortcoming that has not been previously identified. The inverters, thus, created do not rely on direct series connection of their components and are therefore not subject to uneven voltage distribution among the components as their parameters drifted with age, temperature, and operating voltages. Balancing resistors and their accompanied losses are also avoided, which surely are attractive features [22], [23]. The proposed inverters should, however, be considered only when the users can accept higher component counts even though mainly of lower rated components. Operating principles of these inverters are now discussed before proving their performances in simulation and experiment.

II. SL and TL Cells

The original voltage-type Z-source inverter proposed in [1] uses an impedance network with two capacitors and two inductors. Presence of the two inductors allows the VSI bridge to be shorted without causing damages. That means, for example, switches SA and SA' from phase-leg A can be turned on simultaneously to introduce an additional shoot-through state. This is in addition to the usual six active and two null non-shoot-through states that the VSI bridge can assume and is the main contributor to the voltage-boost capability of a voltage-type Z-source inverter. Relevant expressions governing the inverter peak dc-link voltage $\hat{v}_i$, peak ac voltage $\hat{v}_{\rm ac}$, and Z-source capacitor voltage V_C in terms of the input voltage $V_{\rm dc}$ have already been derived in [1]. They are merely listed here in (1) for subsequent comparison with others

$$V_C = \frac{1-d_{\rm ST}}{1-2d_{\rm ST}}V_{\rm dc} \quad \hat{v}_i = \frac{1}{1-2d_{\rm ST}}V_{\rm dc}$$
$$\hat{v}_{\rm ac} = M\frac{\hat{v}}{2} = \frac{1}{1-2d_{\rm ST}}\left(\frac{MV_{\rm dc}}{2}\right) \tag{1}$$

where $d_{\rm ST} < 0.5$ represents the fractional shoot-through time per switching period and $M \leq 1.15$ represents the modulation ratio with triplen offset included.

From (1), the boosting gain can clearly be identified as $1/(1-2d_{\rm ST})$ since the other term enclosed by the parentheses represents the normal ac output voltage of a conventional VSI. Even higher gain than this can conveniently be obtained by using other inductive structures rather than the two inductors found in the original Z-source inverters. Two of the structures are now introduced before extending them further in Section IV using the alternate-cascading technique for resolving some design issues.

A. SL Cell

Fig. 1(b) shows the SL cell with two inductors and three diodes, which has earlier been applied to different types of dc–dc converters for the same reason of enhancing voltage gain [16]. The same SL cell can now replace the upper inductive block shown in Fig. 1(a) for representing the conventional Z-source inverter. Strictly, components of the Z-source network need not be symmetrical even though it is usually assumed to be so. That means replacing the upper inductive block alone will work fine but with asymmetrical voltage and current stresses experienced by its components. To gain an even higher boost and symmetrical distribution of stresses, the lower inductive block in Fig. 1(a) should similarly be replaced by a second vertically flipped SL cell whose D_1-labeled diodes now point left.

Entering a shoot-through state then causes diodes D and D_2 to block, while diodes D_1 conduct to charge the two inductors (L_1 and L_2) per SL cell in parallel. The energy needed for charging them is supplied by the Z-source capacitors. On the other hand, when in a non-shoot-through state, diodes D_1 block, while diodes D and D_2 conduct to discharge L_1 and L_2 in series. Since the dc-link voltage appearing across the external ac loads during a non-shoot-through state is the sum of voltages across the two SL cells and input source, series connection of L_{S1} and L_{S2} will boost it further. Even higher gain can be achieved by using more inductors and diodes per cell. An example layout showing three inductors and six diodes per cell can be found in Fig. 1(c). In general, if $\gamma_{\rm SL}$ inductors are used in each SL cell and with two cells replacing the two inductive blocks shown in Fig. 1(a), capacitor voltage V_C, peak dc-link voltage $\hat{v}_i$, and peak ac output voltage $\hat{v}_{\rm ac}$ of the resulting inverter can be computed as [17]

$$V_C = \frac{1-d_{\rm ST}}{1-(\gamma_{\rm SL}+1)d_{\rm ST}}V_{\rm dc} \quad \hat{v}_i = \frac{1+(\gamma_{\rm SL}-1)d_{\rm ST}}{1-(\gamma_{\rm SL}+1)d_{\rm ST}}V_{\rm dc}$$
$$\hat{v}_{\rm ac} = M\frac{\hat{v}_i}{2} = \frac{1+(\gamma_{\rm SL}-1)d_{\rm ST}}{1-(\gamma_{\rm SL}-1)d_{\rm ST}}\left(\frac{MV_{\rm dc}}{2}\right) \tag{2}$$

where $d_{\rm ST}$ is now limited to $1/(\gamma_{\rm SL}+1)$, determined by setting the denominator of (2) to zero.

Note that, instead of replacing inductive blocks of the conventional Z-source layout shown in Fig. 1(a), the same can be applied to the improved, quasi-, or embedded Z-source inverters discussed in [24]–[28]. As explained in [21], these circuits retain the basic X-shaped structure and are different only with their source placements. Such difference causes their capacitor voltage stresses and source current ripples to be different but will not affect their gains and basic operating principles. The same SL cells can thus be used in place of their inductors. This replacement is straightforward and will hence not be discussed further.

B. TL Cell

Unlike the SL cell which uses independent inductors, the TL cell shown in Fig. 1(d) uses a coupled or TL with two windings and two diodes. The TL cell can again be used in place of the upper inductive block drawn in Fig. 1(a) to give an asymmetrical circuit. If symmetrical circuit is preferred, a second vertically flipped TL cell can replace the lower inductive block in the same figure with diodes D_{1_TL} and D_{2_TL} now pointing left. Under shoot-through condition, diode D_{1_TL} conducts, while D_{2_TL} blocks, leading to the charging of the W_1 winding and the open circuiting of the W_2 winding. On the other hand, when in a non-shoot-through state, diode D_{2_TL}conducts, while D_{1_TL} blocks to discharge the two windings in series. Currents flowing through the two halves of the TL therefore experience step transitions, which will not happen with a normal single-winding inductor whose current is always continuous. Such step transitions are fine so long as magnetic energy stored in the interrupted winding can be transferred to the other winding through perfect coupling.

Returning back to the non-shoot-through state, since the windings are discharged in series, the inverter ac output is again boosted higher than the conventional Z-source inverter. Its corresponding voltage expressions have earlier been derived and are written here as [18]

$$\begin{aligned} V_C &= \frac{1-d_{\mathrm{ST}}}{1-(\gamma_{\mathrm{TL}}+2)d_{\mathrm{ST}}}V_{\mathrm{dc}} \\ \hat{v}_i &= \frac{1+\gamma_{\mathrm{TL}}d_{\mathrm{ST}}}{1-(\gamma_{\mathrm{TL}}+2)d_{\mathrm{ST}}}V_{\mathrm{dc}} \\ \hat{v}_{\mathrm{ac}} &= M\frac{\hat{v}_i}{2} = \frac{1+\gamma_{\mathrm{TL}}d_{\mathrm{ST}}}{1-(\gamma_{\mathrm{TL}}+2)d_{\mathrm{ST}}}\left(\frac{MV_{\mathrm{dc}}}{2}\right) \end{aligned} \tag{3}$$

where $\gamma_{\mathrm{TL}} = W_2/W_1$ is the turns ratio of the TL. Like the SL cells, replacement of the inductors by the TL cells is not limited to Fig. 1(a) only. The same replacement can be applied to the improved, quasi-, and embedded Z-source inverters, whose operating principles remain unchanged. The resulting inverters would, as usual, have lower capacitor voltages and/or smoother source currents.

C. SL Versus TL Cells

The SL cells shown in Fig. 1(b) and (c) obviously require more inductors and diodes if higher voltage gain is demanded. The added inductors will always charge in parallel and discharge in series, hence enduring evenly distributed stresses. Its diodes, on the other hand, will endure different blocking voltages depending on which of the two groups they belong to. For the example shown in Fig. 1(b), diodes labeled as D_1 form one group, while diode D_2 individually forms the second group. Their respective blocking voltages can be determined as (4) and (5), which are found to be independent of the source placement

$$V_{D1} = -\frac{d_{\mathrm{ST}}}{1-(\gamma_{\mathrm{SL}}+1)d_{\mathrm{ST}}}V_{\mathrm{dc}} \quad \text{(Non-shoot-through)} \tag{4}$$

$$V_{D2} = -\frac{1-d_{\mathrm{ST}}}{1-(\gamma_{\mathrm{SL}}+1)d_{\mathrm{ST}}}V_{\mathrm{dc}} \quad \text{(Shoot-through)}. \tag{5}$$

On the contrary, the TL cell uses lesser components even for significantly raised voltage gain. It relies solely on the turns ratio of the TL for its voltage boost, which, like most magnetically coupled devices, will experience high current stress at its low-voltage W_1 winding. This is particularly true for the TL topology, whose shoot-through state causes diode D_{2_TL} in Fig. 1(d) to block and, hence, to force energy from the W_2 to W_1 winding. The latter thus experiences a surge in instantaneous current. In addition to that, diodes of the TL topology are noted to experience higher blocking voltages, whose expressions are written as

$$V_{D1\_\mathrm{TL}} = -\frac{\gamma_{\mathrm{TL}}d_{\mathrm{ST}}}{1-(\gamma_{\mathrm{TL}}+2)d_{\mathrm{ST}}}V_{\mathrm{dc}} \quad \text{(Non-shoot-through)} \tag{6}$$

$$V_{D2\_\mathrm{TL}} = -\frac{\gamma_{\mathrm{TL}}(1-d_{\mathrm{ST}})}{1-(\gamma_{\mathrm{TL}}+2)d_{\mathrm{ST}}}V_{\mathrm{dc}} \quad \text{(Shoot-through)}. \tag{7}$$

These equations are clearly γ_{TL} times larger than those in (4) and (5) after setting $\gamma_{\mathrm{SL}} = \gamma_{\mathrm{TL}} + 1$ to equalize their winding turns and gains. The TL cell therefore endures higher stresses that might eventually limit its gain if appropriately rated components are not available or too costly. Common to both SL and TL cells, however, capacitors C_a and C_b of the inverter that they applied in Fig. 1(a) are experiencing high voltage stresses according to (2) and (3) as γ_{SL} and γ_{TL} increase.

To tolerate the higher stresses, series connection of lower rated capacitors is possibly the most obvious and common approach. The resulting voltage sharing among the capacitors would then depend on their capacitances, whose values can vary prominently with ages, dielectric types, ambient, and storage temperatures. Capacitances are therefore likely to be unbalanced with the smallest value, having the largest impedance ($= 1/(j2\pi fC)$, where f is the frequency), tolerating the highest voltage stress. Such unbalance worsens if a few capacitors leak, causing their voltages to gradually transfer to the healthy ones. Rated voltages of the healthy capacitors might eventually be exceeded, resulting in multiple points of failure. A simple technique for balancing the voltages is to add balancing resistors [22], [23], which unavoidably will introduce additional losses. Better balancing techniques are therefore preferred with a possible technique discussed as follows.

III. Alternate-Cascading Technique and Its Existing Problem

In [21], cascading techniques applied to Z-source inverters for producing higher voltage gains are introduced. Among them, the alternate-cascading technique is more promising since it uses comparably lesser inductors. It is now briefly described before identifying a problem that has not been previously discussed. Resolving this problem is necessary before the alternate-cascading technique can be merged with the SL or TL boosting cell.

A. Operating Principles

Fig. 2 shows two conventional Z-source impedance networks with the second flipped vertically. For easier referencing, they

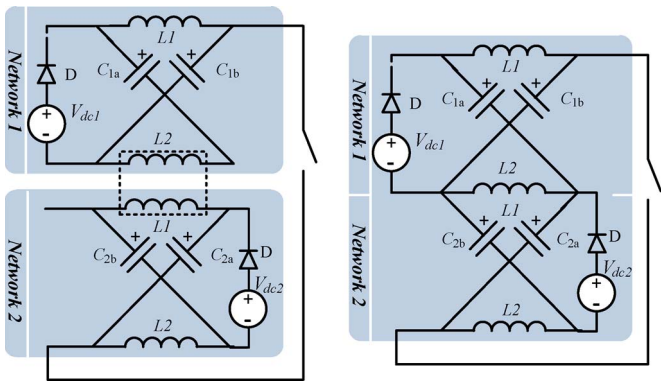

Fig. 2. Alternate-cascading technique illustrated with two networks.

are respectively referred to as networks 1 and 2. As seen, the lower inductor of network 1 and the upper inductor of network 2 can be merged to give the alternate-cascaded network shown on the right of Fig. 2. The cascaded network uses one lesser inductor, and for the general case of N networks in cascade, the governing expressions have earlier been derived as [21]

$$V_C = \frac{1-d_{\rm ST}}{1-(N+1)d_{\rm ST}}\frac{V_{\rm dc}}{N}$$
$$\hat{v}_i = \frac{1}{1-(N+1)d_{\rm ST}}V_{\rm dc}$$
$$\hat{v}_{\rm ac} = M\frac{\hat{v}_i}{2} = \frac{1}{1-(N+1)d_{\rm ST}}\left(\frac{MV_{\rm dc}}{2}\right) \quad (8)$$

where the input-to-output voltage gain is noted to be either the same $(N=1)$ or higher $(N\geq 2)$ than that of the conventional Z-source inverter with the same $d_{\rm ST}$ and M.

Gain of (8) is, however, lower than those in (2) and (3) for the SL and TL topologies if their denominators are equalized by setting $N=\gamma_{\rm SL}=\gamma_{\rm TL}+1$. The amount lower is the same for both topologies and can therefore be determined by considering the SL topology as an example. Dividing (2) by (8) then leads to the first multiplication term in (9). This term can further be simplified by substituting $d_{\rm ST}<1/(\gamma_{\rm SL}+1)$, obtained by setting the common denominator of (2) and (8) to zero. The resulting middle term in (9) is undeniably smaller than two since $(\gamma_{\rm SL}-1)/(\gamma_{\rm SL}+1)$ is always between zero and one for $\gamma_{\rm SL}\geq 1$. Gain of the alternate-cascaded inverter is therefore lower than those of the noncascaded SL and TL inverters. This finding is, however, true only when the denominators of (2) and (8) are equalized to give the same variation range for $d_{\rm ST}$ and hence $M=1.15(1-d_{\rm ST})$ according to [12]. Different conclusions will surface if the basis of comparison changes, which certainly has many options. Covering all options fully in this paper alone is, however, not possible because of the space involved

$$1+(\gamma_{\rm SL}-1)d_{\rm ST} < 1+\frac{\gamma_{\rm SL}-1}{\gamma_{\rm SL}+1} < 2. \quad (9)$$

Besides lower gain, the alternate-cascaded inverter is observed to have more capacitors ($2N$ in total) than the SL and TL topologies. These capacitors, as understood from (8), sustain voltages that are N times smaller with no (or minimal) sharing problems expected, unlike with direct series connection. That means proportionally lower rated capacitors can be used for better stress distribution or simply when higher rated ones are not available. Other components like its input diodes are also not experiencing higher stresses. Alternate cascading is thus an effective technique for distributing stresses at a higher boost level.

Referring to Fig. 2, it should also be noted that two sources are explicitly shown. Their presences would raise the inverter reliability but are strictly not compulsory. That means if one of them is removed and the other is set to $V_{\rm dc}$, the same ac output amplitude would be produced, but with asymmetrical distribution of voltages between the networks.

B. Existing Problem

In [21] where alternate cascading was first introduced, all capacitors were assumed similar (e.g., $C_{1a}=C_{1b}=C_{2a}=C_{2b}$ in Fig. 2). This cannot be the case in theory, as demonstrated here through simple charging/discharging circuit analysis. Although the results in [21] did not show any significant distortion (which might be the reason why it was not investigated), such design consideration, if not clarified, will cause more advanced alternate-cascaded inverters to malfunction.

Taking Fig. 2 as an example, the appropriate capacitance relation can be derived by considering the shoot-through state. During this period, the uppermost inductor is charged by capacitors C_{1a} and C_{2a}, while the lowermost inductor is charged by C_{1b} and C_{2b}. For the middle inductor, its charging energy is drawn from C_{2a} and C_{1b}, which rightfully should discharge two times more energy than C_{1a} and C_{2b}, if the three inductors are similar. That means C_{2a} and C_{1b} must draw two times more energy from the dc sources during their charging process when in the non-shoot-through state.

Since the charging and discharging paths of all capacitors are the same, doubling of energy to and from C_{2a} and C_{1b} over the same time interval can only be achieved by doubling their capacitances. The proper capacitance relation should therefore be $C_{2a}=C_{1b}=2C_{1a}=2C_{2b}$ and not the equal relation read from [21].

IV. Alternate-Cascaded SL and TL Z-Source Inverters

So far, the following statements have been identified.

1) The SL and TL Z-source inverters produce the same higher gain but with some of their components stressed by high voltages and/or currents.
2) The alternate-cascaded Z-source inverter produces a lower gain but has more even distribution of stresses among its components.

It might therefore be of interest to merge different techniques to develop the alternate-cascaded SL and TL Z-source inverters, whose performances lie between boundaries set by the individual techniques. The following explains operating principles of the proposed inverters in detail.

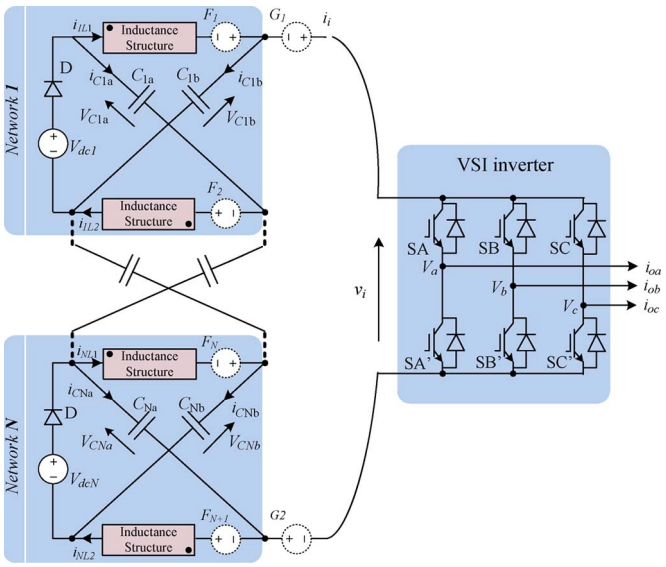

Fig. 3. Alternate-cascaded topology with N networks.

A. Alternate-Cascaded SL Z-Source Inverter

The alternate-cascaded SL inverter is formed by replacing those inductive blocks shown in Fig. 3 with multiple SL cells. The resulting inverter can be analyzed by state-space averaging with equal sources of $V_{\rm dc}/N$ first placed at $V_{\rm dc1}$ to $V_{\rm dcN}$. If each SL cell has $\gamma_{\rm SL}$ inductors and N networks are in cascade, entering a shoot-through state would cause the inductors to charge in parallel with a common voltage given by

$$v_L = NV_C. \tag{10}$$

On the contrary, when it is in a non-shoot-through state, the inductors discharge in series, leading to

$$v_L = \frac{\left(\frac{V_{\rm dc}}{N}\right) - V_C}{\gamma_{\rm SL}}. \tag{11}$$

Averaging v_L to zero then gives rise to the first expression in (12) for calculating the capacitor voltage V_C when the sources are equally placed at $V_{\rm dc1}$ to $V_{\rm dcN}$ only. This expression can further be applied to arrive at those remaining generic expressions in (12) for computing the peak dc-link voltage $\hat{v}_i$ during non-shoot-through state and peak ac output voltage $\hat{v}_{\rm ac}$

$$\begin{aligned} V_C &= \frac{1-d_{\rm ST}}{1-(1+N\gamma_{\rm SL})d_{\rm ST}}\frac{V_{\rm dc}}{N} \\ \hat{v}_i &= \frac{1+(\gamma_{\rm SL}-1)d_{\rm ST}}{1-(1+N\gamma_{\rm SL})d_{\rm ST}}V_{\rm dc} \\ \hat{v}_{\rm ac} &= \frac{1+(\gamma_{\rm SL}-1)d_{\rm ST}}{1-(1+N\gamma_{\rm SL})d_{\rm ST}}\left(\frac{MV_{\rm dc}}{2}\right). \end{aligned} \tag{12}$$

The capacitor voltage V_C and gain in (12) can obviously be tuned by adjusting the variables $\gamma_{\rm SL}$ and N appropriately with the former also found to be independent of capacitance. The resulting capacitor voltage distribution is thus not affected by capacitance drifting, unlike in a direct series-connected circuit. Besides that, (12) informs that, for the extreme cases of $\gamma_{\rm SL}=1$ and $N=1$, it simplifies to (8) and (2) for representing the alternate-cascading and SL techniques separately. These simplifications are expected since the alternate-cascaded SL inverter is realized as a combination of both techniques.

Also shown in Fig. 3 is the presence of alternative sources at positions marked with symbols F_1 to F_{N+1}, G_1, and G_2. Values of these sources and those at $V_{\rm dc1}$ to $V_{\rm dcN}$ are neither fixed nor compulsory, meaning that they can be set to zero if intended. Such source nullification will not alter the expressions for $\hat{v}_i$ and $\hat{v}_{\rm ac}$ so long as the total input voltage is kept at $V_{\rm dc}$. The only influence expected is the presence of different capacitor voltages, as demonstrated by the following two examples:

$$V_C = \frac{1+(\gamma_{\rm SL}-1)d_{\rm ST}}{1-(1+N\gamma_{\rm SL})d_{\rm ST}}\frac{V_{\rm dc}}{N+1}$$
(Sources equally placed at F_1 to F_{N+1}) (13)

$$V_C = \frac{\gamma_{\rm SL}d_{ST}}{1-(1+N\gamma_{\rm SL})d_{\rm ST}}V_{\rm dc}$$
(Sources placed at G_1, G_2 or equally among them). (14)

While placing sources at $V_{\rm dc1}$ to $V_{\rm dcN}$ or F_1 to F_{N+1}, it is also important to note that differences in source values will cause some capacitors to endure higher voltage stresses, while others are less stressed. Capacitors with different ratings are therefore needed, whose values are still lower than that demanded by the single-network inverter shown in Fig. 1. For networks with multiple renewable sources, it is also important for the sources to have their own maximum-power-point trackers including power stages. By itself, the proposed inverter uses only $d_{\rm ST}$ and M as control variables and is thus not able to simultaneously track individual maximum power points for the sources if they are subject to different operating conditions.

A better recommendation is therefore to place the sources at G_1, G_2, or both, if the same capacitor rating is preferred for all networks or if only one consolidated source is available. Placing at these positions will not alleviate the requirement for individual-maximum-power-point trackers if the sources are renewable and subject to different operating conditions. It, however, helps to ensure that all capacitors are stressed equally according to (14), which certainly is lower than that of the single-network SL inverter discussed in Section II-A. For the latter, its V_C expression is also given by (14) except with $N=1$. If N is now raised by alternate cascading, $\gamma_{\rm SL}$ can be reduced proportionally, whose effect is a smaller numerator for (14) and, hence, a smaller V_C stress for the alternate-cascaded SL Z-source inverter.

B. Alternate-Cascaded TL Z-Source Inverter

Instead of the SL cells, the inductive blocks shown in Fig. 3 can be replaced by TL cells to form the alternate-cascaded TL Z-source inverter. The inverter can again be analyzed by performing state-space averaging with equal sources placed at $V_{\rm dc1}$ to $V_{\rm dcN}$ only. When in the shoot-through state, diode $D_{1\_\rm TL}$ in each TL cell in Fig. 1(d) conducts, while diode $D_{2\_\rm TL}$, together with all D-labeled diodes in Fig. 3, blocks. Low-voltage W_1 winding of each TL cell is therefore charged

TABLE I
SUMMARY OF VOLTAGE AND CURRENT EXPRESSIONS FOR PROPOSED INVERTERS ($I_{\rm dc} \equiv$ Average Source Current)

Factors	Alternate-Cascaded SL	Alternate-Cascaded TL
Number of Cascaded Networks	N	N
Total Number of L OR Total Number of Transformers	$\gamma_{SL}(N+1)$	$(N+1)$ each with turns ratio γ_{TL}
Total Number of C	$2N$	$2N$
Total Number of Diodes	$N+3(\gamma_{SL}-1)(N+1)$	$N+2(N+1)$
Input-to-Output Gain $\hat{v}_{ac}/V_{dc}$	$\frac{M\{1+(\gamma_{SL}-1)d_{ST}\}}{2\{1-(1+N\gamma_{SL})d_{ST}\}}$	$\frac{M\{1+\gamma_{TL}d_{ST}\}}{2\{1-[1+N(\gamma_{TL}+1)]d_{ST}\}}$
V_C/V_{dc} (Sources at V_{dc1} to V_{dcN})	$\frac{1-d_{ST}}{N\{1-(1+N\gamma_{SL})d_{ST}\}}$	$\frac{1-d_{ST}}{N\{1-[1+N(\gamma_{TL}+1)]d_{ST}\}}$
V_C/V_{dc} (Sources at F_1 to F_{N+1})	$\frac{1+(\gamma_{SL}-1)d_{ST}}{(N+1)\{1-(1+N\gamma_{SL})d_{ST}\}}$	$\frac{1+\gamma_{TL}d_{ST}}{(N+1)\{1-[1+N(\gamma_{TL}+1)]d_{ST}\}}$
V_C/V_{dc} (Sources at G_1 or G_2)	$\frac{\gamma_{SL}d_{ST}}{1-(1+N\gamma_{SL})d_{ST}}$	$\frac{(\gamma_{TL}+1)d_{ST}}{1-[1+N(\gamma_{TL}+1)]d_{ST}}$
Switch and Diode D Stresses $\hat{v}_i/V_{dc}$	$\frac{1+(\gamma_{SL}-1)d_{ST}}{1-(1+N\gamma_{SL})d_{ST}}$	$\frac{1+\gamma_{TL}d_{ST}}{1-[1+N(\gamma_{TL}+1)]d_{ST}}$
Other Diode Stresses See Notations in Fig. 1(b) to (d)	$\frac{d_{ST}}{1-(1+N\gamma_{SL})d_{ST}}$ for D_1 $\frac{1-d_{ST}}{1-(1+N\gamma_{SL})d_{ST}}$ for D_2	$\frac{\gamma_{TL}d_{ST}}{1-[1+N(\gamma_{TL}+1)]d_{ST}}$ for D_{1_TL} $\frac{\gamma_{TL}(1-d_{ST})}{1-[1+N(\gamma_{TL}+1)]d_{ST}}$ for D_{2_TL}
Per Inductor Current for SL OR Per W_1-side Magnetising Current for TL	$I_L=\frac{I_{dc}}{1+(\gamma_{SL}-1)d_{ST}}$	$I_m=\frac{(\gamma_{TL}+1)I_{dc}}{1+\gamma_{TL}d_{ST}}$
Shoot-Through Current	$\gamma_{SL}(N+1)I_L$	$(N+1)I_m$
Simplification to Non-Cascaded SL OR TL	$N=1$	$N=1$
Simplification to Conventional Z-Network [1]	$N=1$, $\gamma_{SL}=1$	$N=1$, $\gamma_{TL}=0$

by N capacitors in series, while its companion W_2 winding remains opened. The winding voltages can then be written as

$$v_{W1}=NV_C \quad v_{W2}=\gamma_{\rm TL}v_{W1}=\gamma_{\rm TL}NV_C. \tag{15}$$

On the other hand, when in the non-shoot-through state, diode $D_{1\_\rm TL}$ blocks, while diodes $D_{2\_\rm TL}$ and all D-labeled diodes in Fig. 3 conduct to give the following winding voltages:

$$v_{W1}=\frac{\left(\frac{V_{\rm dc}}{N}\right)-V_C}{\gamma_{\rm TL}+1} \quad u_{W2}=\frac{\gamma_{\rm TL}(V_{\rm dc}-V_C)}{\gamma_{\rm TL}+1}. \tag{16}$$

Averaging the winding voltages to zero per switching period then results in the first expression in (17) for computing the capacitor voltage V_C when the sources are at $V_{\rm dc1}$ to $V_{\rm dcN}$ only. This expression can subsequently be used to derive the other two generic expressions in (17) for computing $\hat{v}_i$ and $\hat{v}_{\rm ac}$, respectively

$$\begin{aligned} V_C &= \frac{1-d_{\rm ST}}{1-[1+N(\gamma_{\rm TL}+1)]\,d_{\rm ST}}\frac{V_{\rm dc}}{N} \\ \hat{v}_i &= \frac{1+\gamma_{\rm TL}d_{\rm ST}}{1-[1+N(\gamma_{\rm TL}+1)]\,d_{\rm ST}}V_{\rm dc} \\ \hat{v}_{\rm ac} &= \frac{1+\gamma_{\rm TL}d_{\rm ST}}{1-[1+N(\gamma_{\rm TL}+1)]\,d_{\rm ST}}\left(\frac{MV_{\rm dc}}{2}\right). \end{aligned} \tag{17}$$

The gain of (17) can clearly be tuned by adjusting the TL turns ratio $\gamma_{\rm TL}$ and number of networks N in cascade. Setting $N=1$ will reduce (17) to the TL expressions in (3), while eliminating $\gamma_{\rm TL}(=0)$ will simplify it to the alternate-cascaded expressions in (8). Equating $\gamma_{\rm TL}=\gamma_{\rm SL}-1$ will also lead to those expressions in (12) for representing the alternate-cascaded SL inverter with the same number of winding turns. These cases are mentioned for illustrative purposes only. In general, the control variables should be chosen to produce the demanded gain while not overstressing any of the components available for implementing the inverter.

The same analytical approach can be applied to the circuit even when some of its sources are set to zero or shifted to any of the positions shown in Fig. 3. Expressions for $\hat{v}_i$ and $\hat{v}_{\rm ac}$ would remain unchanged so long as the total source voltage is kept at $V_{\rm dc}$. The only expression expected to change is that for V_C, as illustrated by the following two source-shifting examples:

$$V_C=\frac{1+\gamma_{\rm TL}d_{\rm ST}}{1-[1+N(\gamma_{\rm TL}+1)]\,d_{\rm ST}}\frac{V_{\rm dc}}{N+1}$$

(Sources equally placed at F_1 to F_{N+1}) (18)

$$V_C=\frac{(\gamma_{\rm TL}+1)d_{\rm ST}}{1-[1+N(\gamma_{\rm TL}+1)]\,d_{\rm ST}}V_{\rm dc}$$

(Sources placed at G_1, G_2 or equally among them). (19)

C. Summary of Performances

The mathematical equations derived for the two alternate-cascaded inverters can be used to compute voltage stresses experienced by their components. Relevant expressions obtained are summarized in Table I. These expressions can equally be used for computing stresses experienced by the conventional Z-source inverter [1] and noncascaded SL and TL inverters if the simplifications spelled in the last two rows of Table I are substituted accordingly. Also given in Table I are expressions for computing inductor current in each SL cell and magnetizing current in each TL cell. These expressions can further be used to compute current stresses experienced by other components if needed. For illustration, expressions for the shoot-through currents are included, which, according to Fig. 3, give the instantaneous switch current stresses of the rear inverter bridge.

TABLE II
PARAMETERS USED FOR SIMULATION AND EXPERIMENT

Parameter	Non-Cascaded SL	Alternate-Cascaded SL		Non-Cascaded TL	Alternate-Cascaded TL	
	Simulation	Simulation	Experiment	Simulation	Simulation	Experiment
N	1	2	2	1	2	2
V_{dc1}	NA	50 V	160 V (G2)	NA	50 V	200 V (G2)
V_{dc2}	NA	50 V	0 V	NA	50 V	0 V
Total V_{dc}	100 V	100 V	160 V	100 V	100 V	200 V
γ_{SL} or γ_{TL}	$\gamma_{SL} = 4$	$\gamma_{SL} = 2$	$\gamma_{SL} = 2$	$\gamma_{TL} = 3$	$\gamma_{TL} = 1$	$\gamma_{TL} = 1$
Inductor or Winding L	1.35 mH	1.35 mH	1.35 mH	500 μH	500 μH	500 μH
$C_a = C_b$	220 μF	NA	NA	220 μF	NA	NA
$C_{1b} = 2C_{1a}$ $C_{Na} = 2C_{Nb}$	NA	C_{1a}=220 μF C_{1b}=440 μF	C_{1a}=220 μF C_{1b}=440 μF	NA	C_{1a}=220 μF C_{1b}=440 μF	C_{1a}=220 μF C_{1b}=440 μF
AC Filter L	5 mH	5 mH	5 mH	5 mH	5 mH	5 mH
AC Load R	30 Ω	30 Ω	30 Ω	30 Ω	30 Ω	30 Ω
M	0.89 × 1.15	0.875 × 1.15	0.9 × 1.15	0.89 × 1.15	0.875 × 1.15	0.9 × 1.15
d_{ST} (boost)	0.11	0.125	0.1	0.11	0.125	0.1
d_{ST} (buck)	0	0	0	0	0	0
Modulating Frequency	50 Hz	50 Hz	50 Hz	50 Hz	50 Hz	50 Hz
Carrier Frequency	5 kHz	5 kHz	8.6 kHz	5 kHz	5 kHz	8.6 kHz

V. PERFORMANCE COMPARISON IN SIMULATION

The proposed alternate-cascaded SL and TL Z-source inverters were first simulated in Matlab/Simulink for comparison with their noncascaded correspondences. Modulation scheme used for the inverters was the same as that developed earlier for the conventional Z-source inverter since the main purpose here was still to generate shoot-through, non-shoot-through active, and null states [1]. Other details about parameters used for the simulations can be read from Table II.

A. Alternate Versus Noncascaded SL Topologies

The alternate-cascaded SL Z-source inverter was simulated with two networks ($N = 2$) and two inductors ($\gamma_{\rm SL} = 2$) per SL cell. Each network was powered by a 50-V dc source placed in series with its input diode, hence giving a total of $V_{\rm dc} = 100$ V for the two networks. With these simulation models and the control parameters read from Table II, Fig. 4 shows the waveforms obtained for the alternate-cascaded SL inverter. The dc-link and capacitor voltages read from the figure are 280 and 110 V, respectively, which certainly are close to those computed using (12).

The noncascaded SL inverter was also simulated but with only one network and four inductors per SL cell, giving $N' = 1$ and $\gamma'_{\rm SL} = 4$ ($'$ is added here to represent the noncascaded case). These parameters cause denominator of (2) for the noncascaded inverter to be the same as that of (12) for the alternate-cascaded inverter. The dc source powering the noncascaded inverter was also set to 100 V and was placed in series with the input diode shown in Fig. 1(a). Shoot-through time chosen here for the noncascaded case was slightly shorter than that for the alternate-cascaded inverter if they were to produce the same input-to-output voltage gain $\hat{v}_{\rm ac}/V_{\rm dc}$. Values read from Table II are thus $d'_{\rm ST} = 0.11$ for the noncascaded inverter and $d_{\rm ST} = 0.125$ for the alternate-cascaded inverter. Other possible values can be read from Fig. 5, which, when iterated, can be used to draw those comparative plots shown from Figs. 6–8.

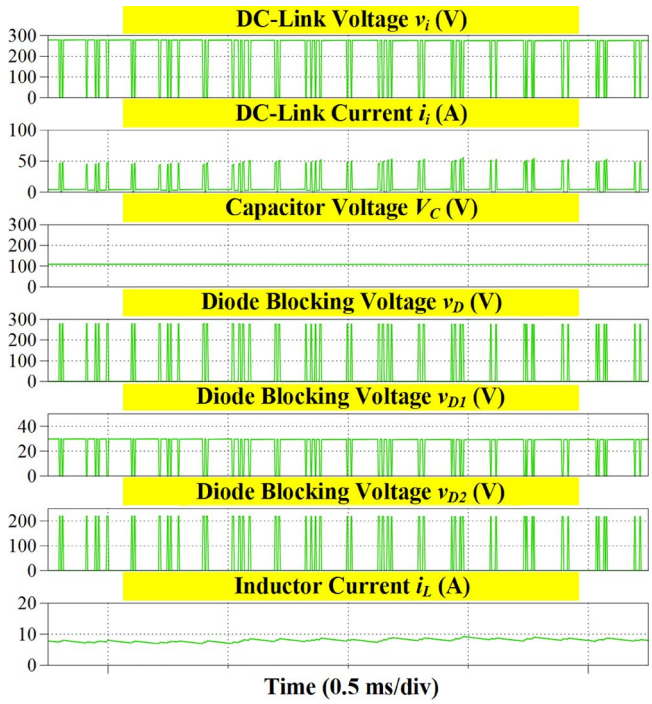

Fig. 4. Simulation results obtained for alternate-cascaded SL Z-source inverter with $N = 2$, $\gamma_{\rm SL} = 2$, $d_{\rm ST} = 0.125$, and $M = 0.875 \times 1.15$.

Fig. 6 specifically shows the capacitor voltage ratio of the alternate-cascaded and noncascaded SL inverters, which, as intended, is always smaller than one. The peak diode voltages $\hat{v}_D$, $\hat{v}_{D1}$, and $\hat{v}_{D2}$, whose subscripts represent those diode notations used in Fig. 1(b) and (c), are, however, greater than one, as demonstrated by those curves plotted in Fig. 7. That

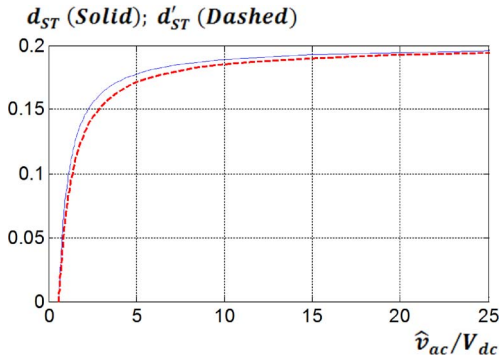

Fig. 5. Shoot-through durations of alternate-cascaded and noncascaded Z-source inverters with the same $\hat{v}_{\rm ac}/V_{\rm dc}$ gain.

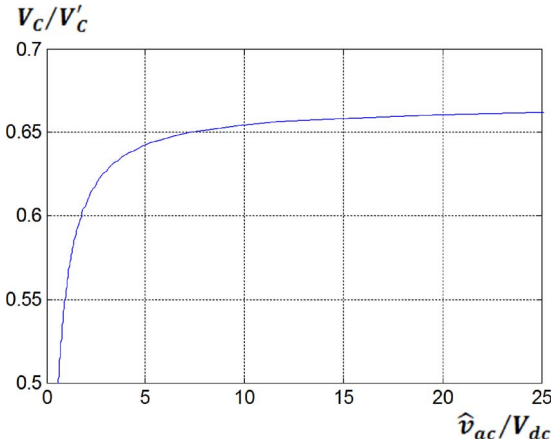

Fig. 6. Capacitor voltage ratio of alternate-cascaded and noncascaded Z-source inverters with the same $\hat{v}_{\rm ac}/V_{\rm dc}$ gain.

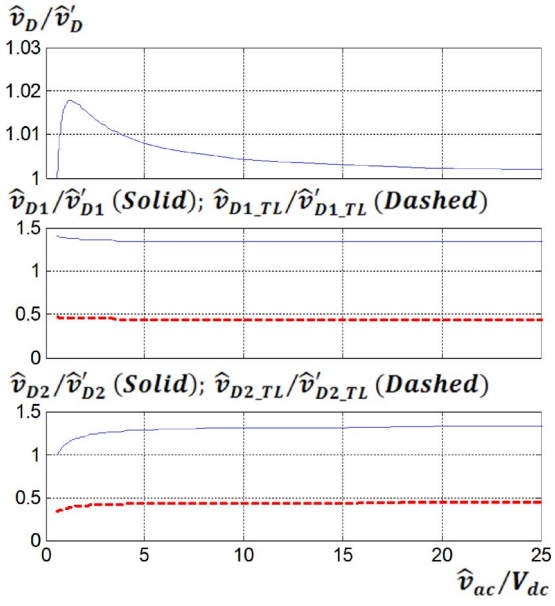

Fig. 7. Diode voltage ratios of alternate-cascaded and noncascaded Z-source inverters with the same $\hat{v}_{\rm ac}/V_{\rm dc}$ gain.

means diodes of the alternate-cascaded SL inverter are more stressed than their noncascaded counterpart. This, however, is not likely to be a problem since the highest diode voltage is always $\hat{v}_D$ according to Table I, which is at most only 2% higher than the noncascaded value. That should comfortably be compensated by the eight lesser diodes saved by the alternate-cascaded SL inverter (11 as compared to 19 needed by the noncascaded circuit).

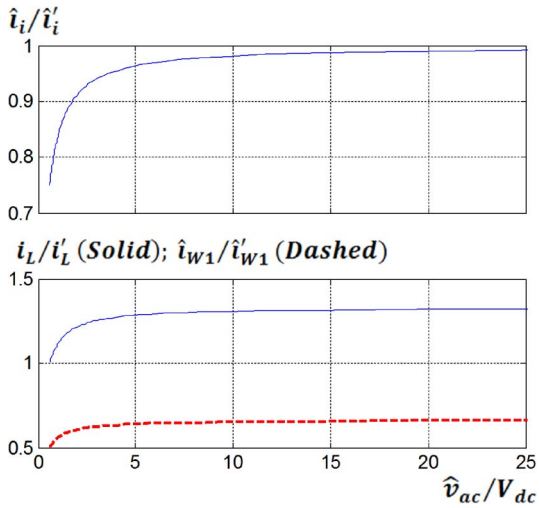

Fig. 8. Current ratios of alternate-cascaded and noncascaded Z-source inverters with the same $\hat{v}_{\rm ac}/V_{\rm dc}$ gain.

Besides voltages, relevant current ratios are also plotted in Fig. 8 to show the slightly lower shoot-through current carried by the alternate-cascaded SL inverter. Its individual inductor current i_L is, however, higher since there are two lesser inductors to share the demanded current (six as compared to eight found in the noncascaded circuit). This is unlikely a problem since the inductor current is continuous with no high instantaneous peak.

The aforementioned findings can further be extended to cases with higher N and $\gamma_{\rm SL}$. In general, if N is more prominent, the capacitor voltage ratio and shoot-through current would be smaller but not the diode voltage ratios and individual inductor current. The latter two would, however, be manageable since the increase in highest diode voltage is not expected to be high and the inductor current would remain as continuous with no high instantaneous peak. The reverse would happen for more prominent $\gamma_{\rm SL}$, whose behaviors will slowly approach those of the noncascaded inverter.

B. Alternate Versus Noncascaded TL Topologies

Comparison was next performed for the alternate-cascaded and noncascaded TL Z-source inverters. The alternate-cascaded inverter was realized with two networks $(N = 2)$ and a unity turns ratio $(\gamma_{\rm TL} = 1)$ for the TL cell shown in Fig. 1(d). Each network had a 50-V dc source connected in series with its input diode, hence giving a total $V_{\rm dc}$ of 100 V. These parameters, together with those control parameters listed in Table II, led to those waveforms shown in Fig. 9, where high instantaneous voltages and currents can clearly be seen. When powered by a 100-V dc source in series with its input diode, the same waveforms, but with different amplitudes, were also observed for the noncascaded SL inverter whose parameters were $N' = 1$ and $\gamma'_{\rm TL} = 3$. These parameters led to the same denominator for (3) and (17), which can now be compared by adjusting their

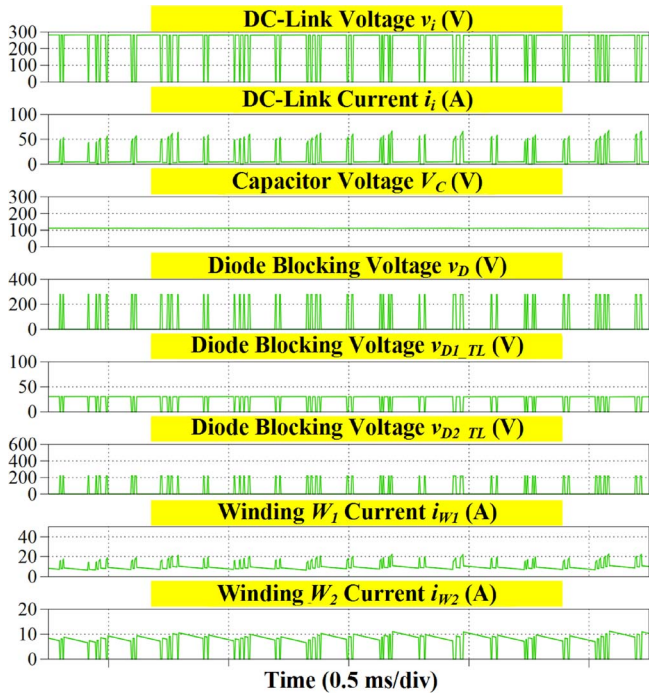

Fig. 9. Simulation results obtained for alternate-cascaded TL Z-source inverter with $N = 2$, $\gamma_{\rm TL} = 1$, $d_{\rm ST} = 0.125$, and $M = 0.875 \times 1.15$.

shoot-through durations in accordance to Fig. 5 to keep their gains similar.

The comparative figures eventually obtained for the TL inverters are similar to those shown from Figs. 6–8, except for those three thick dashed curves shown in Figs. 7 and 8. For the first two shown in Fig. 7, they inform that, unlike the SL inverters, the alternate-cascaded TL inverter imposes smaller voltage stresses across its diodes $D_{1\_\rm TL}$ and $D_{2\_\rm TL}$ in each TL cell. Complementing, the third dashed curve shown in Fig. 8 informs that high winding current flowing through $W1$ is greatly reduced by the alternate-cascading technique, which certainly is a favorable feature. These advantages of the alternate-cascaded TL inverter will further strengthen whenever N is raised to up its prominence.

C. Alternate-Cascaded Versus Conventional Topologies

Comparison is next performed between the alternate-cascaded and conventional Z-source inverters with the former using the same circuit parameters of $N = 2$ and $\gamma_{\rm SL} = 2$ or $\gamma_{\rm TL} = 1$. Both inverters are set to produce the same input-to-output voltage gain $\hat{v}_{\rm ac}/V_{\rm dc}$ by using those shoot-through times shown in Fig. 10. In that figure, superscript z has been added to identify the conventional Z-source inverter, whose shoot-through time is at least 2.5 times longer. Corresponding voltage and current ratios obtained are shown in Fig. 11, whose important findings are summarized as follows.

1) First plot: Capacitor voltages of the alternate-cascaded SL and TL inverters are always kept below 0.5 times ($\leq 1/N$, where $N = 2$) that of the conventional Z-source inverter. Placing the sources at other locations shown in Fig. 3 will not affect this finding.

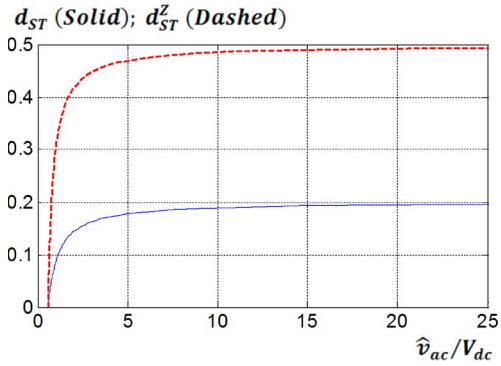

Fig. 10. Shoot-through durations of alternate-cascaded and conventional Z-source inverters with the same $\hat{v}_{\rm ac}/V_{\rm dc}$ gain.

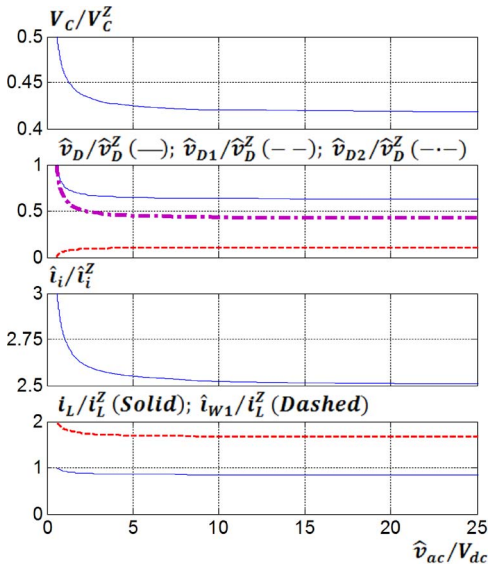

Fig. 11. Voltage and current ratios of alternate-cascaded and conventional Z-source inverters with the same $\hat{v}_{\rm ac}/V_{\rm dc}$ gain.

2) Second plot: At gain close to unity, $\hat{v}_D = \hat{v}_{D2} = \hat{v}_D^Z$ is low and equal to the input voltage $V_{\rm dc}$ of the SL inverter. It gives rise to two ratios that start at one and fall to 0.64 and 0.4, respectively, as the gain and actual diode voltages increase rapidly ($\gg V_{\rm dc}$). The third ratio linked to $\hat{v}_{D1}$, unlike the earlier two, increases with the gain to an upper limit of 0.13. The same variations are produced by $\hat{v}_{D1\_\rm TL}$ and $\hat{v}_{D2\_\rm TL}$ of the TL inverter, which are thus not duplicated here.
3) Third plot: Shoot-through currents of the alternate-cascaded inverters are 2.5–3 times higher. They are caused by shorter shoot-through durations, whose corresponding instantaneous currents must be higher.
4) Fourth plot: Individual inductor current of the alternate-cascaded SL inverter is 0.8 times smaller. In contrast, magnetizing current of the alternate-cascaded TL inverter is 1.6 times higher but contributed by two coupled windings. Per winding wise, the current would be 0.8 times smaller.

In addition to those observations noted from Fig. 11, it should be mentioned here that maximum modulation ratio M of the alternate-cascaded inverters can always be kept above

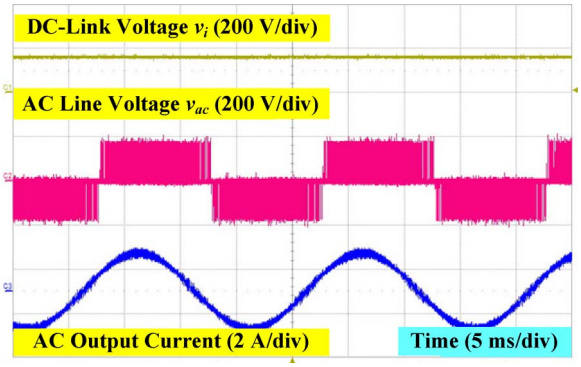

Fig. 12. Experimental results obtained for alternate-cascaded SL Z-source inverter with $N = 2$, $\gamma_{\rm SL} = 2$, $d_{\rm ST} = 0$, and $M = 0.9 \times 1.15$.

0.8 as compared to 0.5 for the conventional Z-source inverter. Better utilization of the dc-link voltage is thus achieved by the alternate-cascaded inverters, whose spectral performances would hence be better. Voltage stresses endured by switches (SA to SC′ in Fig. 3) of the alternate-cascaded inverters would also be lower and is, in fact, similar to $\hat{v}_D/\hat{v}_D^Z$ shown in Fig. 11. The switch stresses at high gain experienced by the alternate-cascaded inverters can thus be read as 0.64 times lower from the figure.

VI. Experimental Results

The advantages of the alternate-cascaded SL and TL Z-source inverters have already been clarified with reference to their noncascaded correspondences. Experimental results are now presented for validating their practicalities. For the alternate-cascaded SL inverter, two impedance networks and three SL cells with two inductors each were built, giving rise to $N = 2$ and $\gamma_{\rm SL} = 2$. Control parameters used were arbitrarily set as $d_{\rm ST} = 0$ and $M = 0.9 \times 1.15$ for the voltage-buck mode and as $d_{\rm ST} = 0.1$ and the same M for the voltage-boost mode. The latter gave an anticipated boost factor of $(1 + 0.1)/(1 - 5 \times 0.1) = 2.2$. Other system parameters used were kept the same as in the simulation and listed in Table II unless stated otherwise.

With the alternate-cascaded SL inverter powered by a dc source of 160 V placed at its dc link (G2 in Fig. 3), Fig. 12 shows the results captured under voltage-buck mode. The dc-link voltage shown in the figure is clearly not chopped, but kept constant at 160 V, from which an ac peak current of 1.8 A is obtained. The dc-link voltage obviously changes when entering the voltage-boost mode represented by Fig. 13. Instead of being constant, the dc-link voltage in Fig. 13(a) switches between zero and a peak of 320 V. This represents a boost factor of two, which is close to the computed value of 2.2 after accounting for parasitic losses in a real system. The boosted ac peak current is read as 3.5 A, which again represents a gain close to two (ac and dc gains are the same because of the same M used). Fig. 13(b) further shows the capacitor voltage V_C and inductor current i_L of one network, which clearly are continuous except for some switching noises superimposed. These noises are not seen in simulation and are thus likely picked up from the hardware semiconductor switching. Unlike V_C and i_L, the dc-link current

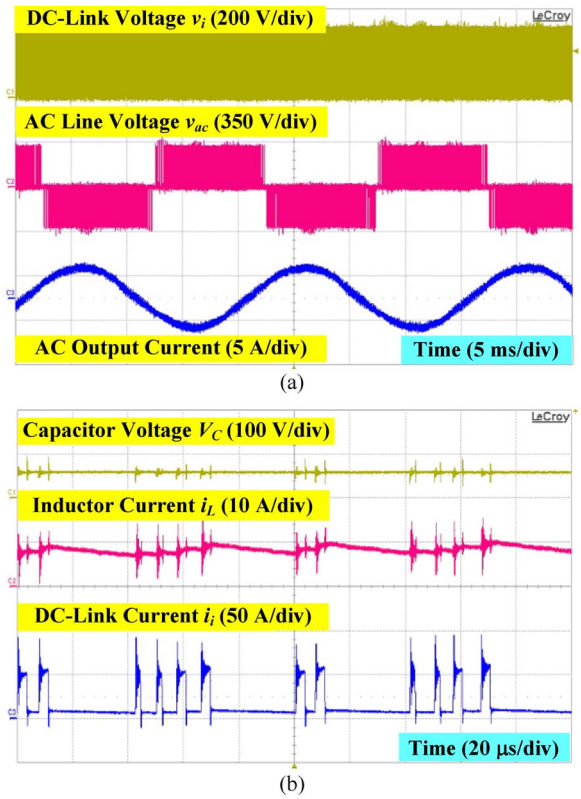

Fig. 13. Experimental results obtained for alternate-cascaded SL Z-source inverter with $N = 2$, $\gamma_{\rm SL} = 2$, $d_{\rm ST} = 0.1$, and $M = 0.9 \times 1.15$.

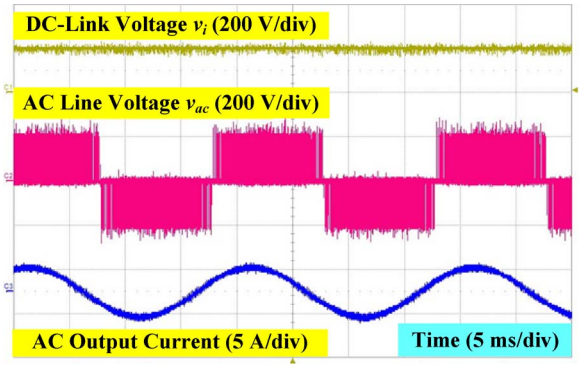

Fig. 14. Experimental results obtained for alternate-cascaded TL Z-source inverter with $N = 2$, $\gamma_{\rm TL} = 1$, $d_{\rm ST} = 0$, and $M = 0.9 \times 1.15$.

shown in the same figure is chopping with high instantaneous values detected during shoot-through.

The experimental setup was next configured as an alternate-cascaded TL Z-source inverter with two networks in cascade $(N = 2)$ and three 1:1 TLs $(\gamma_{\rm TL} = 1)$. Control and system parameters used were kept unchanged, meaning that the same boost factor of 2.2 was anticipated. Also anticipated was the less ideal performance caused by leakage inductance of the TLs, which should reflect as noisier waveforms in the following experimental figures.

The alternate-cascaded TL inverter was eventually powered by a dc source of 200 V placed at its dc link (G2 in Fig. 3), whose results are shown in Figs. 14 and 15. Fig. 14 shows the results for voltage-buck mode, whose dc-link voltage and ac peak current are read as 200 V and 2.5 A, respectively. The

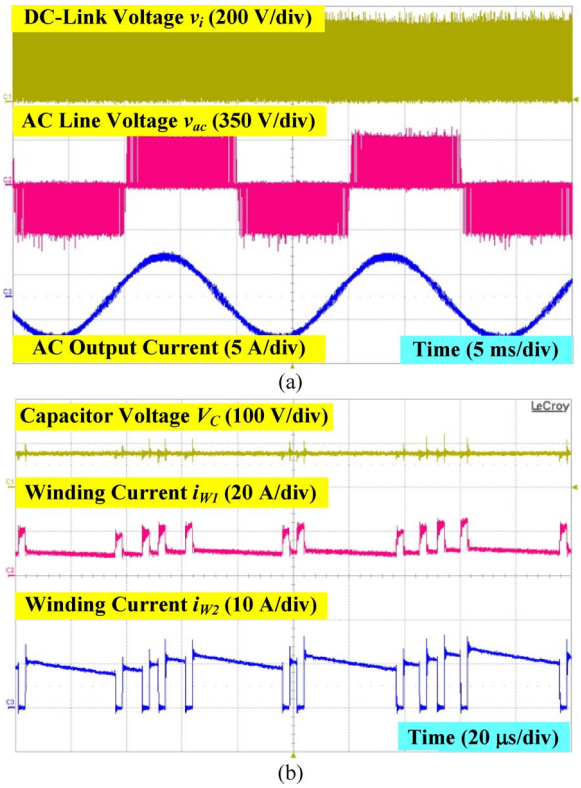

Fig. 15. Experimental results obtained for alternate-cascaded TL Z-source inverter with $N = 2$, $\gamma_{\rm TL} = 1$, $d_{\rm ST} = 0.1$, and $M = 0.9 \times 1.15$.

dc-link voltage is subsequently boosted to 380 V in Fig. 15(a), representing a boost factor of 1.9, which is close to the computed value of 2.2. The boosted ac peak current is also read as 5 A, which, when divided by the 2.5 A read from Fig. 15(a), gives a correct ac gain of two (close to the dc gain because of the same M used). Fig. 15(b) further shows the capacitor voltage V_C and winding currents i_{W1} and i_{W2} of the alternate-cascaded TL inverter. These waveforms match those simulated in Fig. 9, which certainly helps to strengthen findings presented in this paper.

VII. Conclusion

This paper has presented a new family of alternate-cascaded SL and TL Z-source inverters with enhanced voltage boost in addition to their usual voltage-buck ability. Unlike other inverters, the inverters proposed here allow voltage gains to be freely set by tuning two control parameters that can also be used to minimize voltage and current stresses endured by their components. Mathematical proofs, simulation, and experimental results have demonstrated these advantages, as well as confirmed the practicalities of the inverters.

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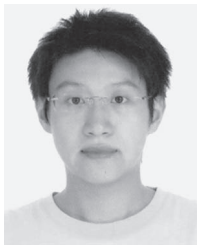

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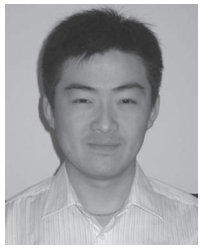

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