

# Contrast Optimization in a Multi-Windowing Image Processing Architecture

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## Abstract

It is well known that the most vision applications are often focused on several small image ranges and consequently the whole image acquisition is not necessary. From this definition, it is evident that one of the main goal of an efficient vision sensor is to select windows of interest (WOI) in the image and concentrates processing resources on it. This notion is crucial for the choice of the imaging technology. For the conception of our sensor, called *SeeMos*, FPGA architecture and a CMOS Imager have been chosen. The main advantage of CMOS imagers is to adopt a digital memory style readout, using the row decoders and column amplifiers. Random access of pixel values becomes possible, allowing selective readout of windows of interest (WOI). But most of applications consider a wide dynamic range scene with intensity variations of more than 6 decades and the different selected WOI need specific contrast settings. With our sensor, we propose a method to optimize the contrast stretching in each WOI. The approach is based on a servoing loop which controls the Analog/Digital Converter parameters. As result, several gray-level snapshots illustrate the validity of our approach.

## 1 Introduction

Traditionally, an image is transduced by a sensor (camera), converted and stored (image grabber) and processed on a host computer [7]. A classical controversy in theories of visual perception is whether the processing of visual information proceeds in parallel or sequentially. This computational aspect is crucial for many real-time applications and in the

most cases, the programmable devices become the best option. In this way, we have chosen to build a versatile embedded smart camera based on a high density FPGA and the CMOS imaging technology. Actually, new CMOS-APS imagers and CCD sensors present very similar performances, but CMOS imagers have an additional interest property. The structure of these sensors includes an integrated addressing device which allows a random access to the pixels. This advantage (random access readout) allows reading only few pixels and contrary to the CCD imagers, it is possible to obtain a high speed imaging capability. This particularity is very useful in image processing where the most vision applications are often focused on several small image ranges and consequently the whole image acquisition is not necessary. Consequently, it is evident that one of the main goals of an efficient vision sensor is to select windows of interest (WOI) in the image and concentrates processing resources on it. Moreover, the CMOS imagers are capable of imaging high dynamic range scenes without saturation. For these reasons of high dynamic and high frame rate, together with random accessibility of pixels, the CMOS imaging is very useful in many fields.

In this paper, we focus on the optimization of the contrast from the high dynamic range image. Indeed, outdoor real world scenes have dynamic intrascene ranges that might extend about 5 decades [6]! Consequently, when imaging natural scenes the response of the classical sensors (CCD or linear CMOS) saturates in parts of the scene. To overcome these problems several techniques have been proposed. Most of these techniques are based on "on-chip" methods as multi-sampling, threshold detection, integration time control [1] [4] [3]. Others approaches consider illumination techniques for a best optical dynamic range [2]. But a wide dynamic implies a weak contrast in a homogenous enlightened scene. Consequently the high dynamic is not always the best way or it is necessary to adapt the signal con-

ditioning.

The paper is arranged as follows. In the next section, a short overview of the sensor is presented. This is followed in section III by a description of the control laws for the contrast optimization and in a last section few results illustrates our method.

## 2 Overview of the sensor

The *SeeMos* sensor is a smart camera dedicated to active vision. The core of this camera is based on a FPGA and a CMOS imager. The global processing system is composed of System On Programmable Chip (SOPC) by which an entire system of components is put on a single chip (FPGA)(Fig.1).

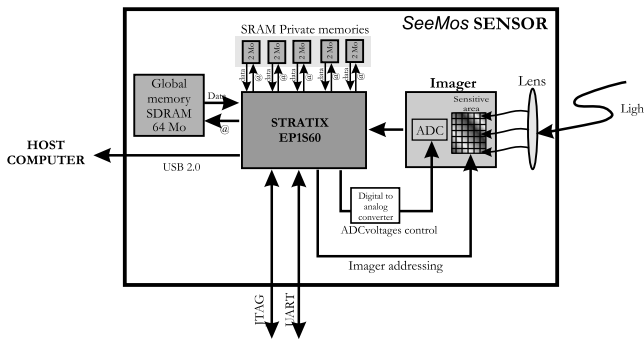


Figure 1: Architecture of the sensor

The global system is integrated into a modular architecture composed of three modules :

- **Main board** : This is the core of the system. It was designed around a FPGA Stratix EP1S60 manufactured by Altera which is connected to 5 SRAM (2MB) and a SDRAM (64MB). Of course, this component enables a high density of integration (57120 Logic Elements), but three main advantages of this component led us to this choice. *Stratix* is optimized to maximize the performance benefits of SOPC integration based on a *NIOS* embedded Processor. A *NIOS* processor is a user-configurable soft core processor, allowing many implementations and optimization options. *Stratix* integrates *DSP Blocks*. These embedded *DSP Blocks* have been optimized to implement several DSP functions with maximum performance and minimum logic resource utilization. The *Stratix* device incorporates a configurable internal memory called TriMatrix memory. The TriMatrix memory is composed of three sizes of efficient embedded RAM blocks.

- **Imaging device board** : This board is composed of a CMOS imager manufactured by Neuricam. This imager allows full 2D addressing with a column bus and a row bus. This imager has a resolution of  $640 \times 480$  (VGA) and provides a

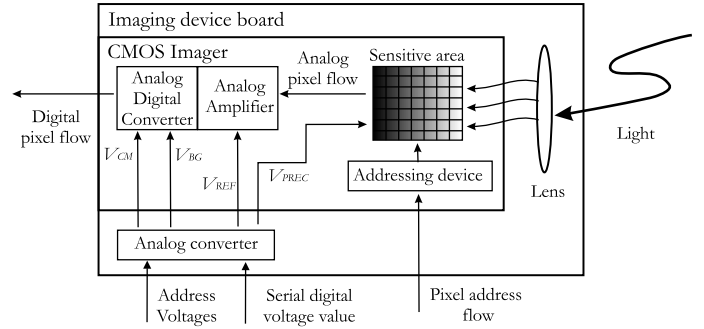


Figure 2: Imaging device board synoptic

broad dynamic range (120db) due to the pixel structure, which has a logarithmic response. Four analog converters allow to control four analog voltages of the imager: Analog signal offset, Digital conversion range, voltage reference and a pixels precharge voltage. In this work, these four converters are used to optimize the conversion range.

- **Communication board** : This last board is connected to the main board and manages all communications with a host computer. The communication bus is actually high-speed USB2.0.

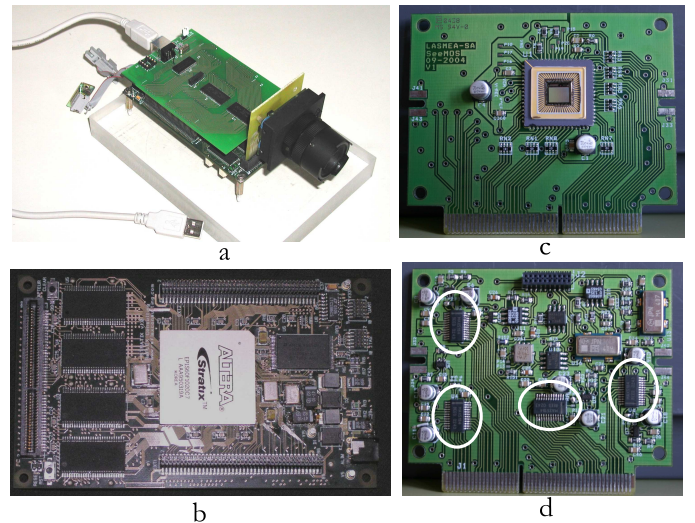


Figure 3: a - camera, b - top view of the main board, c - front view of the imaging board, d - back view of the imaging board (The circles show the 4 converters)

An overview of the embedded vision system is proposed on figure 3.

## 3 Dynamic contrast optimization

In this section, a method is proposed to optimize the image contrast in spite of illumination variations.

As it is written above, the imager used in our sensor has a log-response, in others terms, the output voltage is proportional to the logarithm of the light intensity over more than five decades of illumination.

In many cases, the illumination in each WOI is homogenous and only a small part of the log response is used; consequently the contrast is weak. In order to enhance continuously image contrast, a visual feedback is performed on CMOS imager read out circuit to adapt pixels transduction chain. The set of three voltage references of analog amplifier and analog to digital converter are controlled according to digital pixels values variations.

A reference voltage  $v_{ref}$  allows to maintain pixel output voltage centered on the output voltage of amplifier in order to avoid the distortions that occur close to the supply rails. And during digitalization step, the reference voltages  $v^+$  and  $v^-$  are respectively set to the top and bottom limits of the conversion range. These three voltage references are used in a triple servoing loops in order to avoid video amplifier saturation and to adapt the levels of the Analog/Digital conversion range to the current visual signal.

### 3.1 Servoing loops

The control loop applied to the three voltage references is proposed on the figure 4. The maximum

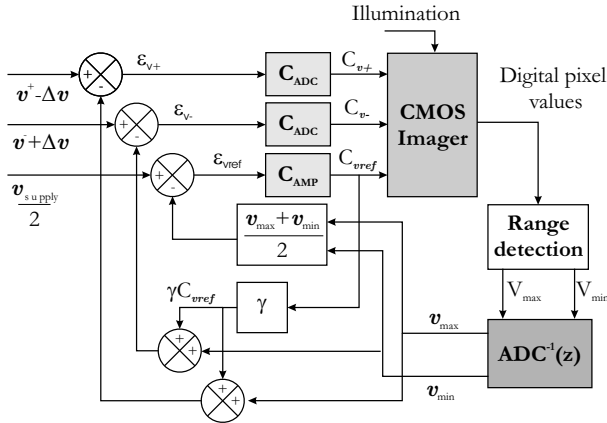


Figure 4: Servoing process of read out imager circuit.

$V_{max}$  and minimum  $V_{min}$  values are extracted in order to estimate the digital signal range. An inverse model of analog digital converter is used in order to evaluate the maximum  $v_{max}$  and minimum  $v_{min}$  values of amplifier output signal. In the Analog/Digital conversion range, the amplifier output signal is given by:

$$v = \frac{V}{2^N - 1}(v^+ - v^-) + v^-$$

where  $N$  is the number of digitalization bits and  $v$  is the analog signal and  $V$  is the digital signal.

So, the  $v_{ref}$  voltage is servoing on center of the amplifier output signal  $v$  considered as reference feature. The half of amplifier supply voltage defines the reference of a proportional ( $C_{AMP}$ ) controller and allows to avoid analog amplifier saturation. In order to optimize the digitalization process, the voltage references  $v^+$  and  $v^-$  are respectively controlled according to the evaluation of  $v_{max}$  and  $v_{min}$ . The references of these two proportional ( $C_{ADC}$ ) controller include a tolerance margin  $\Delta v$ . When amplifier output voltage is outside the range of digital conversion, the measurements of  $V_{max}$  and  $V_{min}$  are wrong because the system is not linear. The tolerance margin  $\Delta v$  allows to ensure the validity of  $V_{max}$  and  $V_{min}$  measurements. Lastly, considering the amplifier gain  $\gamma$  and the dependance of the servoing loops, the correction which is applied to  $v_{ref}$  voltage is included in the two others servoing loops. The value  $\gamma \cdot C_{vref}$  is added to  $v_{max}$  and  $v_{min}$  values to anticipate the effect of  $v_{ref}$  correction on  $v^+$  and  $v^-$  controls.

### 3.2 FPN correction

One of the main problem with logarithmic pixels is that the quality of the resulting output image is severely degraded by fixed pattern noise (FPN). The FPN is caused by mismatches between the components of each pixel. A calibration stage is necessary to alleviate the dissimilarities of the pixel responses. An image of reference which stores the offset values between the pixels responses when exposed to the same illumination is added to the raw image.

In our case, the digital conversion range is modified continually. In order to release an efficient fpn correction during servoing process, this image of reference is refreshed according to the variation of the digital conversion range. The equation which allows to adapt the image of reference is as follows :

$$(I_{ref}(i))^k = \frac{(I_{ref}(i))^0 \cdot (v^+ - v^-)^0}{(v^+ - v^-)^k}$$

where  $i$  is the pixel index,  $k$  indicates a specific state of read out imager circuit,  $(I_{ref}(i))^k$  is the image of reference evaluated for a specific state of read out imager circuit and  $(I_{ref}(i))^0$  stores the offset values between the pixels responses.

## 4 Experimental results

The implemented system allows to manage several windows of interest. The generation of pixels address and the servoing loops are performed independently[5]. Then, the contrast of each window of interest is optimized locally. In this section,

two set of images are proposed to illustrate the servoing process efficiency.

Firstly, on figure 5 a lamp is placed in front of the image sensor. The image on left result of standard adjustment of read out imager circuit, and the right image is the result obtained with the servoing process. The image histogram distribution is improved and previous saturations are removed. The third image is a zoom on filament bulb of the lamp. In spite of extreme illumination conditions, none saturation is observed. The second sequence of images (fig. 6)

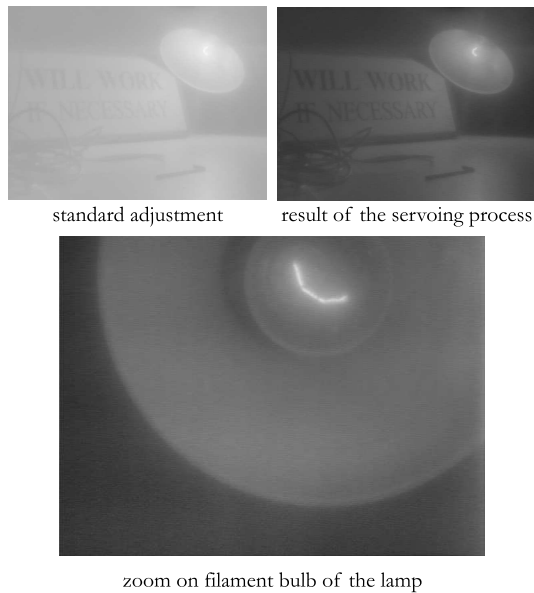


Figure 5: Images resulting from high level of illumination

illustrates the results for two windows of interest. The first image is obtained with servoing process on the global image. The two small images are the results of local windows of interest. One is located on a region of correct illumination conditions and the second is on dark part of the scene. The windows of interest use different states of read out imager circuit to adapt image transduction.

## 5 Conclusion

In this paper, an embedded vision system based on a CMOS imager is presented. The interest of this imaging technology is illustrated with a method of dynamic contrast optimization. The memory style read out of CMOS imager is used to address local windows of interest. A servoing process allows to adapt read out imager circuit according to local illumination signal. The results demonstrates the efficiency of the approach which allows an adaptation of the vision system according to the illumination variations of a real environnement.

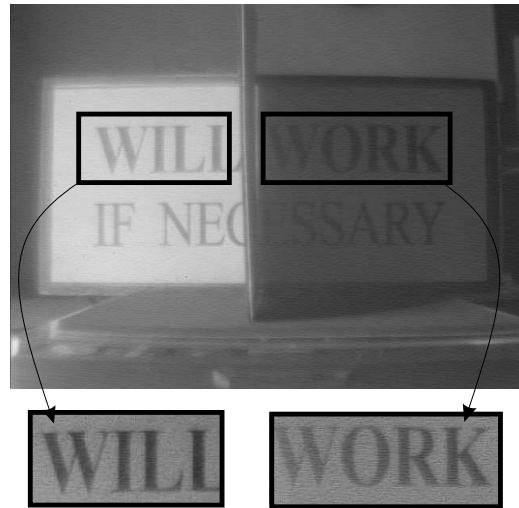


Figure 6: Illumination adaptation of local windows of interest

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