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Error Reduction for Temperature Detection Unit of Sigma-Delta High Resolution Temperature Sensor

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Abstract. *The differential base-emitter voltage of two bipolar transistors under different current density can be used to measure the temperature, since it is proportional to absolute temperature (PTAT) with high linearity and little correlative to process. It can be transferred to a $\Sigma-\Delta$ modulator to generate digital output, which is further filtered and extracted to remove the quantized noise. In this paper, several non-ideal factors which affect the transfer precision related to the temperature sensing unit are first introduced and analyzed. Then, in order to reduce the error, the triode parasitic resistance elimination technology is used to eliminate the parasitic resistance, and the dynamic element matching technique is applied to improve the current mirrors' and capacitors' matching degree. Both analytic proof and simulation results show the effectiveness of the proposed scheme.*
Keywords: High resolution temperature sensor, $\Sigma-\Delta$ modulator, Temperature detection unit, Error reduction.

1. **Introduction.** In recent years, with the advance and development in temperature measurement and material technologies, many new kinds of temperature sensors continuously come into the market, such as optical fiber temperature sensors [1], ultrasonic temperature sensors [2], magnetic resonance temperature sensors [3], microwave temperature sensors [4], PN junction temperature sensors [5], and so on. Among them, PN junction temperature sensors become the most powerful induction-based temperature devices due to their good stability, high temperature sensitivity, ease of integration and low cost advantages. In a conventional CMOS process, a PN junction has three kinds of voltage with different temperature characteristics, i.e., the voltage with a positive temperature coefficient, the voltage with a negative temperature coefficient, and the voltage independent of temperature.

Since temperature is a natural analog signal that changes very slowly, thus we can improve the Signal to Quantization Noise Ratio (SQNR) and increase the precision of

the analog-digital conversion of the temperature sensor by adopting a very large oversampling factor. The main principle of the $\Sigma-\Delta$ modulator [6] is to use the oversampling and noise shaping technologies to improve SQNR, and these two technologies have been already suggested as early as in 1946 and 1954. In fact, the $\Sigma-\Delta$ modulator has been there for more than 40 years. However, because of the technical restrictions of Integrated Circuits (IC) forty years ago, the idea of improving the precision at the cost of increasing the sampling rate was not popular at that time. Up to 1980's, with the continuous improvement of the VLSI technology, the chip area is gradually reduced, thus the on-chip noise is a major factor limiting high-precision A/Ds. At the same time, since the transistor feature size is reduced, the processing speed of digital circuits is greatly improved, which makes the advantages of digital $\Sigma-\Delta$ modulators in high-precision A/D convertors clear.

In order to be able to detect the temperature change, it is necessary to convert the temperature information into the voltage and/or current information which can be detected with the circuit. Since both the base-emitter voltage $V_{\mathtt{be}}$ of a bipolar transistor and the base-emitter voltage difference $\Delta V_{\mathtt{be}}$ between two bipolar transistors under different current densities are temperature dependent. Among them, the $\Delta V_{\mathtt{be}}$ value has a good linear relationship with temperature, and it does not change with the process, thus the paper just adopts the property of proportional to absolute temperature (PTAT) [7] of $\Delta V_{\mathtt{be}}$ to achieve the temperature measurement. In addition to finding a temperature-dependent voltage, we also need a temperature independent reference voltage to convert the temperature information into digital information to be read and calculated by other modules. In this paper, we do not specifically design a reference voltage, but embed the reference voltage design into the $\Sigma-\Delta$ modulator design, that is, using $V_{\mathtt{be}}$ and $\Delta V_{\mathtt{be}}$ indirectly to achieve a reference voltage. The rest of this paper is organized as follows. Section 2 gives the measurement principle of the temperature detection unit. Section 3 analyzes the error introduced from the temperature detection unit. Section 4 introduces our solutions to reducing the error. Section 5 provides some simulation results. Section 6 concludes the whole paper.

2. **Measurement Principle.**

2.1. **The Relationship between the Base-emitter Voltage and Temperature.**

For a bipolar device, there is an exponential relationship between its collector current I_C and its base-emitter voltage $V_{\mathtt{be}}$, which is usually expressed as:

$$I_C = I_S \mathtt{exp}(\frac{V_{\mathtt{be}}}{\eta V_T}) \tag{1}$$

Where I_S is the saturation current and $V_T = kT/q$ is the thermal voltage. Here, $k = 1.38 \times 10^{-23}\mathtt{J/K}$, $q = 1.6 \times 10^{-19}\mathtt{C}$, and thus $V_T = 26\mathtt{mV}$ at room temperature. For a real PN junction, the non-ideality factor η in Eq. (1) is about between 1.05 and 1.1, and for a diode-connected bipolar transistor, $\eta = 1$, and thus we adopt the later as the temperature sensing element. Therefore, Eq. (1) can be rewritten as:

$$V_{\mathtt{be}} = V_T \ln(\frac{I_C}{I_S}) \tag{2}$$

For the saturation current I_S, it has been shown that [8]

$$I_S = C \cdot T^{(4-n)} \mathtt{exp}(-\frac{V_{g0}}{V_T}) \tag{3}$$

Where C is a constant, n is the exponent with $n \approx 1.5$, V_{g0} is the voltage of V_T when T equals to absolute zero degree. Taking into account that, in the actual circuit, the

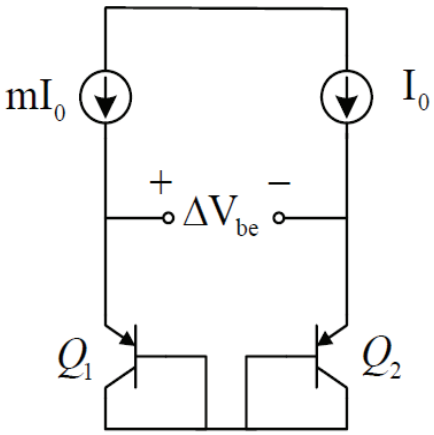

FIGURE 1. The circuit to generate the voltage with a positive temperature coefficient

collector current I_C also has a temperature coefficient, we assume that

$$I_C = D \cdot T^x \tag{4}$$

Where D is a constant and x is the exponent. Substituting Eqs. (3) and (4) into Eq. (2), we have

$$V_{\mathtt{be}} = V_{g0} + \frac{kT}{q}\ln(\frac{D}{C}) + [x-(4-n)]\frac{kT}{q}\ln(T) \tag{5}$$

As can be seen from Eq.(5), the relationship between $V_{\mathtt{be}}$ and T is not simply linear but it is a non-ideal equation with the higher order term $[x-(4-n)]kT/q\ln(T)$. However, from Eq. (5), it can be also found that, when the collector current has a positive temperature coefficient with $x = 4 - n$, it would eliminate the effect of the higher-order term [9], but the design is very difficult for generating such collector current with $x = 2.5$. Thus, we generally only take $x = 1$ to reduce the curvature of the PN junction temperature characteristic curve.

As we know, if the current density of two bipolar transistors is different, then the voltage difference $\Delta V_{\mathtt{be}}$ between them will show some positive temperature coefficient [10]. As shown in Fig.1, assuming that the area of the transistor $\mathtt{Q}_2$ is n times that of the transistor $\mathtt{Q}_1$, while the current flowing in $\mathtt{Q}_1$ is m times that of $\mathtt{Q}_2$, then we have:

$$\Delta V_{\mathtt{be}} = V_{\mathtt{be1}} - V_{\mathtt{be2}} = \frac{kT}{q}\ln(\frac{mI_0}{I_S}) - \frac{kT}{q}\ln(\frac{I_0}{nI_S}) = \frac{kT}{q}\ln(mn) \tag{6}$$

The derivation of Eq. (6) can be obtained as follows:

$$\frac{\partial \Delta V_{\mathtt{be}}}{\partial T} = \frac{k}{q}\ln(mn) \tag{7}$$

From Eq. (7), we can see that $\Delta V_{\mathtt{be}}$ eliminates the non-ideal property that the saturation current I_S brings, thus the linearity of the temperature characteristic curve is very good. In addition, as long as the matching between two current sources and the matching between two bipolar transistors are guaranteed, the on-chip consistency will be improved. Therefore, we generally adopt $\Delta V_{\mathtt{be}}$ as a sensor to sensing the temperature.

From above, we can see that $V_{\mathtt{be}}$ has a negative temperature coefficient while $\Delta V_{\mathtt{be}}$ has a positive temperature coefficient, thus we can easily think of using their summation to obtain a voltage reference with a zero temperature coefficient, i.e.,

$$V_{\mathtt{ref}} = V_{\mathtt{be}} + \alpha \Delta V_{\mathtt{be}} \tag{8}$$

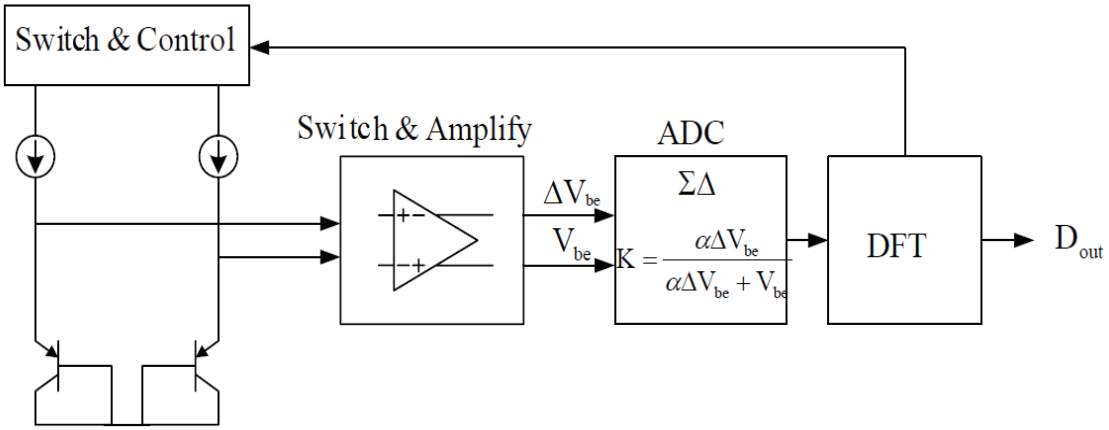

FIGURE 2. The general diagram of the $\Sigma - \Delta$ temperature sensor

According to Eq. (7) and $V_T = kT/q$, as long as the below relationship exists, we can obtain such a voltage with zero temperature coefficient.

$$\frac{\partial V_{\mathtt{ref}}}{\partial T} = 0 \Leftrightarrow \frac{\partial V_{\mathtt{be}}}{\partial T} = -\alpha \frac{\partial \Delta V_{\mathtt{be}}}{\partial T} \Leftrightarrow \frac{\partial V_{\mathtt{be}}}{\partial T} = -\alpha \frac{k}{q} \ln(mn)$$
$$\Leftrightarrow \frac{\partial V_{\mathtt{be}}}{\partial T} = -\alpha \frac{\partial V_T}{\partial T} \ln(mn) \Leftrightarrow \alpha \ln(mn) = -\frac{\partial V_{\mathtt{be}}/\partial T}{\partial V_T/\partial T} \tag{9}$$

In circuit design, it is important to produce a precision voltage reference since almost all of the ADCs require a reference voltage as the reference point of A/D conversion. From Eq. (8), we can see that, to get a very accurate reference voltage, the matching between the current source and transistor is very important. We will mention the dynamic element matching technology later in order to improve their matching degree.

2.2. **The Block Diagram of the Temperature Sensor.** The block diagram of the temperature sensor is roughly shown in Fig. 2.

As can be seen from Fig.2, to implement such a system, we require a current source reference, a $V_{\mathtt{be}}$ generation circuit, a $\Delta V_{\mathtt{be}}$ generation circuit, a $\Sigma - \Delta$ ADC, and a digital processing unit. Wherein $V_{\mathtt{be}}$ and $\Delta V_{\mathtt{be}}$ is modulated by the $\Sigma - \Delta$ ADC, and then processed by the digital processing unit to obtain a ratio proportional to the temperature:

$$K = \frac{\alpha \Delta V_{\mathtt{be}}}{V_{\mathtt{be}} + \alpha \Delta V_{\mathtt{be}}} \tag{10}$$

At the same time, the discrete characteristic of the $\Sigma - \Delta$ ADC provides a good platform for offset cancellation and the application of dynamic element matching technology. To make the change of the value K with the temperature have a very good linearity, it is necessary to make the denominator $V_{\mathtt{be}} + \alpha \Delta V_{\mathtt{be}}$ have small temperature dependence as shown in Eq.(9). In the actual chip, the value of K is not enough to get the value of the output temperature in Celsius degree, we need further processing. The final output temperature value is:

$$D_{\mathtt{out}} = K \cdot A + B \tag{11}$$

In our design, since when $T \approx 600\mathtt{K}$, $V_{\mathtt{be}} = 0$, and when $T = 0\mathtt{K}$, $\Delta V_{\mathtt{be}} = 0$, so that the full scale of the DAC is about 600K, i.e., $A = 600\mathtt{K}$, while $\mathtt{B}$ stands for the conversion constant between an absolute temperature and a Celsius degree, generally $B = -273$.

3. **Error Analysis.** In our DAC design, the oversampling ratio OSR is 12500. And by using the noise shaping technology, we can easily reach the precision of 14bit. So if just from the DAC's perspective, the final conversion accuracy can reach $0.07°\mathrm{C}/\mathtt{bit} \sim 0.08°\mathrm{C}/\mathtt{bit}$. Thus, the main facts that affect the final accuracy of the temperature sensor are the various errors brought by the temperature sensing unit. Assume the factor x that influences the temperature and the final output of the temperature $D_{\mathtt{out}}$ has the following relationship:

$$D_{\mathtt{out}} = f(x) \tag{12}$$

So there is

$$\Delta D_{\mathtt{out}} = \frac{\partial f(x)}{\partial x}\Delta x \tag{13}$$

To make the final output accuracy $\Delta D_{\mathtt{out}}$ of the temperature sensor less than the design precision ΔT, we require:

$$\frac{\partial f(x)}{\partial x}\Delta x \leq \Delta T \tag{14}$$

Thus, derived from Eq.(14), the maximum errors that $V_{\mathtt{be}}$, $\Delta V_{\mathtt{be}}$, A and α can respectively tolerate are

$$|V_{\mathtt{be}} - V_{\mathtt{be\_ideal}}| \leq \Delta T|\frac{\partial D_{\mathtt{out}}}{\partial V_{\mathtt{be}}}|^{-1} \approx \frac{V_{\mathtt{ref}}}{T}\Delta T \tag{15}$$

$$|\Delta V_{\mathtt{be}} - \Delta V_{\mathtt{be\_ideal}}| \leq \Delta T|\frac{\partial D_{\mathtt{out}}}{\partial \Delta V_{\mathtt{be}}}|^{-1} \approx \frac{V_{\mathtt{ref}}}{\alpha(A-T)}\Delta T \tag{16}$$

$$|\alpha - \alpha_{\mathtt{ideal}}| \leq \Delta T|\frac{\partial D_{\mathtt{out}}}{\partial \alpha}|^{-1} \approx \frac{A\alpha_{\mathtt{ideal}}}{T(A-T)}\Delta T \tag{17}$$

$$|A - A_{\mathtt{ideal}}| \leq \Delta T|\frac{\partial D_{\mathtt{out}}}{\partial A}|^{-1} \approx \frac{A_{\mathtt{ideal}}}{T}\Delta T \tag{18}$$

Where $T = AK$ denotes the absolute temperature. In general, to reach the accuracy of $\pm 0.5°\mathrm{C}$, the error ΔT in Eqs. (15)-(18) should be less than $0.05°\mathrm{C}$.Taking $V_{\mathtt{ref}} = 1.2\mathtt{V}, \alpha = 10, A = 600, T_{\mathtt{max}} = 85°\mathrm{C} = 358\mathtt{K}, T_{\mathtt{min}} = -25°\mathrm{C} = 248\mathtt{K}$, for simplicity, we adopts $T = 300\mathtt{K}$ in above equations, thus we should control $|V_{\mathtt{be}} - V_{\mathtt{be\_ideal}}| \leq 0.2\mathtt{mV}, |\Delta V_{\mathtt{be}} - \Delta V_{\mathtt{be\_ideal}}| \leq 0.02\mathtt{mV}, |\alpha - \alpha_{\mathtt{ideal}}|/\alpha_{\mathtt{ideal}} \leq 0.033\%$ and $|A - A_{\mathtt{ideal}}|/A_{\mathtt{ideal}} 0.017\%$. Here, $|A - A_{\mathtt{ideal}}|/A_{\mathtt{ideal}}$ depends on digital units, if we use 14bits, then we can reach the accuracy of 0.001. The precision of α depends on the precision of capacitance matching, if we use the common centroid matching technology, we can only reach the accuracy of 0.05, thus the introduction of dynamic element matching technology is necessary in our paper. The accuracy of both $V_{\mathtt{be}}$ and $\Delta V_{\mathtt{be}}$ should be controlled at the order of $\mu\mathtt{V}$, by using the offset cancellation technique, they can be reduced to the level of $\mu\mathtt{V}$ under the condition of 100dB op-amp DC gain. Meanwhile, the resistance in series on the bipolar transistor will also affect the value of $V_{\mathtt{be}}$, the resistance in series should be less than 20Ω in $10\mu\mathtt{A}$ bias current.

4. Proposed Error Elimination Scheme.

4.1. Elimination of the Resistance in Series.

In our paper, we eliminate the resistance in series by adopting multiple $V_{\mathtt{be}}$'s to obtain a $\Delta V_{\mathtt{be}}$ that is unrelated to the resistance in series. The detailed design is shown in Fig.3.

As shown in Fig.3, there are four cycles in the integrator to complete the generation of a parasitic resistance that is independent of $\Delta V_{\mathtt{be}}$. In the first three cycles, by controlling $\mathtt{S}_1, \mathtt{S}_2, \mathtt{S}_1'$ and $\mathtt{S}_2'$, we make the current through the transistor be $3I$ and I; while in the

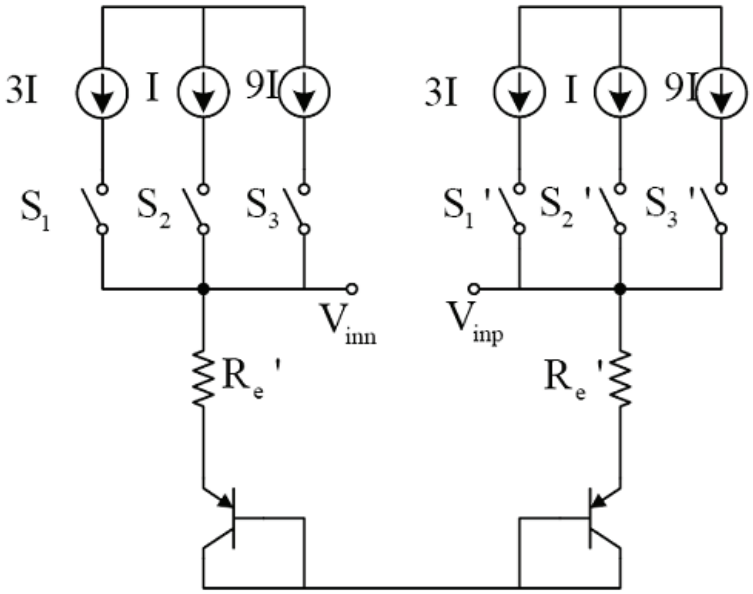

FIGURE 3. The elimination of the parasitic resistance in the transistor

fourth cycle, by controlling the $\mathtt{S}_1, \mathtt{S}_3, \mathtt{S}'_1, \mathtt{S}'_3$, we make the current through the transistor be $3I$ and $9I$. Thus, eventually $\Delta V_{\mathtt{be}}$ is generated as follows:

$$\Delta V_{\mathtt{be}} = 3[(V_T \ln \frac{3I}{I_S} + 3I \cdot R'_e) - (V_T \ln \frac{I}{I_S} + I \cdot R'_e)] + (V_T \ln \frac{3I}{I_S} + 3I \cdot R'_e) - (V_T \ln \frac{9I}{I_S} + 9I \cdot R'_e) = V_T \ln 9 \tag{19}$$

Since the generation of $\Delta V_{\mathtt{be}}$ needs four clock cycles, as compared to the general modulation cycle, more than three times transition time required. However, since we need 2^{14} cycles to complete a conversion, if we use such a parasitic resistance cancellation technique, we need a very long transition time. Thus, alternatively, we adopt another simple technique to reduce the effect of the resistance. That is, we reduce the current to $1\mu\mathtt{A}$ and increase the number of deregulation bits to eliminate the effect of parasitic resistance. In this way, we not only implement a low-power design, but also can reduce the difficulty of design.

4.2. **Matching of the Current Mirror.** In the circuit for $\Delta V_{\mathtt{be}}$ generation, the effects that affect the accuracy of $\Delta V_{\mathtt{be}}$ include not only the parasitic resistance, but also the area of the transistor emitter junction and the ratio of current mirror. Here, we ignore the impact of the area of the emitter junction, and only consider the precision reduction because of the current mirror mismatch. Suppose a current mirror with a ratio of n:1 is achieved by matching n+1 current mirror tubes, due to the presence of the mismatch, we have the current of each channel:

$$I_j = (1 + \delta_j)\overline{I} \tag{20}$$

Where $\overline{I}$ is the average output current of the current source, δ_j is the relative difference between the average current and the current of the j-th current mirror with

$$\sum_{j=1}^{n+1} \delta_j = 0 \tag{21}$$

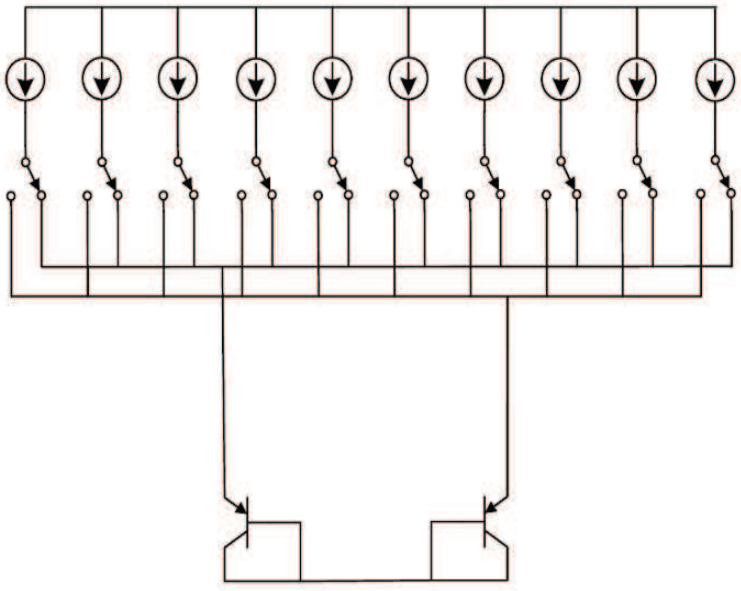

FIGURE 4. The dynamic element matching technology in the current mirror

If we use the j-th current mirror as the unit current source, then the ratio of current source can be expressed as:

$$n' = \frac{\sum_{i=1}^{n+1} I_i - I_j}{I_j} = \frac{(n+1)\overline{I} - (1+\delta_j)\overline{I}}{(1+\delta_j)\overline{I}} = n - (n+1)\frac{\delta_j}{1+\delta_j} \tag{22}$$

Then the mismatch of the ratio of the current mirror can be expressed as

$$\frac{\Delta n}{n} = \frac{n' - n}{n} \approx \frac{n+1}{n}\delta_j \tag{23}$$

Therefore, the $\Delta V_{\mathtt{be}}$ that is generated because of the mismatch of the current mirror can be expressed as:

$$\Delta V_{\mathtt{be}} = V_T \ln(n - \Delta n) = V_T \ln[n(1 - \frac{\Delta n}{n})] \approx V_T \ln n - V_T \frac{n+1}{n}\delta_j \tag{24}$$

Since V_T is equal to 26mV at room temperature, if the matching accuracy of the current mirror is assumed to be 1%, then it will bring an error of $260\mu\mathtt{V}$ to $\Delta V_{\mathtt{be}}$. However, from Section 3, we know that the required error of $\Delta V_{\mathtt{be}}$ should be less than $20\mu\mathtt{V}$, thus the above accuracy does not satisfy our requirements. Even if we can use better layout design to obtain a matching accuracy 0.1%, the generated error is still as large as $26\mu\mathtt{V}$, which is still unacceptable. Therefore, it is necessary to introduce the dynamic element matching technology (DEM) to the current mirror tube.The so-called dynamic element matching technique [11] is to view the generated current in each current mirror tube as a unit current source in turn and inject it into the transistors. Assume there are 10 unit current sources, as shown in Fig. 4.

When we need to generate $\Delta V_{\mathtt{be}}$, each current source as shown in Fig. 4 is viewed as the unit current source in turn. The generation of a group of control signals is equivalent to a shift register, and because of the computational requirement of the integrator, this group requires a clock signal with an XOR-treatment to obtain a final control signal. Similar operation can be performed on the circuit that generates $V_{\mathtt{be}}$.

Such operations are performed in turn, which is equivalent to taking an average value over ΔV_{be}. Without ignoring the quadratic term, we can rewrite Eq.(24) as

$$\Delta V_{\mathsf{be}} \approx V_T \ln n - V_T \frac{\Delta n}{n} \approx V_T \ln n - V_T \frac{n+1}{n}(\delta_j - \delta_j^2) \tag{25}$$

After the averaging process, according to Eq. (21), we have:

$$\overline{\Delta V_{\mathsf{be}}} \approx \frac{1}{n+1}\sum_{j=1}^{n+1}[V_T \ln n - V_T \frac{n+1}{n}(\delta_j - \delta_j^2)] = V_T[\ln n + \frac{1}{n}\sum_{j=1}^{n+1}\delta_j^2] \tag{26}$$

From Eq. (26) we can see that, if the matching precision of current source is only 1%, then eventually the deviation of ΔV_{be} will be only $2.6\mu\mathtt{V}$, which has already met the requirement of our system.

4.3. **Matching of the capacitance.** Finally, we need to consider the precision of capacitor matching, after all, even for a best layout technique, the capacitance accuracy is difficult to reach 0.1%, while it can be seen from Section 3, the accuracy of the matching capacitor must reach 0.03%. Thus, obviously we also need to use the dynamic element matching technique to improve the matching degree of the capacitor.

Fig. 5 shows the schematic diagram of our dynamic element matching technique for capacitors. From Eq. (10), we can see that, obtaining the linearity of K is to some degree dependent of the accuracy of α, which is obtained by the switch group $S_1, S_2, ..., S_m$. When the modulator is needed to perform the Δ operation on ΔV_{be}, all switches $S_1, S_2, ..., S_m$ are on, the stored charge is

$$Q = \sum_{j=1}^{m}[C_j \cdot \Delta V_{\mathsf{be}}] \tag{27}$$

so we subtract one pulse with Q/C_i from the integrator. When the modulator is needed to perform the operation on Vbe, the switches $S_1, S_2, ..., S_m$ work in turn with the stored charge $C_j \Delta V_{\mathsf{be}}$, so we add a pulse with $C_j \Delta V_{\mathsf{be}}/C_i$ to the integrator, thus we have

$$\alpha = \frac{\sum_{j=1}^{m} C_j}{C_j} \tag{28}$$

Similar to the analysis of dynamic element matching technology for the current source, we assume that each capacitor has following capacitance:

$$C_j = (1+\delta_j)\overline{C} \tag{29}$$

After dynamic element matching, we have

$$\alpha' = \frac{1}{\alpha}\sum_{p=1}^{\alpha}[\frac{\sum_{j=1}^{\alpha} C_j}{C_p}] = \frac{1}{\alpha}\sum_{p=1}^{\alpha}[\frac{\alpha + \sum_{j=1}^{\alpha}\delta_j}{1+\delta_p}] = \sum_{p=1}^{\alpha}\frac{1}{1+\delta_p} \approx \alpha + \sum_{p=1}^{\alpha}\frac{\delta_p^2}{2} \tag{30}$$

Thus, the final mismatch can be dropped to the level of δ^2, then with the layout matching condition of 1% we can reach the matching accuracy of 0.01%, which has met our requirement.

5. **Simulation Results.** To demonstrate the effectiveness of the proposed scheme, Fig.6 shows three timing simulation maps for $-25°$C, 25°C and 85°C respectively. We can obviously see that, under the condition of low temperatures, ΔV_{be} is significantly reduced, and the number of Δ operations performed on modulators increases, and the output data '1' is with a relatively small proportion. On the contrary, under the condition of high temperatures, the number of operations performed on modulators increases, the

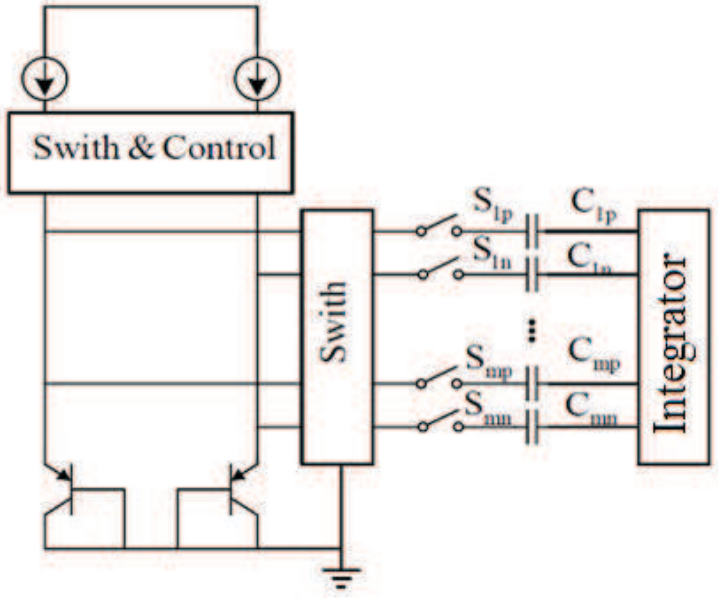

FIGURE 5. The dynamic element matching technology for capacitors

TABLE 1. Simulation results of the temperature sensor

Temperature(°C)	**Digital output[14:4]**
−25	0001010110
−5	0001110111
15	0010011100
35	0010111101
55	0011011011
75	0011111011

output data '1' is with an increasing proportion.The simulation digital output for several temperatures is shown in Table 1.

6. **Conclusion.** In this paper, several techniques are proposed to reduce the error for a fully digital integrated temperature sensor with a 14bit $\Sigma - \Delta$ ADC to achieve the accuracy within $-25 \sim 85°\text{C} \pm 1°\text{C}$ temperature range. These techniques can be applied to other systems[12, 13, 14]. Firstly, we analyze the temperature characteristic curve of the transistor, and summarize the non-ideal characteristics for actual devices. Then, we propose to adopt V_{be} and ΔV_{be} of the triode as temperature sensing devices, and analyze the effect of various noises and temperature mismatch on the ultimate accuracy. We adopt the dynamic element matching technology to improve the matching degree of the circuit. The simulation results demonstrate the effectiveness of the proposed techniques.

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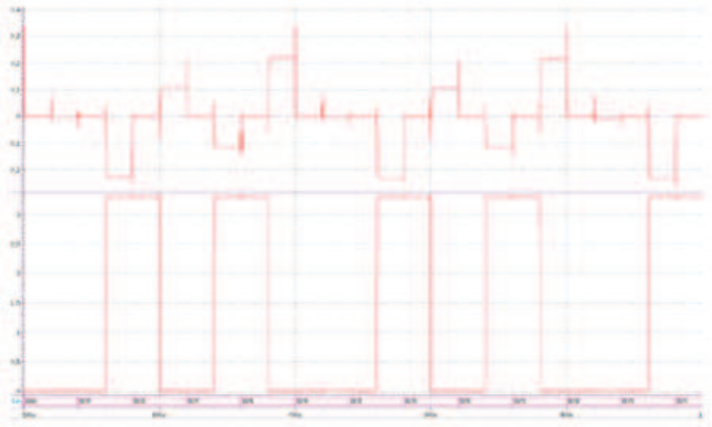
(a) Simulation result of the temperature sensor under −25°C

(b) Simulation result of the temperature sensor under 25°C



(c) Simulation result of the temperature sensor under 85°C

FIGURE 6. Simulation results of the temperature sensor

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