Baseband TIA Design Using Inversion Coefficient MOSFET Model in CMOS 28nm

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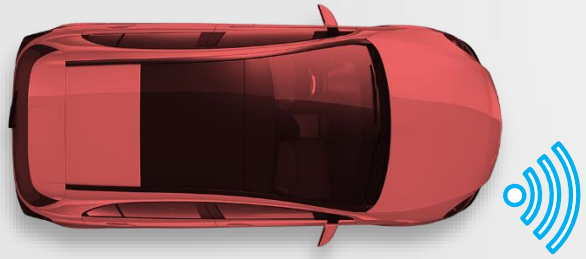
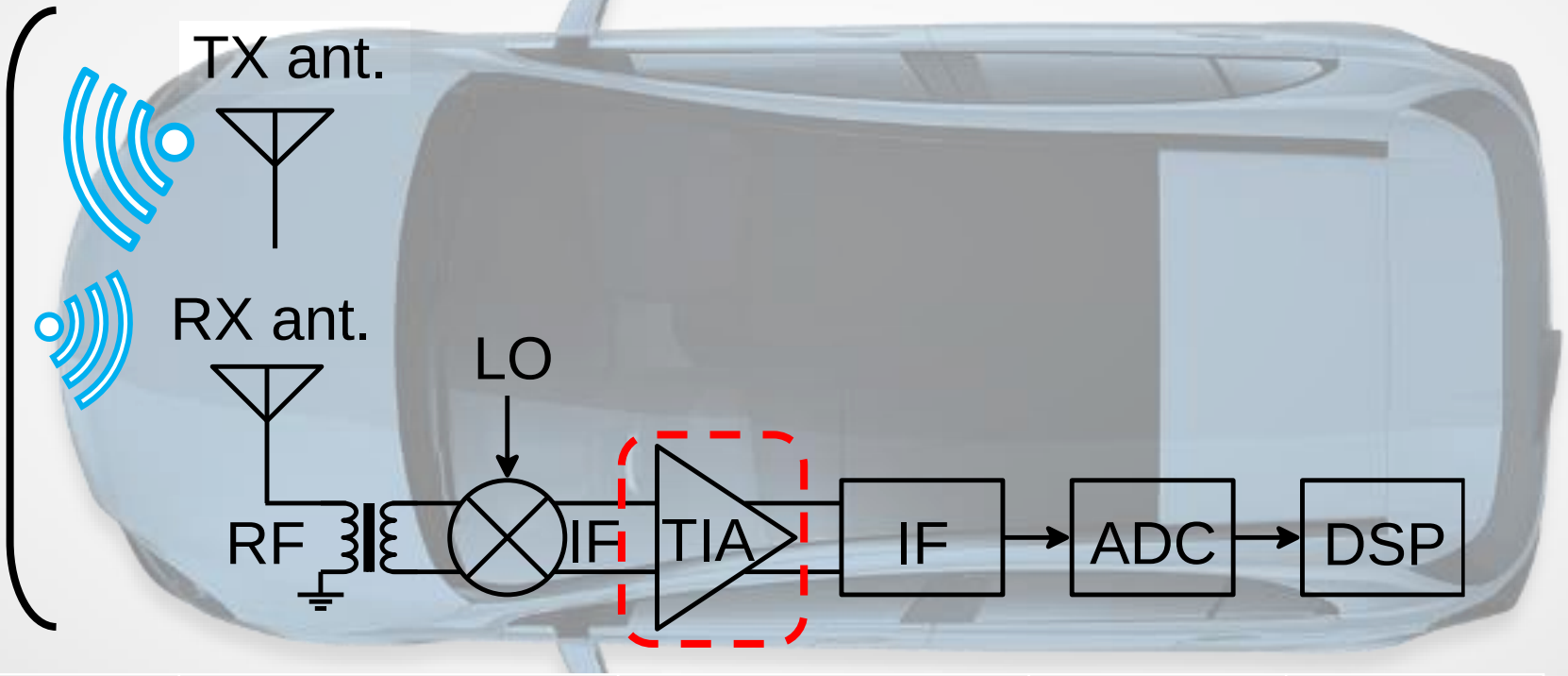
Outline

Radar Receiver Context

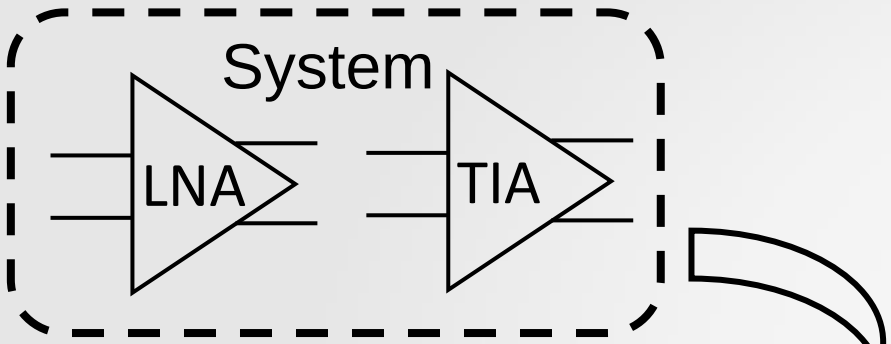
- Challenges of the radar receiver :



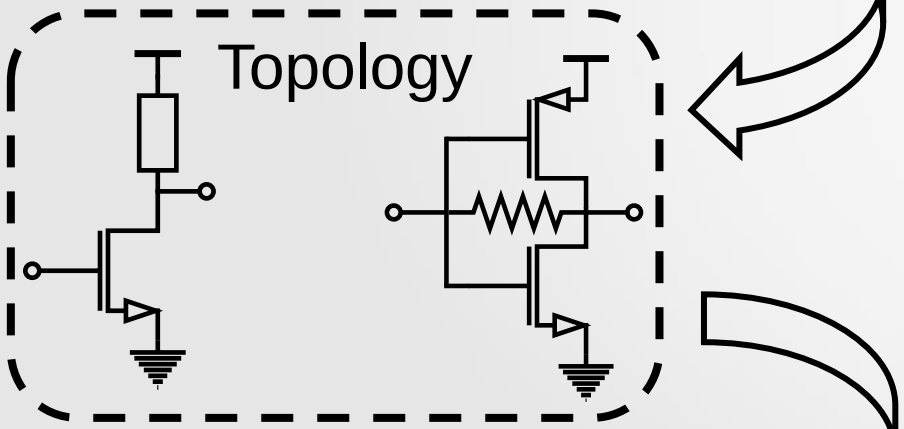


Transimpedance Gain	Bandwidth	Input impedance	Input ref. noise	ICP1	I_{DC}
1,5 kΩ	50 MHz	< 100 Ω	< $1e^{-22}$ A^2/Hz	> 0,5 mA	10 mA

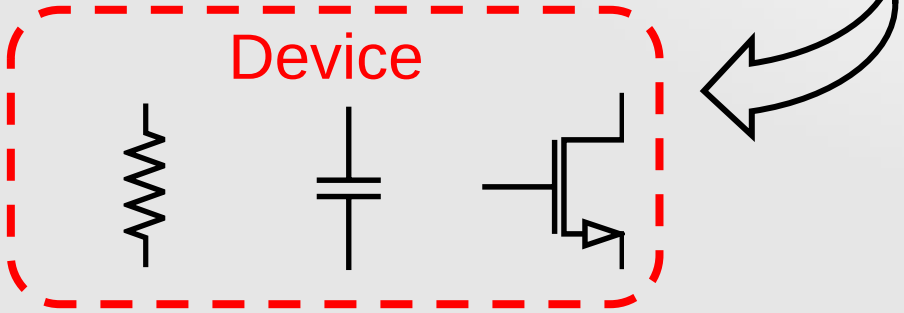
Design Method Strategy



Specs.



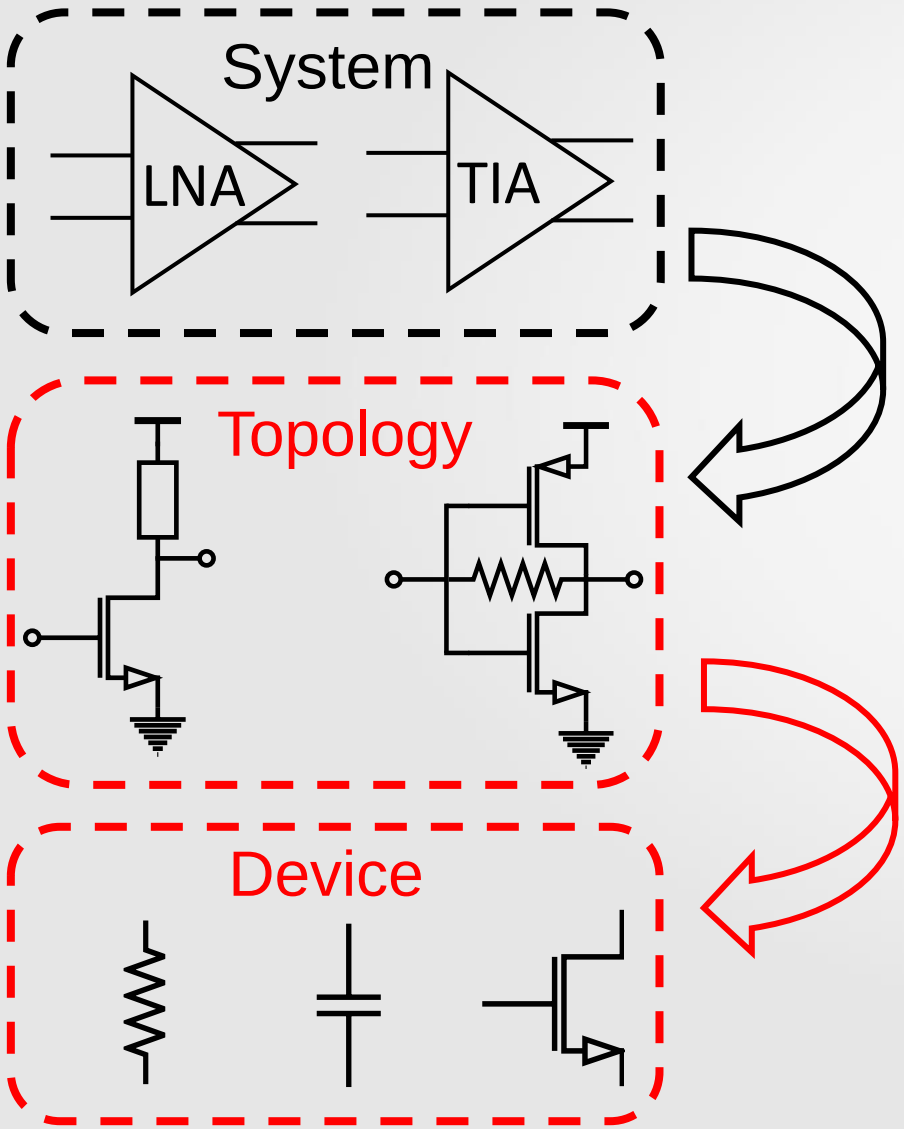
Circuit analysis



METHOD

Technology Extraction

Design Method Strategy



Specs.

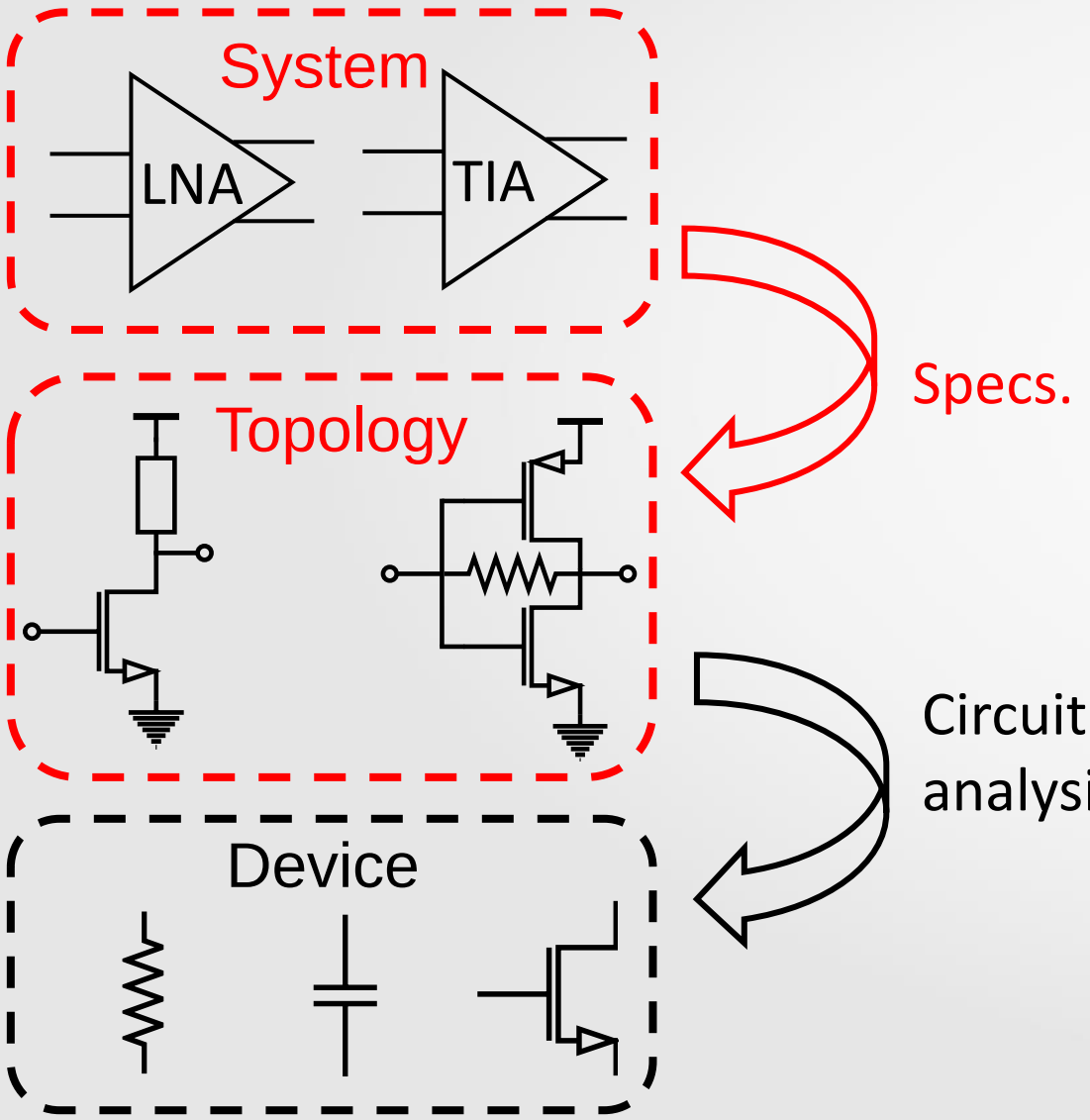
Circuit analysis

METHOD

Technology Extraction

Circuit analysis

Design Method Strategy



Specs.

Circuit analysis

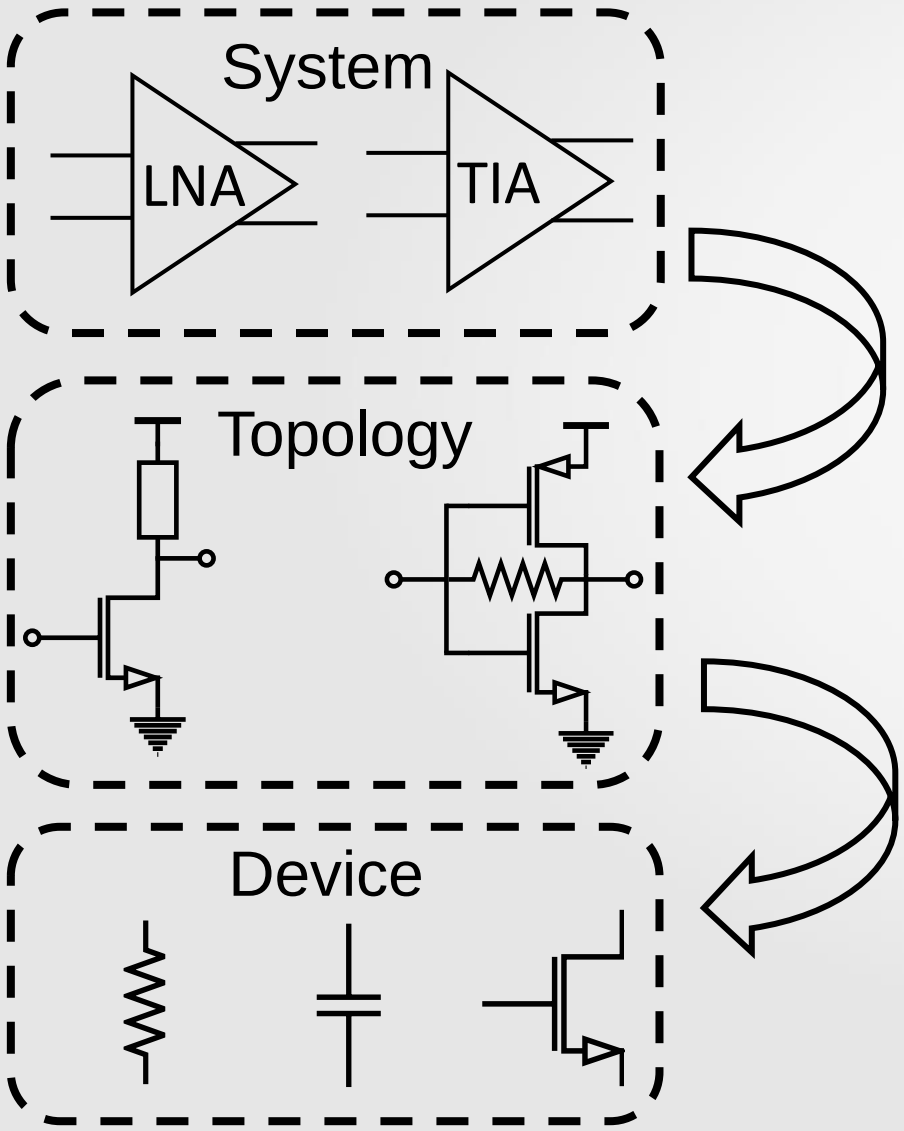
METHOD

Technology Extraction

Circuit analysis

Design space

Design Method Strategy



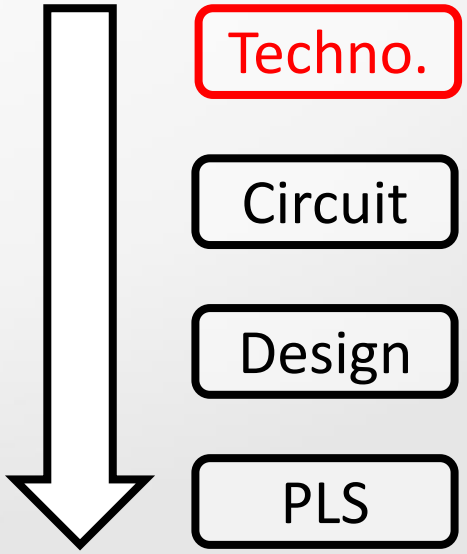
Specs.

Circuit analysis

METHOD

- Technology Extraction
- Circuit analysis
- Design space
- PLS

Outline



Charge based model

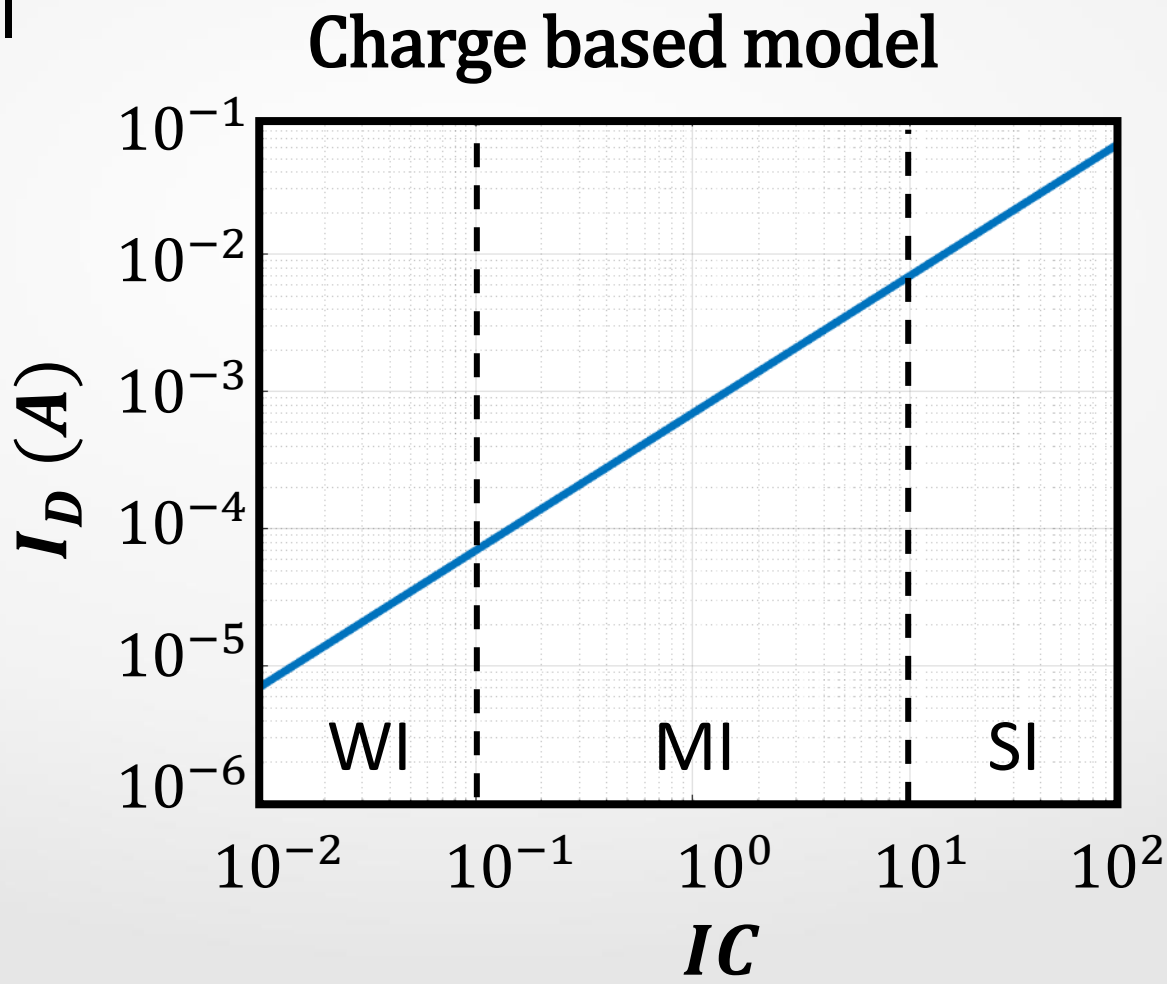
- Inversion Coefficient (IC) = measure of the inversion level in the channel

$$I_D = IC.I_{spec} = IC \cdot I_{spec\_sq} \cdot \frac{W}{L}$$

  - Bias condition
  - Technology
  - Transistor size

- With : $I_{spec\_sq} = 2n\mu_n C_{ox} U_T^2$

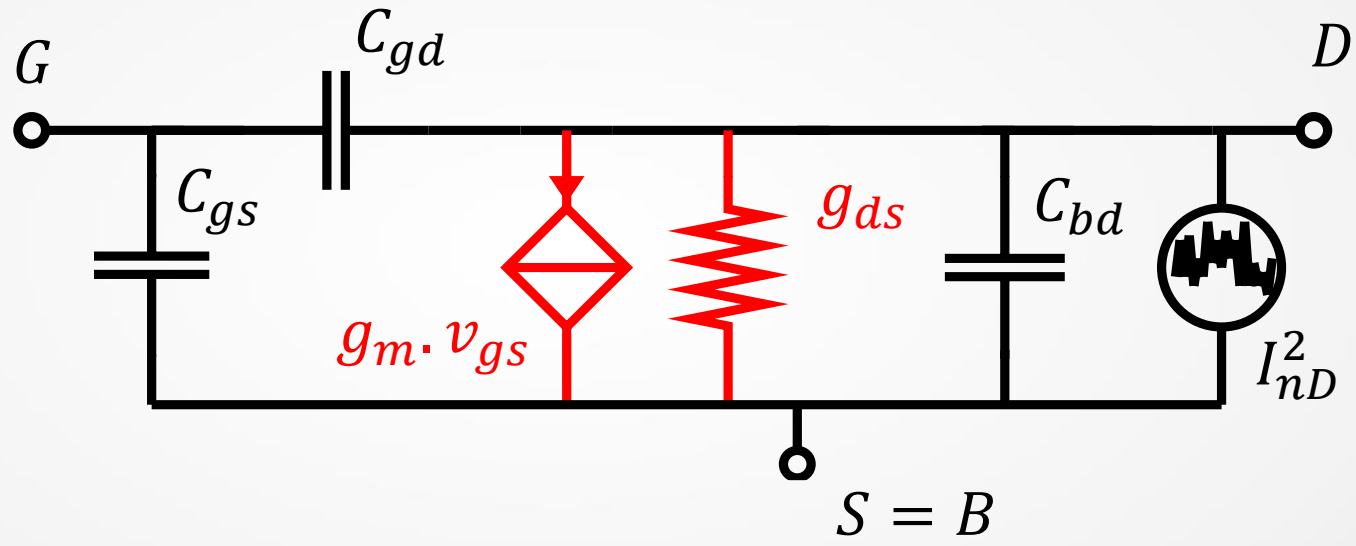
$$U_T = \mathrm{kT/q}$$



Small Signal Model

- $g_m(IC, W, L, techno)$
- $g_{ds}(IC, W, L, techno)$

} Active



Technological parameters (extracted once)		
Active		
I_{spec_sq}, λ_c n, σ_d		

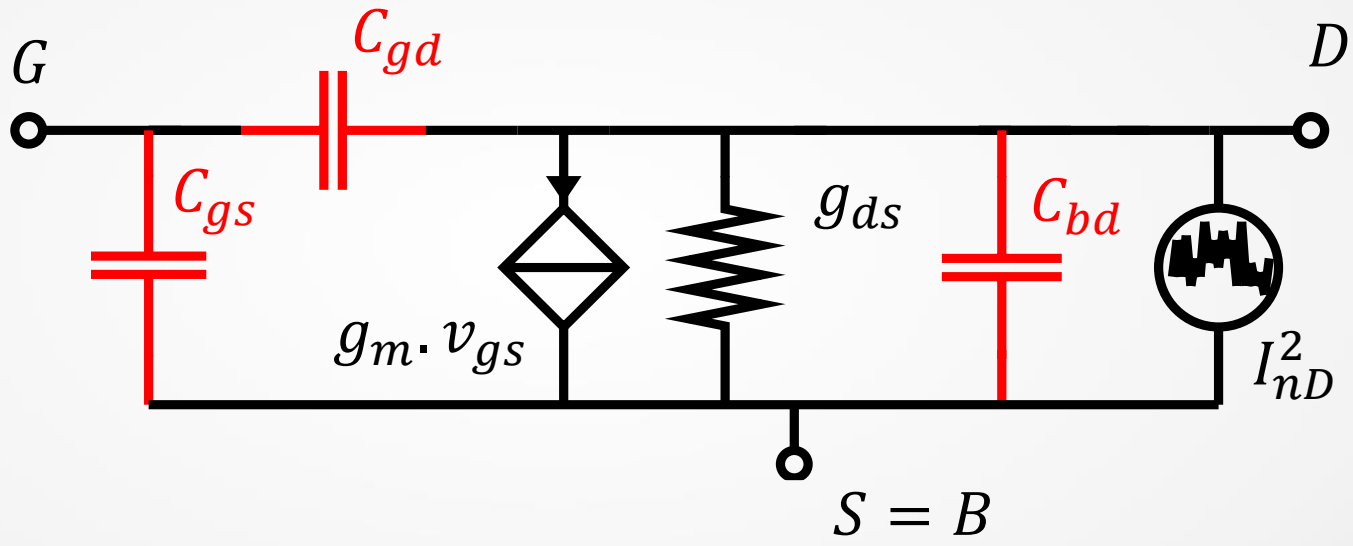
Small Signal Model

- $g_m(IC, W, L, techno)$
- $g_{ds}(IC, W, L, techno)$

} Active

- $C_{gd}(W, L, techno)$
- $C_{gs}(W, L, techno)$
- $C_{bd}(W, L, techno)$

} Passive



Technological parameters (extracted once)		
	Passive	
	$C_{(gs+gb)_{sq}}, C_{(gs+gb)_l}$ $C_{gd_l}, C_{gd_{sq}}, C_{bd_l}$	

Small Signal Model

- $g_m(IC, W, L, techno)$
- $g_{ds}(IC, W, L, techno)$

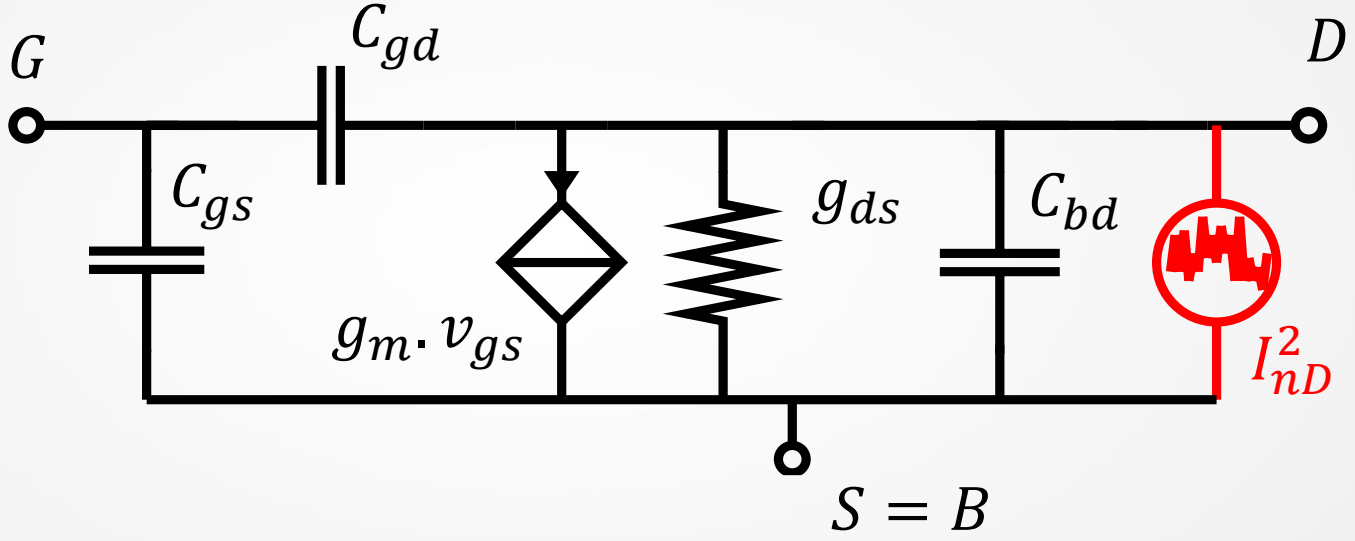
} Active

- $C_{gd}(W, L, techno)$
- $C_{gs}(W, L, techno)$
- $C_{bd}(W, L, techno)$

} Passive

- $i^2_{nD}(g_m, techno)$

} Noise



Technological parameters (extracted once)		
		Noise
		α_{γ_n} (short channel) γ_n (long channel)

Small Signal Model

- $g_m(IC, W, L, techno)$
- $g_{ds}(IC, W, L, techno)$

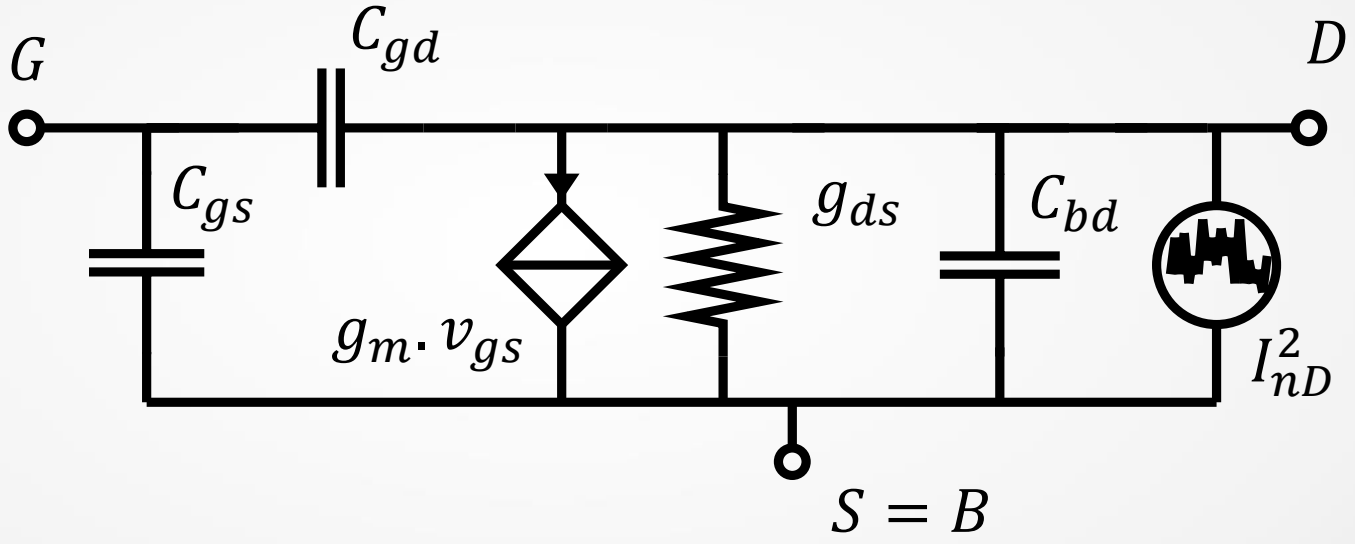
} Active

- $C_{gd}(W, L, techno)$
- $C_{gs}(W, L, techno)$
- $C_{bd}(W, L, techno)$

} Passive

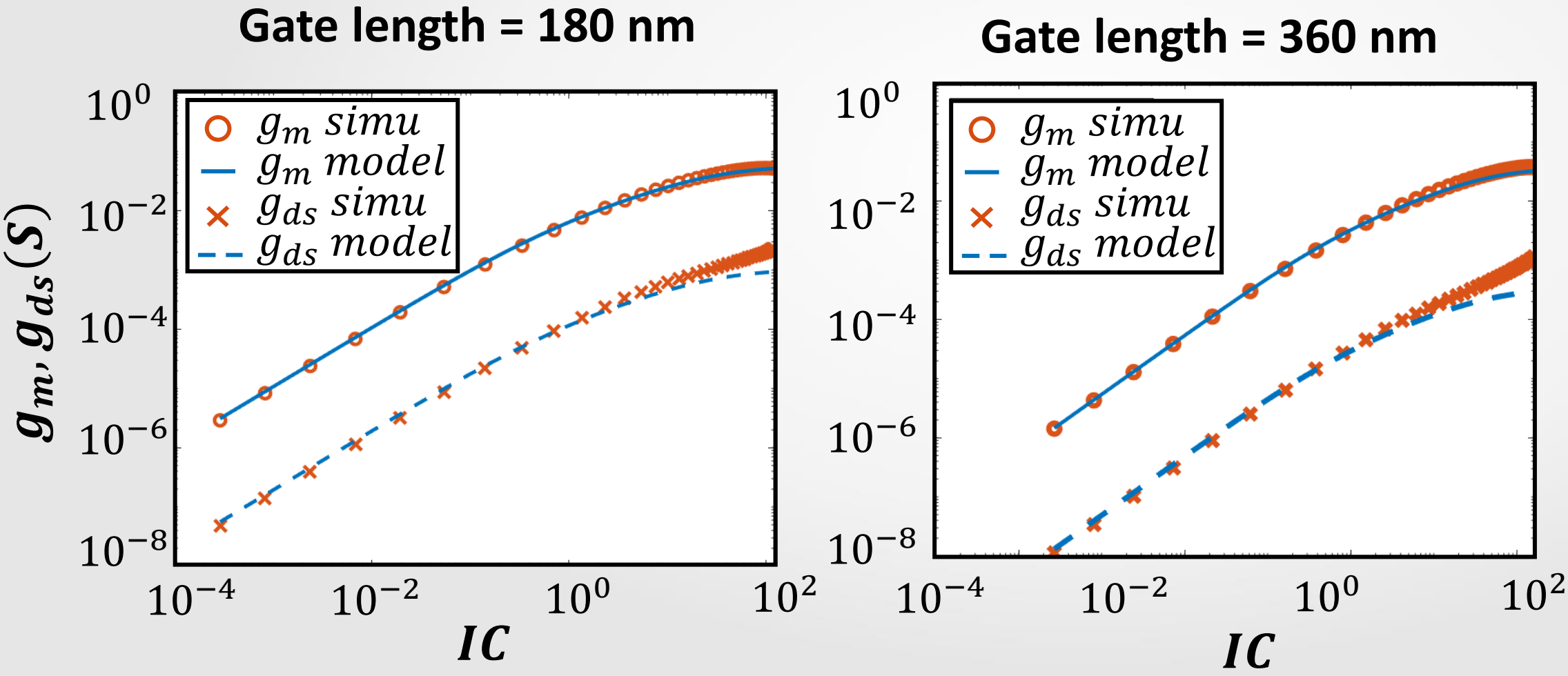
- $i_{nD}^2(g_m, techno)$

} Noise

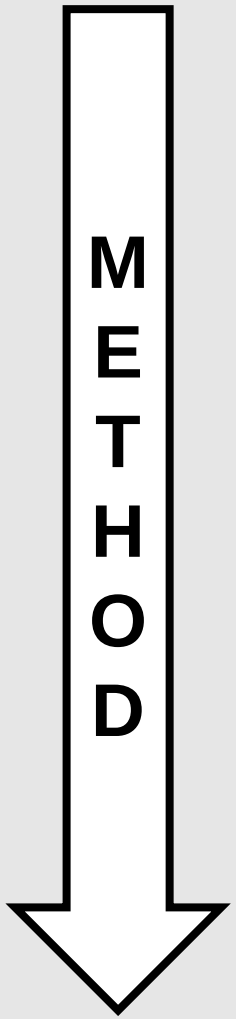


Technological parameters (extracted once)				Design parameters
Active	**Passive**	**Noise**	⇨	**W, L** (transistor size) **IC** (bias condition) Only 3 !!
I_{spec_sq}, λ_c n, σ_d	$C_{(gs+gb)_{sq}}, C_{(gs+gb)_l}$ $C_{gd_l}, C_{gd_{sq}}, C_{bd_l}$	α_{γ_n} (short channel) γ_n (long channel)		

Model Validation



Design Method



Technology Extraction

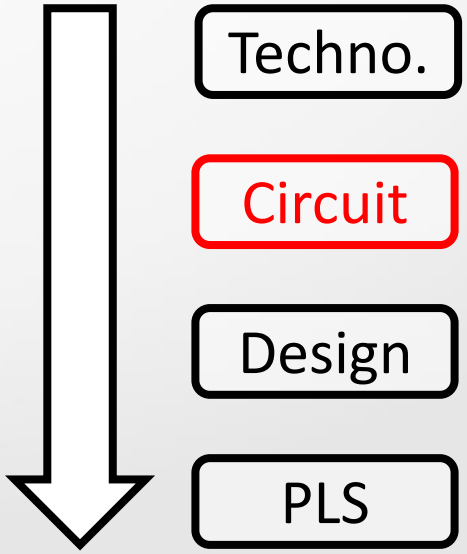
- $I_{spec\_sq}, \lambda_c, C_{gd_l}, C_{(gs+gb)_{sq}}, I_{nD}^2$ …

Circuit analysis

Design space

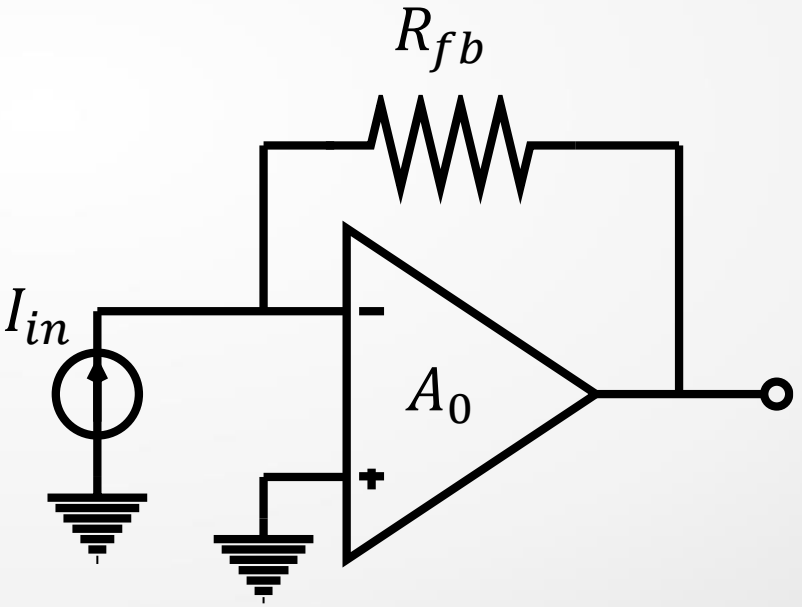
PLS

Outline



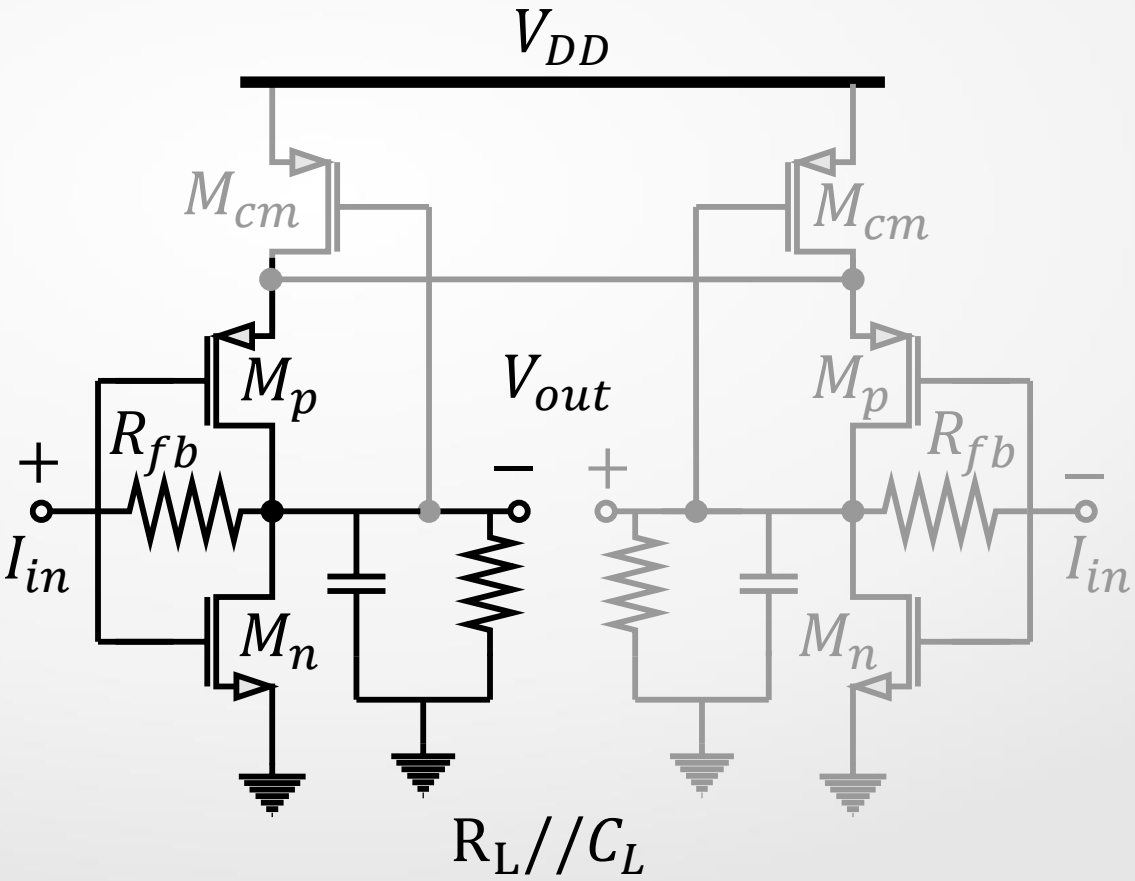
TIA Topology

- General TIA structure : Shunt-shunt amplifier



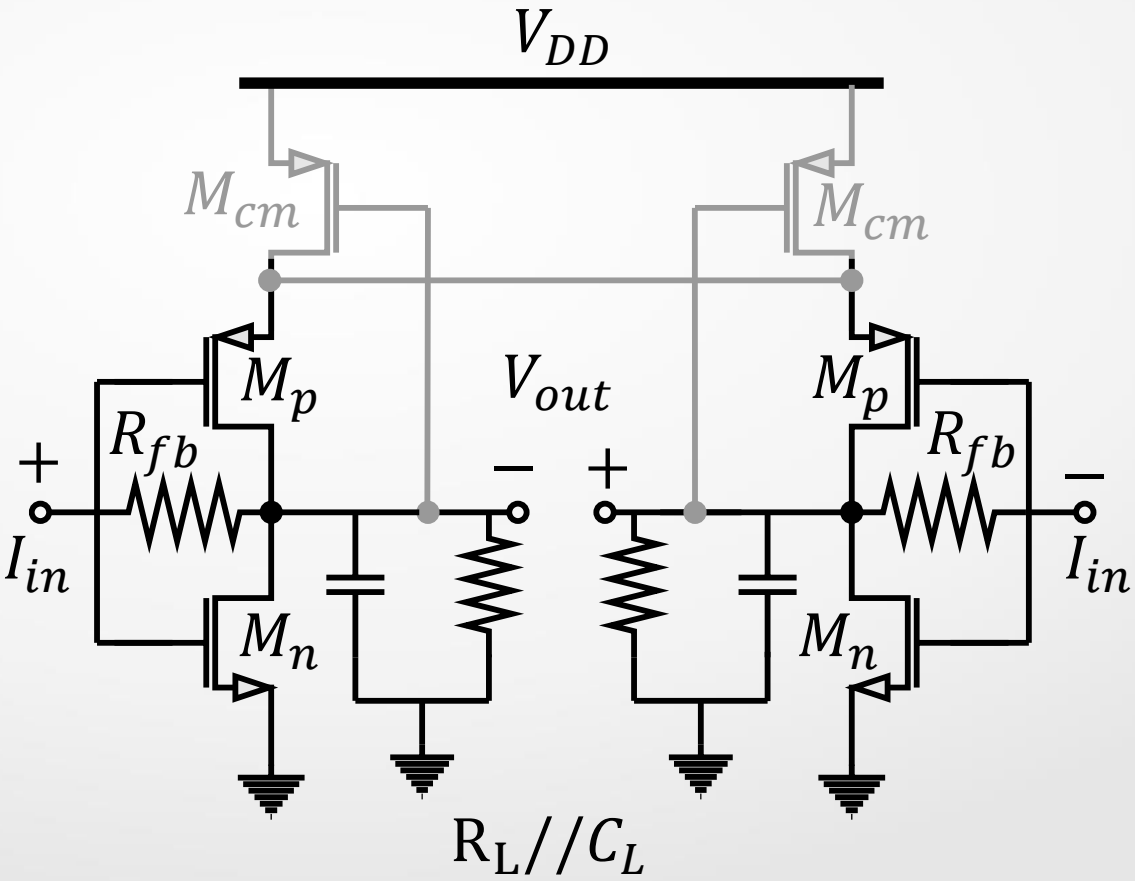
TIA Topology

- General TIA structure：Shunt-shunt amplifier
  - Current reuse with Rfb



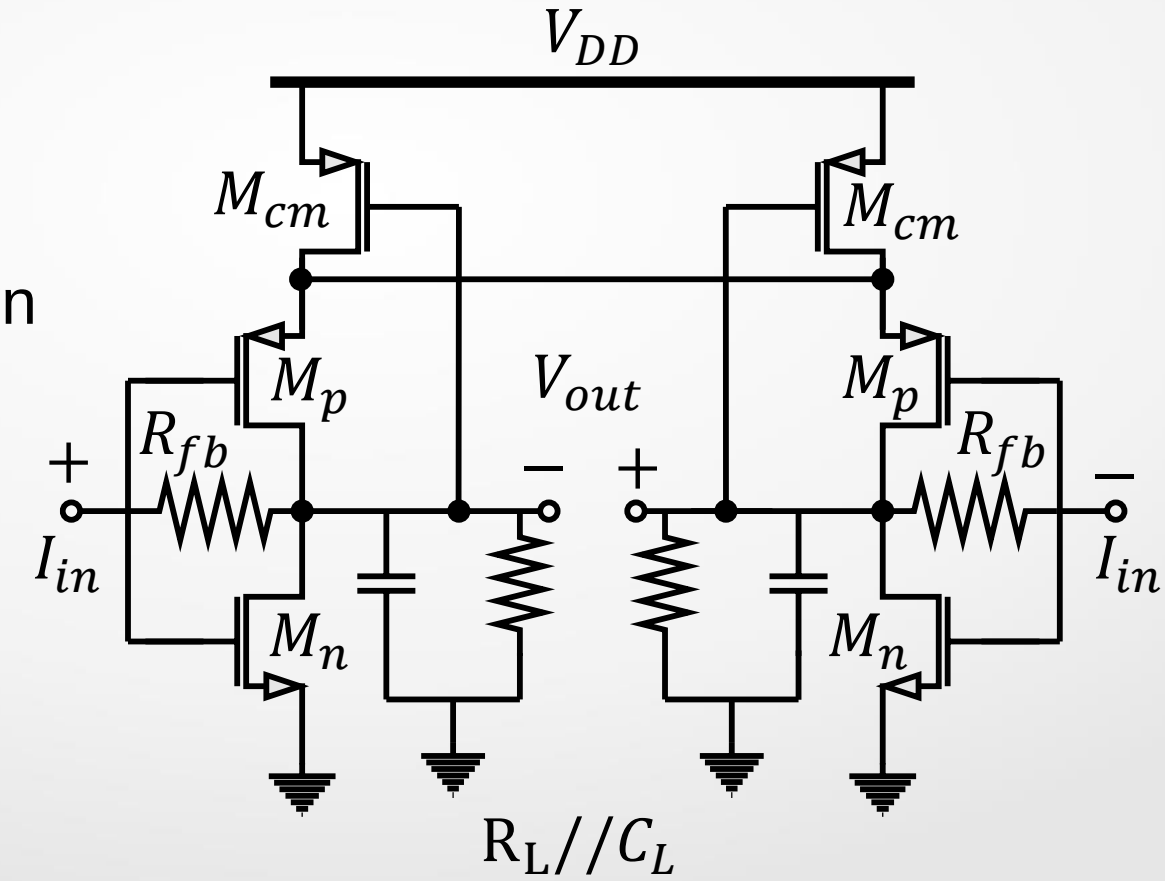
TIA Topology

- General TIA structure : Shunt-shunt amplifier
  - Current reuse with Rfb
  - Differential



TIA Topology

- General TIA structure : Shunt-shunt amplifier
  - Current reuse with Rfb
  - Differential
  - Common mode feedback compensation

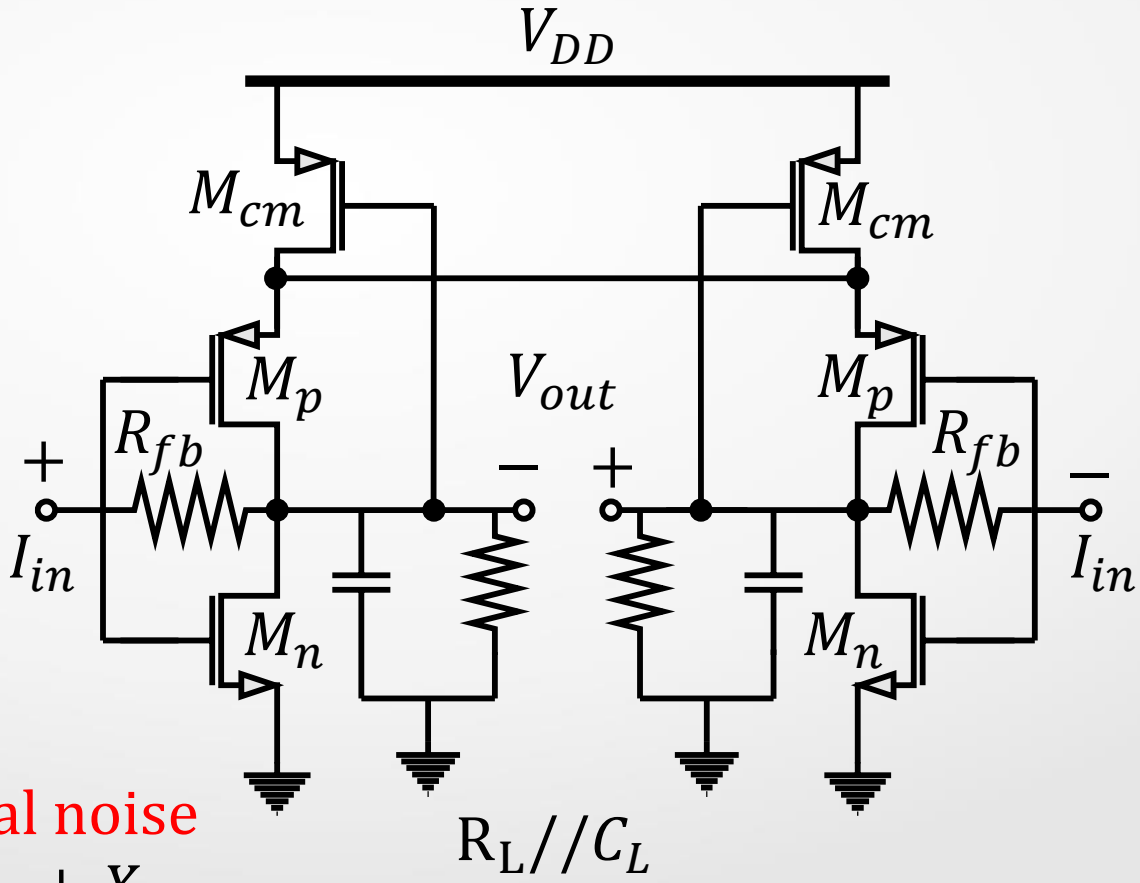


TIA Circuit Analysis

- $A_0 = g_{m,eq}.Z_{out}$ $\quad A_0 \gg 1$
- $Z_{out} = \frac{1}{g_{ds,eq}+j\omega(C_{bd,eq}+C_L)+\frac{1}{R_L}+\frac{1}{R_{Fb}}}$
- $R_{IN} = R_{Fb}.\frac{1}{1+A_0}$ $\quad R_{IN} \ll R_{Fb}$
- $R_T = -(R_{Fb}//j\omega C_{gd,eq})\frac{A_0}{1+A_0}$ $\quad R_T \approx R_{Fb}$
- $i_{n,in}^2 = \frac{v_{n,out}^2}{A_0^2.Z_{IN}^2} = \frac{4kT\left(\gamma_n g_{m,eq}+\frac{1}{R_{Fb}}\right).Z_{out}^2}{A_0^2.Z_{IN}^2}$

Few % of total noise

$$X_{eq} = X_n + X_p$$



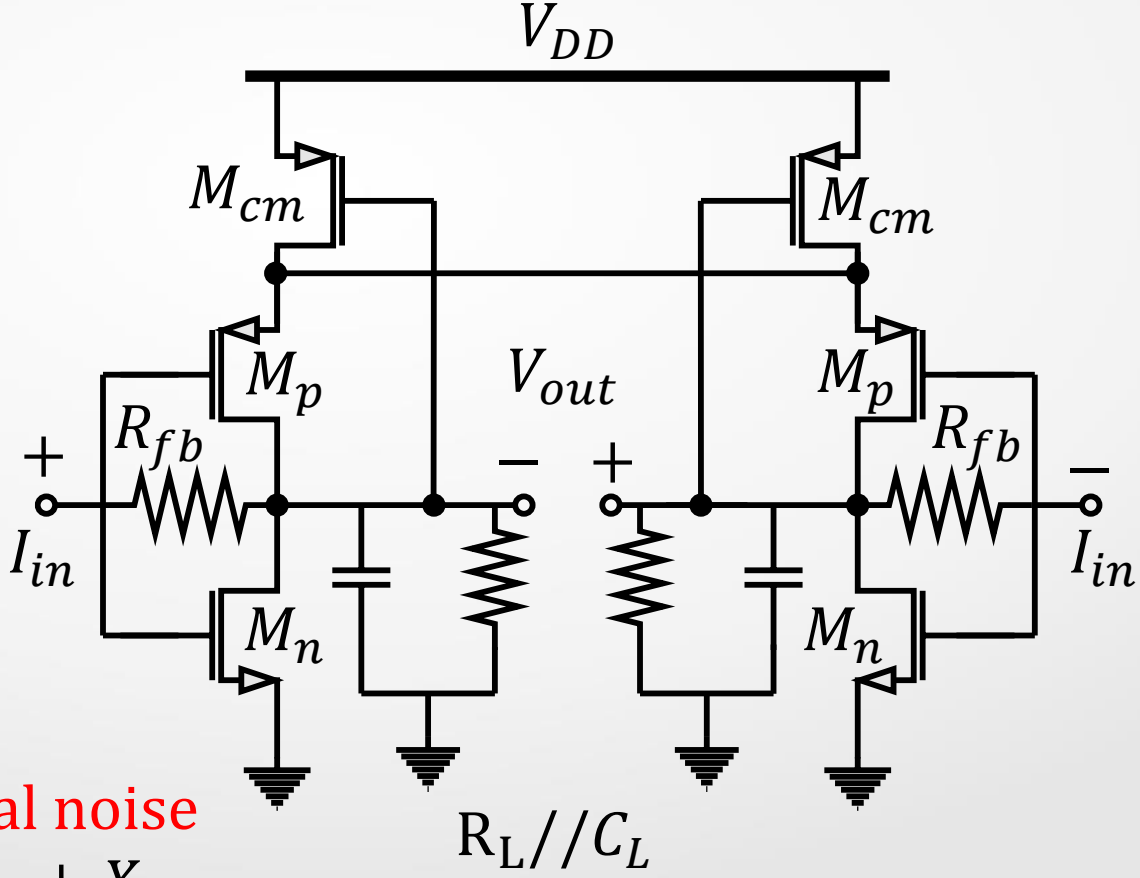
TIA Circuit Analysis

-
-
-
-
-

$g_{m_n}(IC_n, L_n, W_n), g_{m_p}(IC_p, L_p, W_p)$ ...

Additionnal circuit analysis

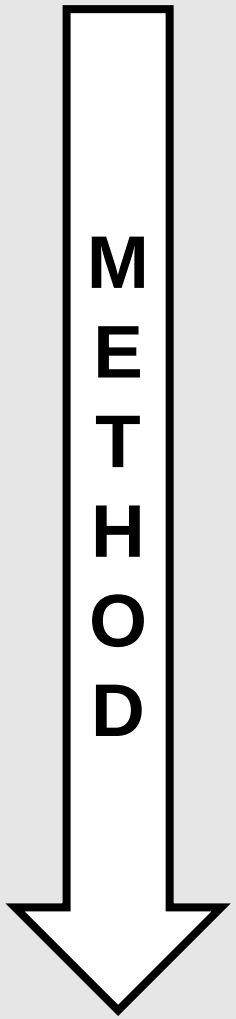
Only 3 design variables :
IC_n, L_n, W_n



tal noise

$X_{eq} = X_n + X_p$

Design Method



Technology Extraction

- $I_{spec\_sq}, \lambda_c, C_{gd_l}, C_{(gs+gb)_{sq}}, I_{nD}^2$ …

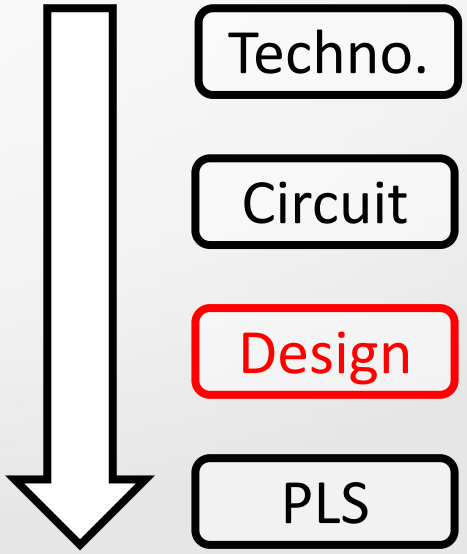
Circuit analysis

- $A_0(IC_n, L_n, \dots), R_T\ (IC_n, L_n, \dots), \dots$

Design space

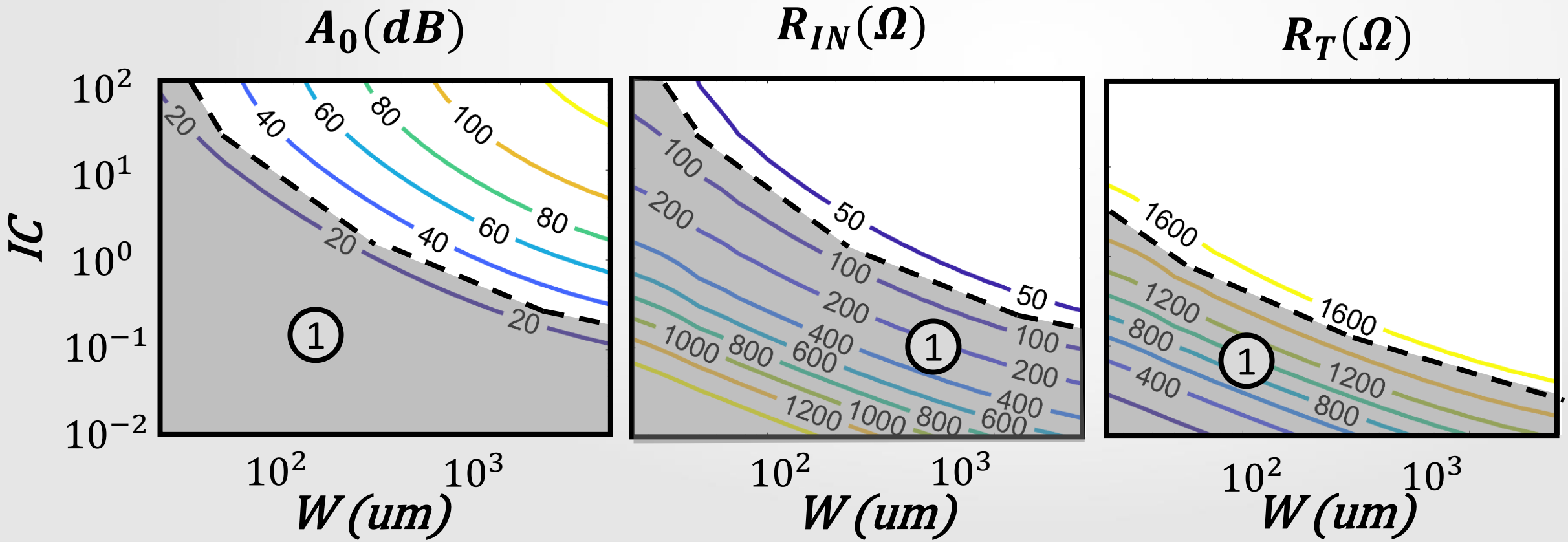
PLS

Outline



Exploring the Design Space

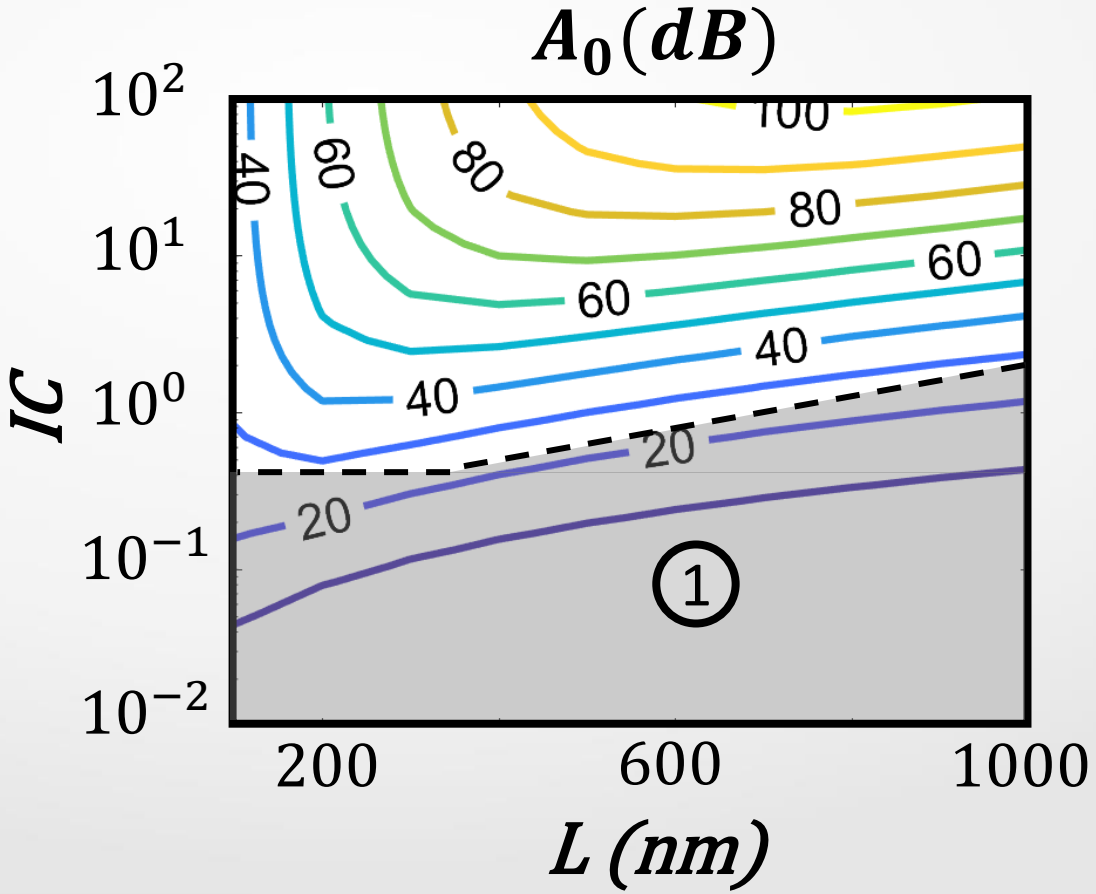
- Simulated characteristics vs IC and W:
  - ① Specs on R_{IN} ($< 100\ \Omega$) and R_T ($> 1{,}5\ k\Omega$): ⇨ $A_0 > 25\ dB$



Exploring the Design Space

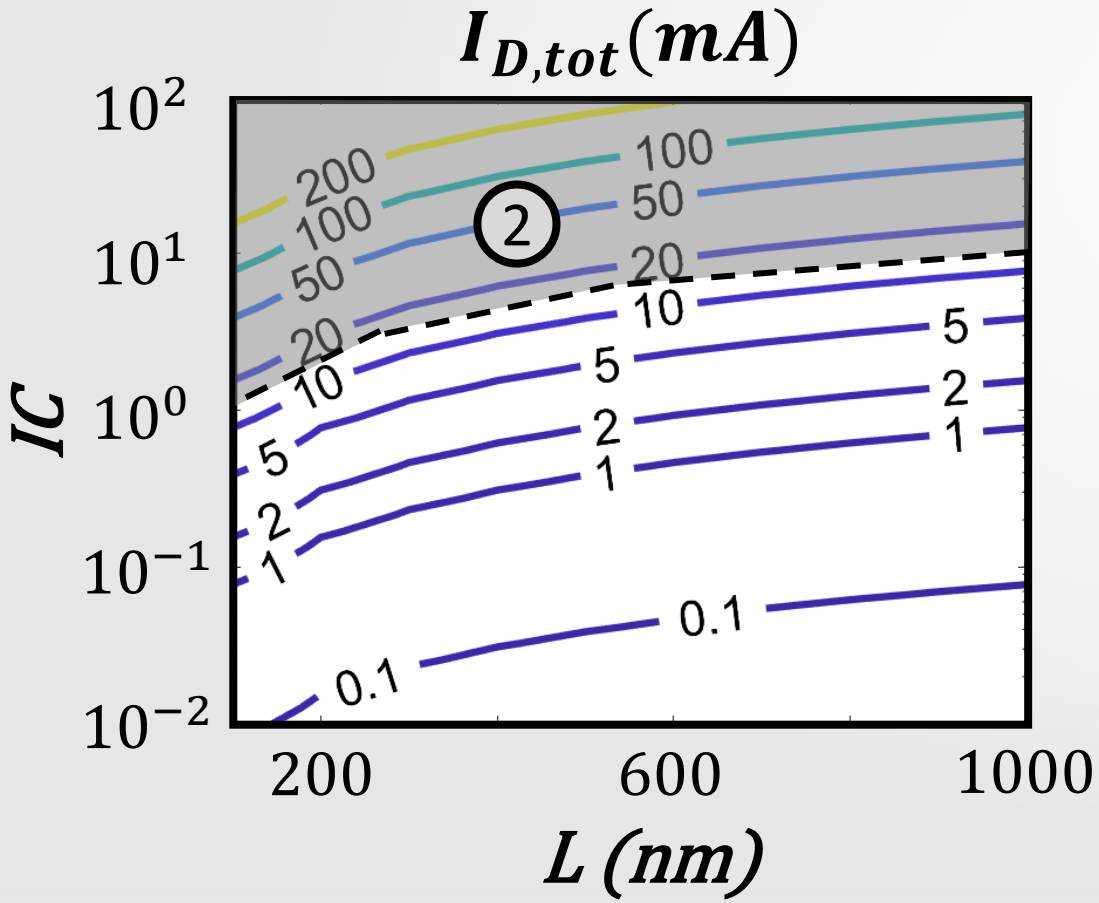
- Voltage gain vs IC and L :

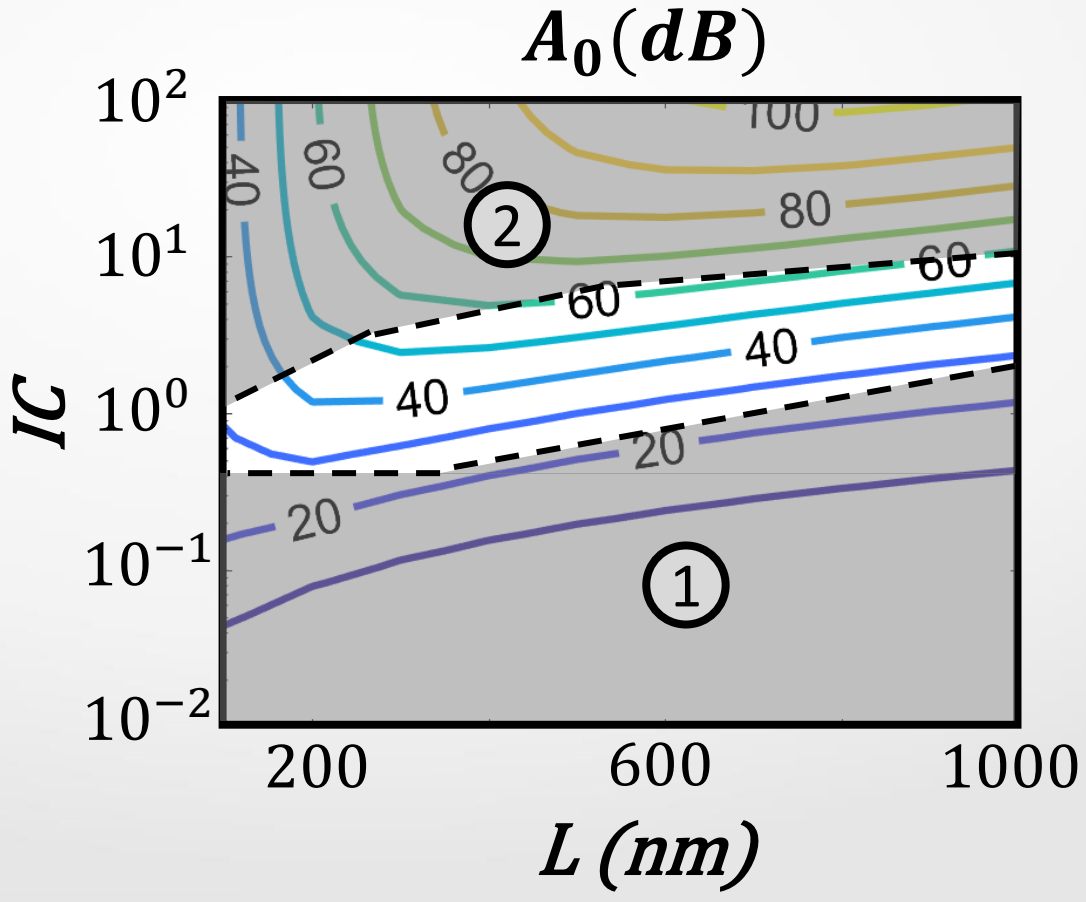
- A_0 trade-offs :
  ① Target value of min. 25 dB.



Exploring the Design Space

- Voltage gain vs IC and L :
  - ② Limit IC to avoid excessive current consumption.

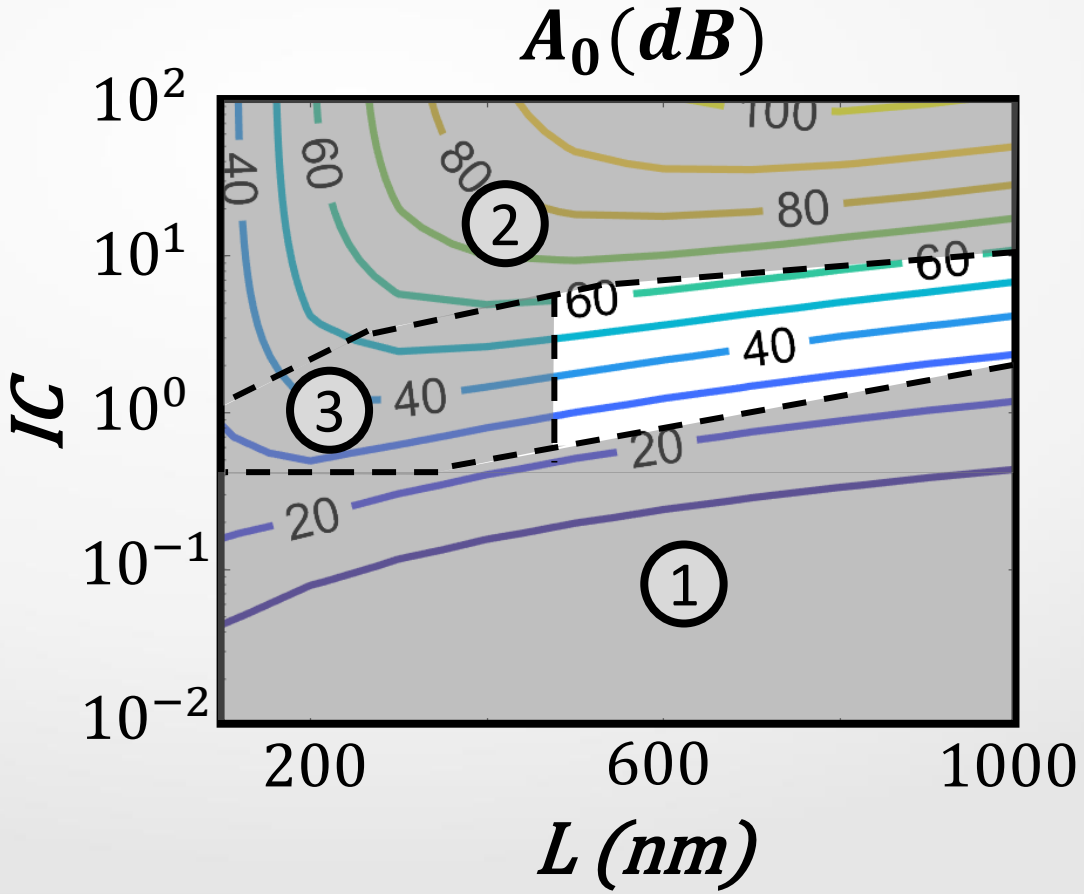




Exploring the Design Space

- Voltage gain vs IC and L :

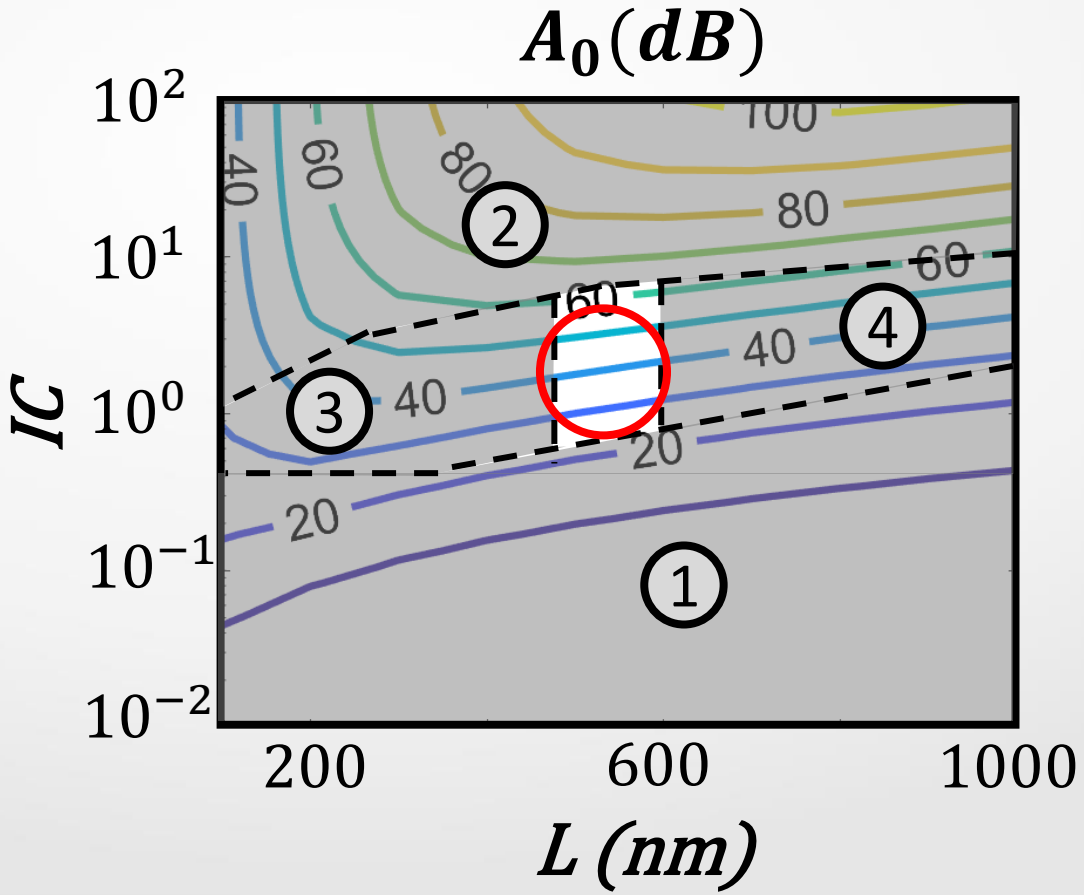
- A_0 trade-off :
  1. Target value of min. 25 dB.
  2. Limit IC to avoid excessive current consumption.
  3. L high enough to avoid excessive flicker noise.



Exploring the Design Space

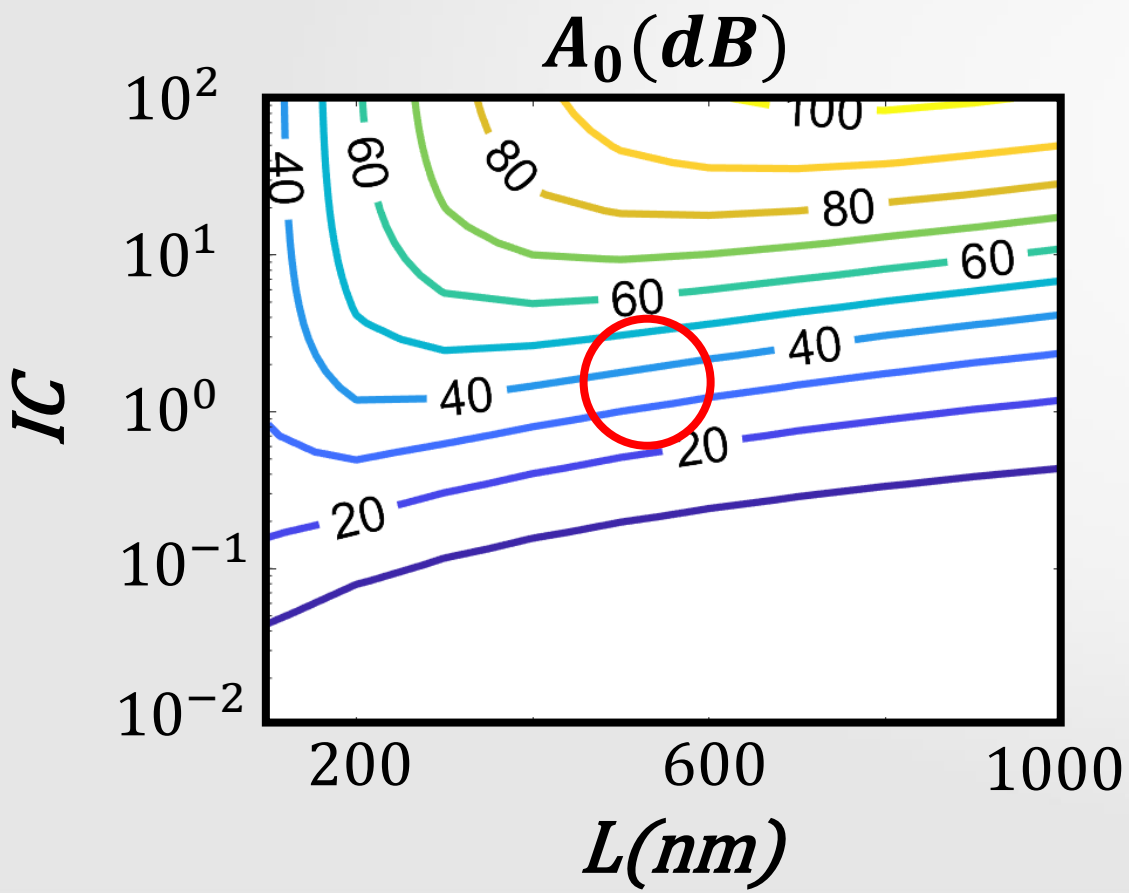
- Voltage gain vs IC and L :

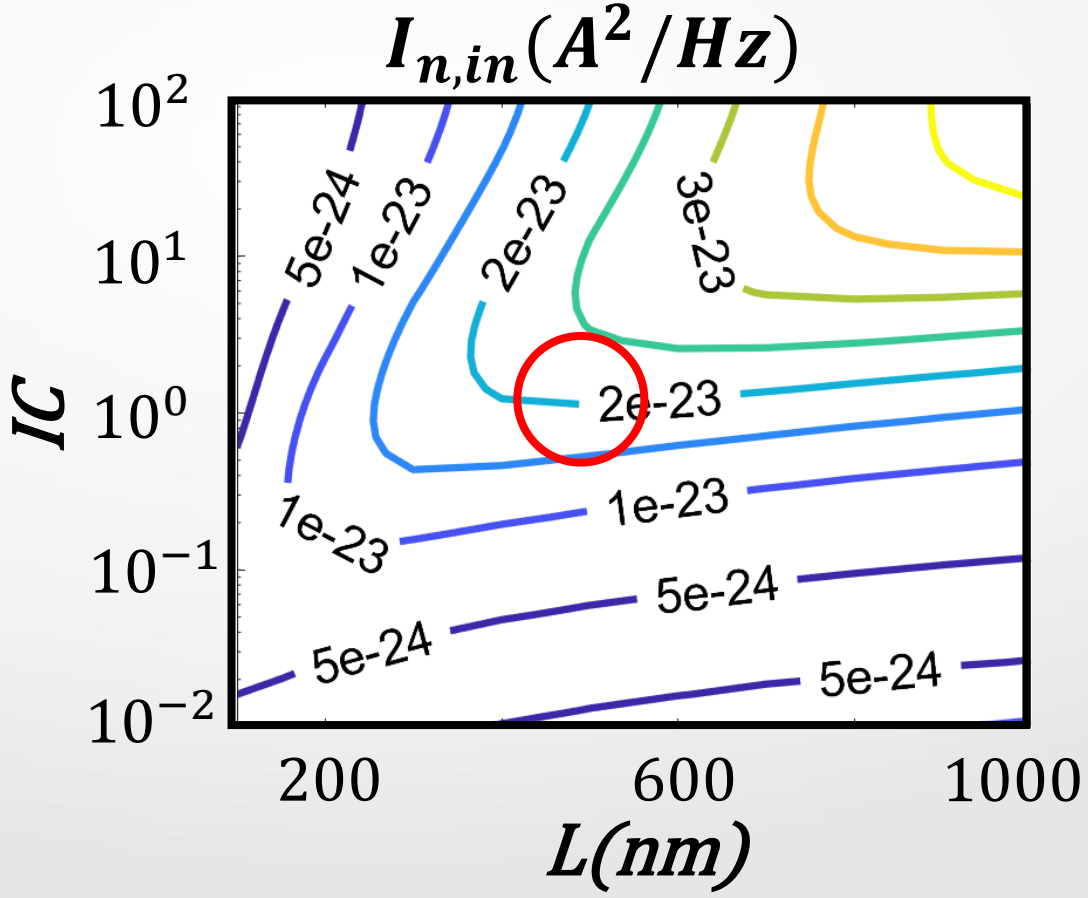
- A_0 trade-off :
  - ① Target value of min. 25 dB.
  - ② Limit IC to avoid excessive current consumption.
  - ③ L high enough to avoid excessive flicker noise.
  - ④ Minimum L to limit size.



Exploring the Design Space

- Simulated characteristics vs IC and L :
  - Noise comply with the specification.





Design Method

METHOD

Technology Extraction

- $I_{spec\_sq}, \lambda_c, C_{gd_l}, C_{(gs+gb)_{sq}}, I_{nD}^2$ …

Circuit analysis

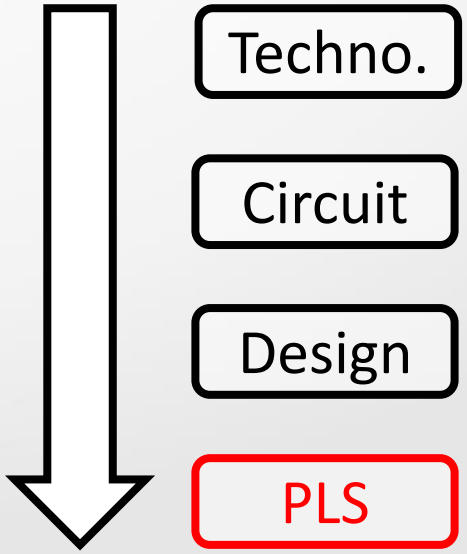
- $A_0(IC_n, L_n, \dots), R_T\ (IC_n, L_n, \dots), \dots$

Design space

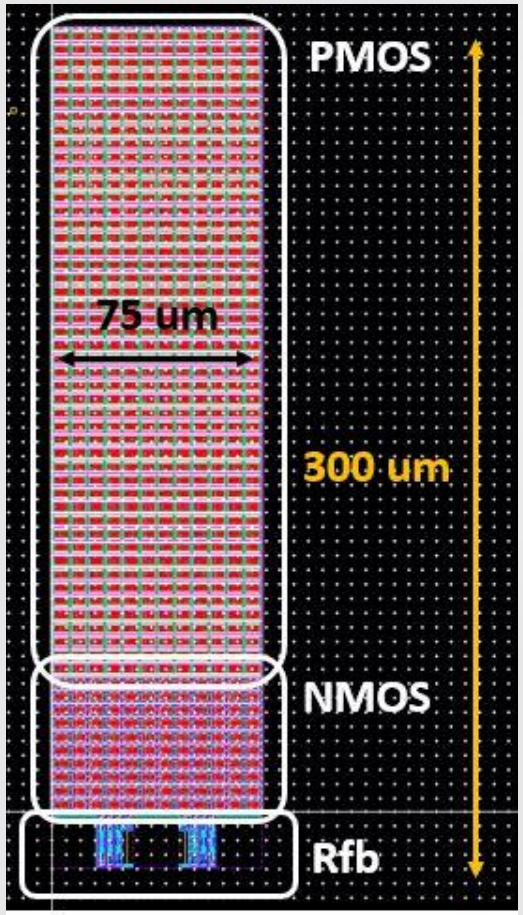
- $IC_n = 2, L_n = 480\ nm, W_n = 1\ mm$ …

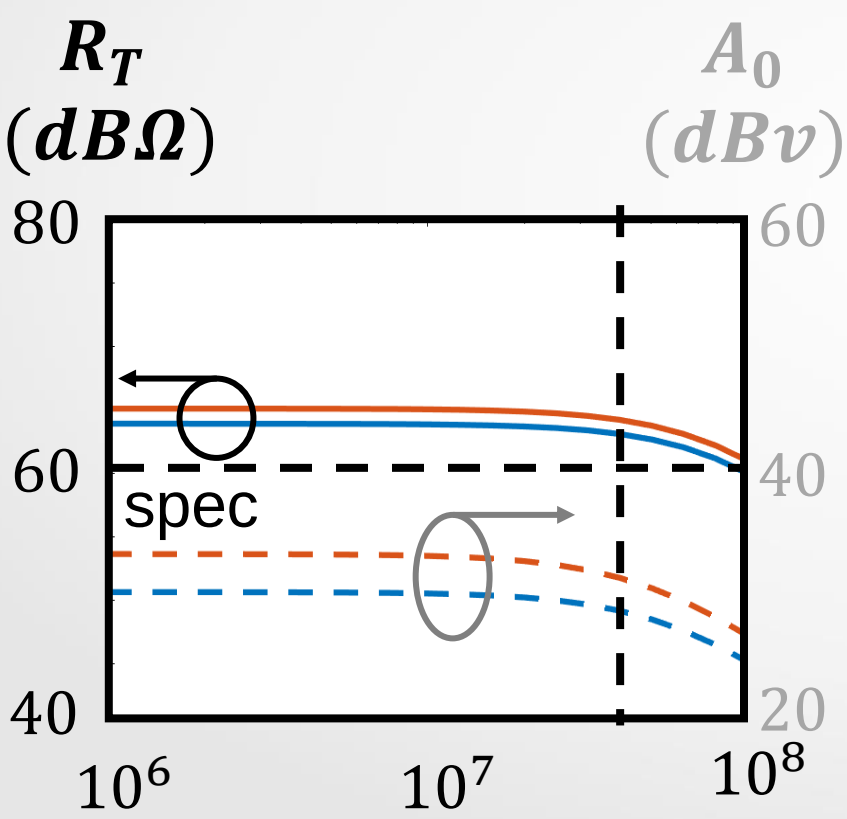
PLS

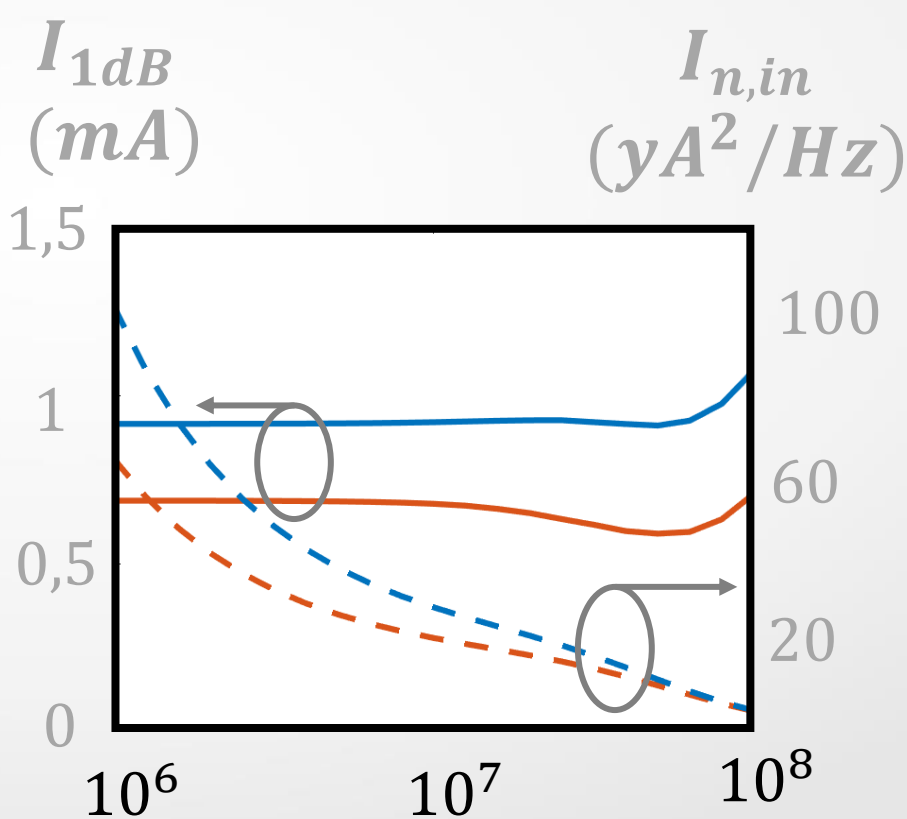
Outline



Post-Layout Simulations







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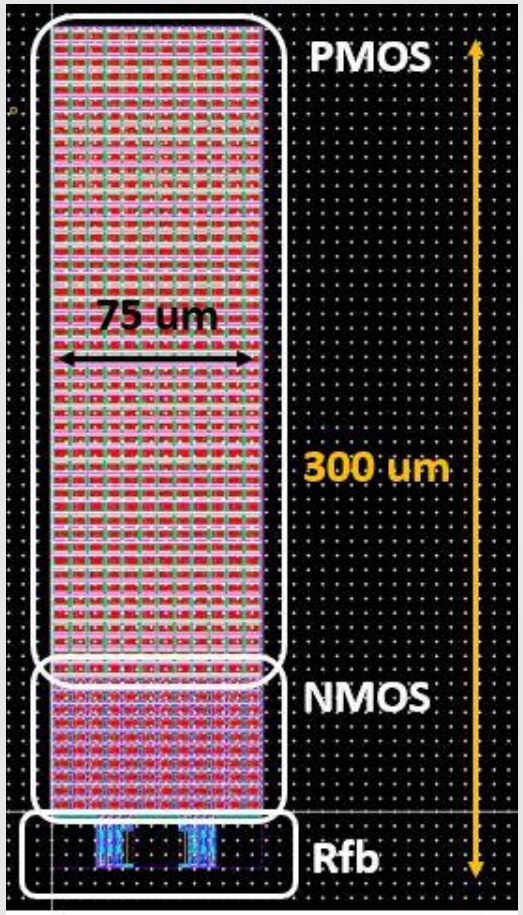
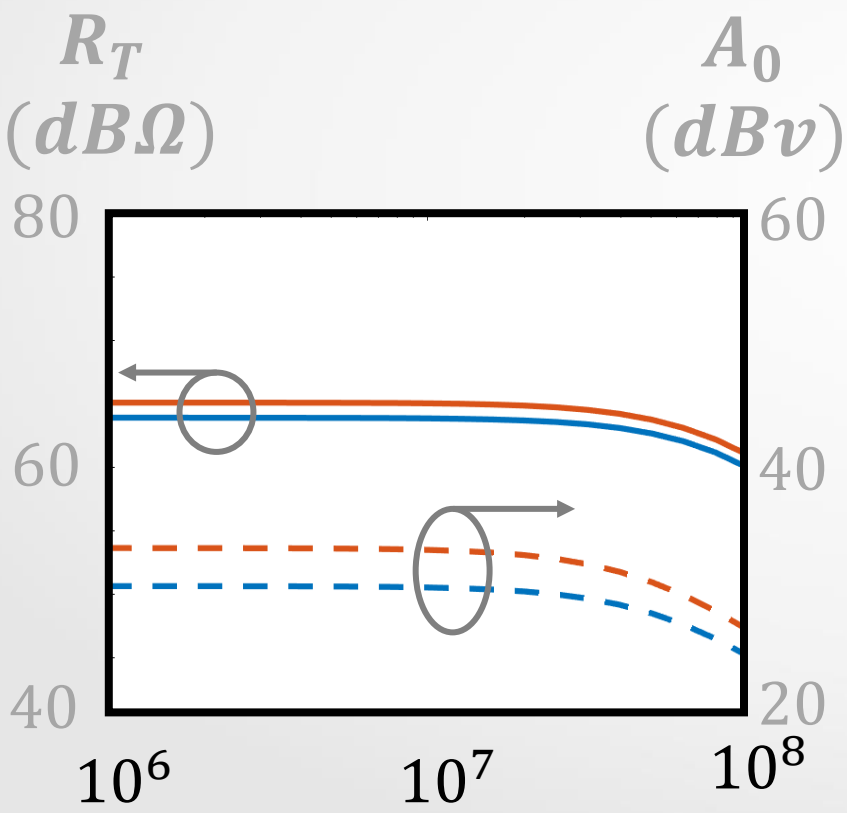
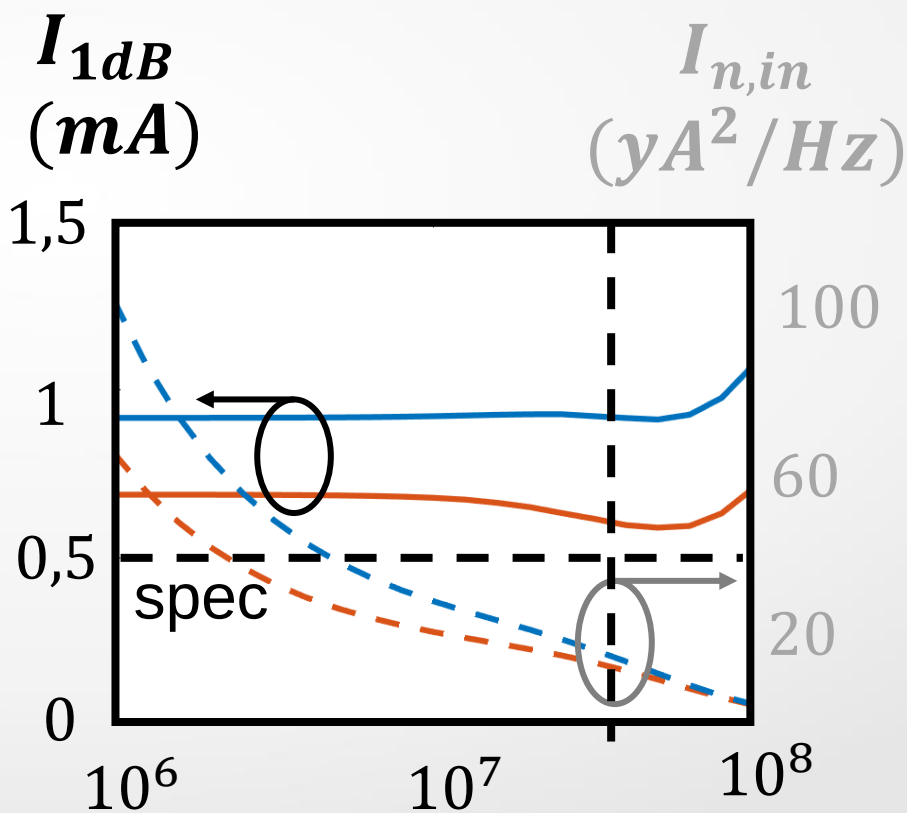
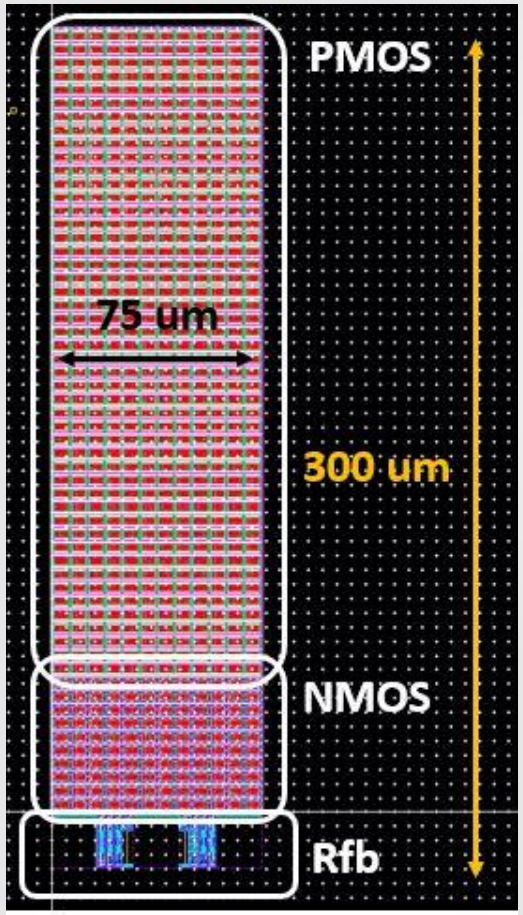
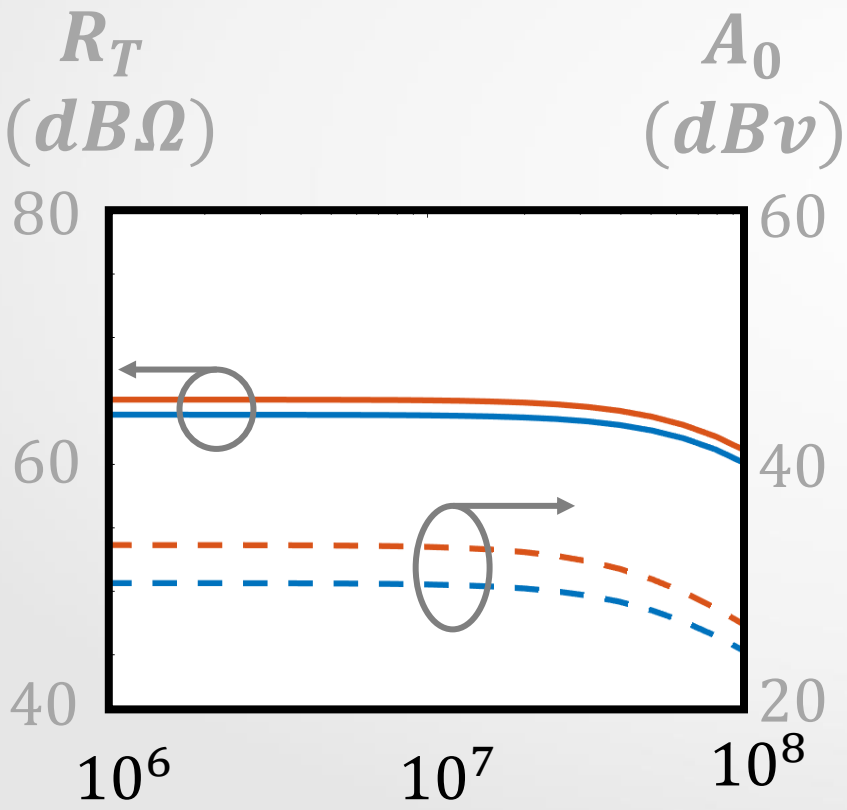


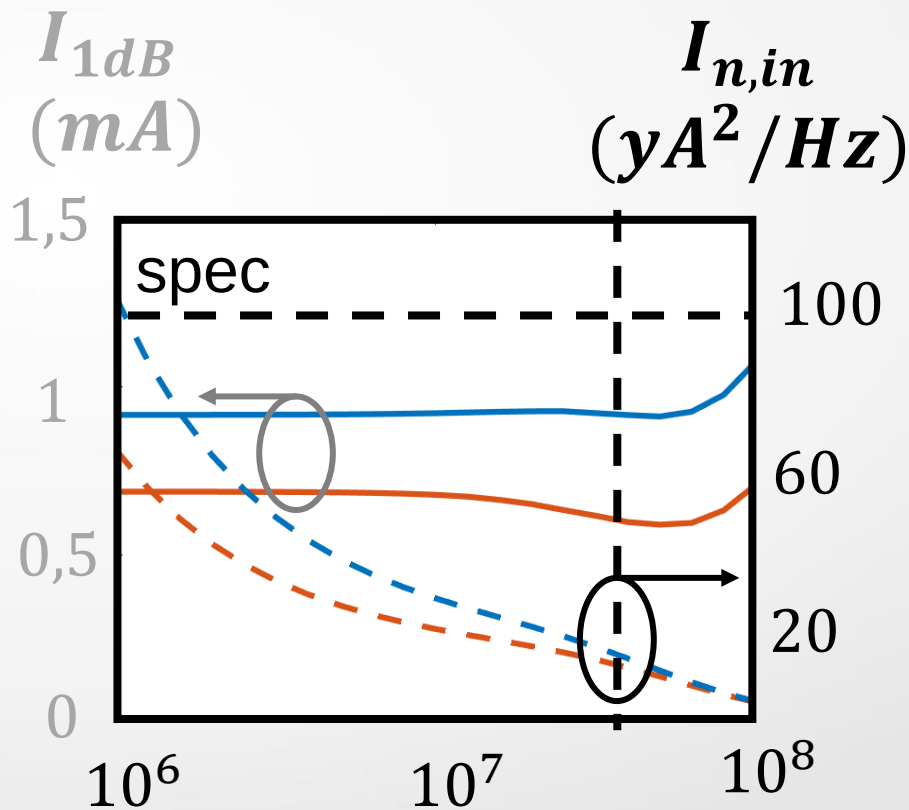




Post-Layout Simulations







Model vs Simulations

	Model	Post-Layout Simulations	Specifications
$A_0\ (dBv)$	36	33.8	
$R_T(dB\Omega)$	65	65.1	63.5
$BW\ (MHz)$	N/A	80	50
$R_{IN}\ (\Omega)$	56	74	< 100
$I_{n,in}(yA^2.Hz^{-1})$	20	53/17*	< 100
$A_{0,cm}(dBv)$	6	6.2	N/A
$V_{DD}\ (V)$	N/A	1.8	1,8
$I_{DC}\ (mA)$	N/A	7.4	10

*@ 1 MHz/@ 10 MHz

Design Method

METHOD

- Technology Extraction → • $I_{spec\_sq}, \lambda_c, C_{gd_l}, C_{(gs+gb)_{sq}}, I^2_{nD}$ …
- Circuit analysis → • $A_0(IC_n, L_n, \dots), R_T\ (IC_n, L_n, \dots), \dots$
- Design space → • $IC_n = 2, L_n = 480\ nm, W_n = 1\ mm$ …
- PLS → • **Method validation and final design !**

Outline

- General Context
- Inversion Coefficient Model
- Circuit Analysis
- Design Space Exploration
- Post-Layout Simulations
- Conclusion

Conclusion

- TIA designed for automotive radar applications.
- TIA design method highlights the topology trade-offs.
- Design method covers all inversion zones.
- Design method can be used to compare topologies or technologies.