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Advances on CMOS Image Sensors

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Abstract

This paper offers an introduction to the technological advances of image sensors designed using complementary metal–oxide–semiconductor (CMOS) processes along the last decades. We review some of those technological advances and examine potential disruptive growth directions for CMOS image sensors and proposed ways to achieve them. Those advances include breakthroughs on image quality such as resolution, capture speed, light sensitivity and color detection and advances on the computational imaging. The current trend is to push the innovation efforts even further as the market requires higher resolution, higher speed, lower power consumption and, mainly, lower cost sensors. Although CMOS image sensors are currently used in several different applications from consumer to defense to medical diagnosis, product differentiation is becoming both a requirement and a difficult goal for any image sensor manufacturer. The unique properties of CMOS process allows the integration of several signal processing techniques and are driving the impressive advancement of the computational imaging. With this paper, we offer a very comprehensive review of methods, techniques, designs and fabrication of CMOS image sensors that have impacted or might will impact the images sensor applications and markets.

1. Introduction

The image sensor market as a whole has presented one of the largest compound annual growth rate of all electronic application markets (Mounier et al., 2014). Charge-coupled device (CCD) and CMOS image sensor (CIS) are the two main technologies in this market. Initially devices based on CCD technology presented better features such as image quality than the CIS-based devices as CCD was quickly optimized for imaging applications. In its early days, CIS devices suffered from higher noise levels which limited their ability to produce good quality images. CIS devices were used mainly for applications where image quality was a less important factor than costs.

However, the CCD technology have been surpassed in the market volume by CIS technology. The principal commercial reason is that the CCD manufacturing is costly compared to CIS. The latter uses the CMOS manufacture process which is largely used in most of other larger electronic markets such as computing and communication. This widespread utilization drives the cost per unit to much lower levels than CCD processes. The consistent reduction of CMOS feature size following the empirical Moore's law also enables pixel size reduction which further drives their cost down. Lower power consumption (for in-chip digital image processing) and potential functional integration are other driving factors leading to the preponderance of CIS devices.

Nowadays current CIS devices present comparable image quality to CCD because of the immense effort from the CIS design and fabrication teams in the last decade or so. This was achieved by a series of innovations including the development of buried (or pinned) photodiodes, previously used in CCD imagers, in CMOS processes. These photodiodes contributed with noise reduction by greatly reducing the carrier traps in the $Si{-}SiO_2$ interface and by enabling correlated double sampling (CDS). This led to the evolution from noisy 3T-APS (three transistors active pixel sensors) to more advanced 4T-APS devices. Figure 1 shows typical 3T-APS and 4T-APS circuits (Choubey et al., 2014). While both incorporate a reset transistor M_{rst}, a buffer source follower M_{sf} and a select switch M_{sel}, the 4T-APS introduces a buried photodiode in place of a p-n junction photodiode and a transmission gate M_{tx}. This pixel led to a surge in low cost digital imaging and it is used by most CIS devices embedded in toys, mobile phones, computers and many DSLR cameras.

In this paper we review some of the techniques beyond the buried photodiode adoption which allowed CIS devices to compete with CCD technology in applications were image quality is fundamental. In section 2 we present some techniques that gave the CIS devices a big advantage over other imaging technologies on different applications. Furthermore, CIS devices are being designed and integrated with a great degree of signal processing capabilities that are easily implemented in CMOS processes. Examples of such capabilities are illustrated in section 3. The final section provides the conclusion of the paper.

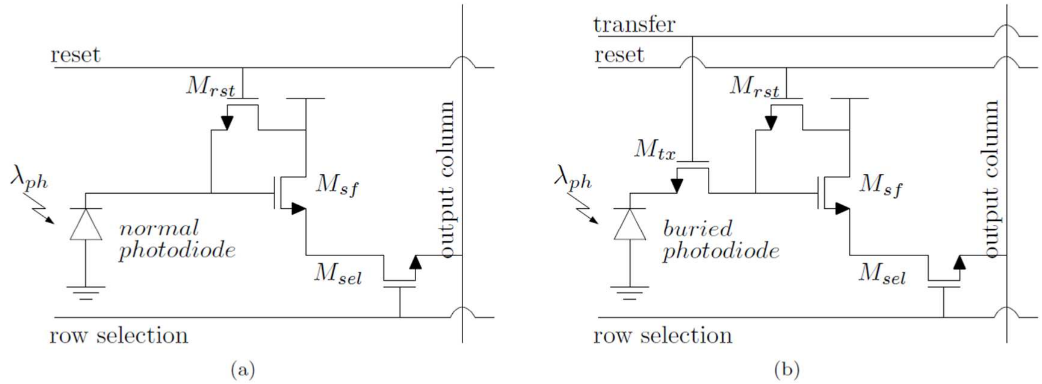

Figure 1: Circuit schematics of 3T- and 4T-APS pixels. Reset and row selection (and charge transfer in 4T-APS pixel) control signals are common to all pixels in the same row while column output signal is the time-multiplexed output common to all pixels in the same column.

2. Advances in image quality

The quality of an image depends fundamentally on its final use. While for some applications just some features need to be discernible, for others an overall visual accuracy is needed. In this section we present the main factors for image quality and advances brought on CIS technology to improve them. These factors are related to the resolution of different aspects of the system: spatial, intensity, spectral and temporal.

2.1. Spatial resolution

Spatial resolution, normally known as just resolution, is the ability of an imaging system to distinguish different parts of an image. Resolution can be measured using methods like modulation transfer function (MTF) and test charts and normally expressed in term of cycles or lines pairs per millimeter (lp/mm). Several factors determine the resolution of an imaging system including the resolution of the lens, focal length and the number of useful pixels on the sensor. Increasing the pixel count has been one of the main focus of the digital camera development in the last decade. The pixel count is still one of fundamental sales pitches for image sensors and market competition has driven the increase of the number of pixels from hundreds of thousands – VGA format, the majority of market share up a decade ago – to hundreds of millions, i.e. megapixels (Julian, 2014). In addition, high resolution imagers also allow for additional functionality like pixel binning to improve performance at low light and windowing or digital zoom, thereby improving cameras with limited optical components.

The increase of pixel count of a CIS is normally obtained by reducing the pixel size itself rather than increasing the overall sensor size. This is mainly due the fabrication costs and also to comply with traditional image formats. Although useful in increasing the resolution, pixel shrinking has its own drawbacks. The most important is the reduction of pixel's full well capacity (FWC) due to the reduction of the photo-detector element. Several techniques have been applied to reduce the pixel size without compromising the FWC considerably. One method is known as pixel-sharing in CIS designs. Pixel-sharing aims to allow some electronic components to be used by other pixels in the vicinity, reducing the total pixel area while achieving similar FWC. This is particularly suitable for use with pixels in 4T-APS, where most of the transistors (reset, source follower and row selection) can be shared while the transmission gate (TX) is used to isolate the photo-diode of each pixel. Several sensors present different pixel sharing configurations such as 2.5T, 1.75T and 1.5T, where 2, 4 and 6 adjacent pixels share common transistors (Kim et al., 2006). Another design technique to preserve the FWC of the pixel is to implement small openings in the photo-detector's p-n junction (Ay, 2011). This is known as peripheral utilization method and aims to increase the overall depletion area of the photo-detector as the further increasing of its lateral area surpass the surface area loss due these openings.

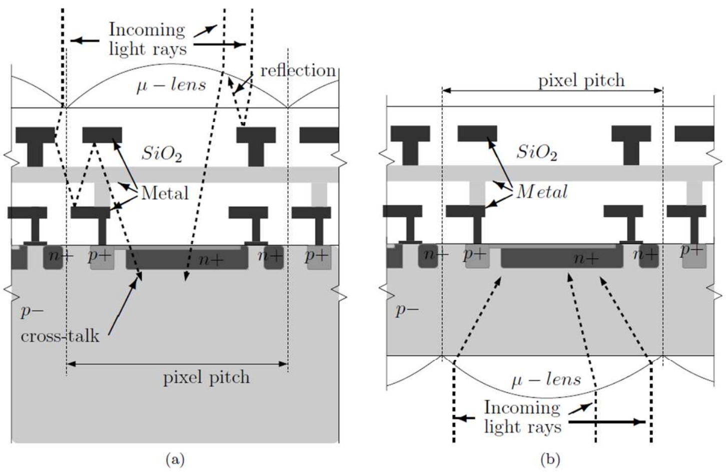

Figure 2: Cross section of two different CIS design approaches. Light falls upon the photodiode throughout the metal layers in a front-side illumination design as in (a) while in (b) – a back-side illumination design – the incoming light reaches the photodiode depletion through the substrate, increasing the fill-factor of the pixel.

In addition to these design methods, fabrication methods are also used to increase the resolution. A good example is swapping the exposed side of the sensor. Most of early sensors were front-side illuminated (FSI), meaning that the light hit the silicon substrate from the side of the sensor where the metal connections are laid out. This situation, as shown in figure 2a, imposes the light to go through those metal and isolation layers. This leads to the reduction of the fill-factor (FF), i.e. the ratio of photo-diode area to the total area of the pixel, and the increase of cross-talk effects. Inverting the side of light incidence as in figure 2b introduced back-side illumination (BSI) to many of the current designs. This allows for further pixel size reduction with similar fill-factor; however, it requires extra processing steps to thin the substrate prior the deposition of anti-reflective layers. The method of resolving colors can also impact the resolution as will be explained in section 2.3 as well non-CMOS approaches for light capture itself such as quantum dots (Tian and Sargent, 2012).

Cross-talk occurs when the signal (light intensity) supposed to be detected by one pixel is also partially detected by neighboring pixels. It reduces the image contrast and is a limiting factor on the pixel size reduction as the pixels are currently smaller than the light path inside the sensor. Optical and electronic cross talks are common. Light reflection on metals is an example of the former and photo-generated carrier diffusion is the main source of the latter. Cross-talk reduction can be achieved employing microlenses and light guides (Tut et al., 2010) to focus the light on the detector area of the pixel and by reducing the number of metal layers for FSI designs. Also front-side deep-trench isolation (F-DTI) can improve the optical properties (Tournier et al., 2011). These not only electrically isolate the pixels by creating a SiO_2 wall, but also act as light reflector due to the difference of Si and SiO_2 refraction indexes.

Although most imaging applications can rely on pixel shrinking to increase resolution, there are cases where it is desirable to increase the sensor size instead (format size) such as to enable photographic features like shallow depth-of-view. Moreover some specific imaging systems cannot reduce the pixel size for different reasons. In radiation detection (X-Ray imaging, high energy particle detection) the optical system has low optical gain (low focus capability) and therefore the sensors size is comparable to the image size (Turchetta et al., 2011). In astronomy or aerial reconnaissance image sensors, the image quality loss due to pixel reduction and lens design is prohibitive. These large format image sensors face different challenges. The readout speed is a concern due to their increased parasitic capacitance. In addition, the die of the image sensor is limited in size by the wafer size itself; increasing the format of such image sensors requires multi-chip stitching (Yamashita et al., 2011). Stitching also leads to high levels of “dead” pixels on the interfaces and increase FPN on the whole image sensor.

2.2. Dynamic Range

The intra-scene dynamic range is a measurement of the capability of capturing light intensity by an image sensor. Although exposure time and aperture settings can be adjusted to avoid under- or over-exposure of some parts of the object of interest, dynamic range defines the relation between the maximum and minimum light intensities that can be detected simultaneously. This is an important specification in many applications in automotive, security and surveillance, medical and scientific fields. However conventional CMOS image sensors have a somehow limited dynamic range of typically between 3 and 4 decades of intensity, i.e., a ratio of 1000:1 to 10000:1 between the highest and the lowest light intensities that can be captured in a scene. This relatively short range leads to inaccurate representation of scenes containing regions with different light intensities. For these scenes, the produced image will present loss of information in areas too dark or too bright or both. To illustrate this limitation, the human eye can detect light intensities over 6 decades though adaptation. Figure 3 illustrates the dynamic ranges of two sensors: a conventional low dynamic range (LDR) CIS and a wide dynamic range (WDR) CIS.

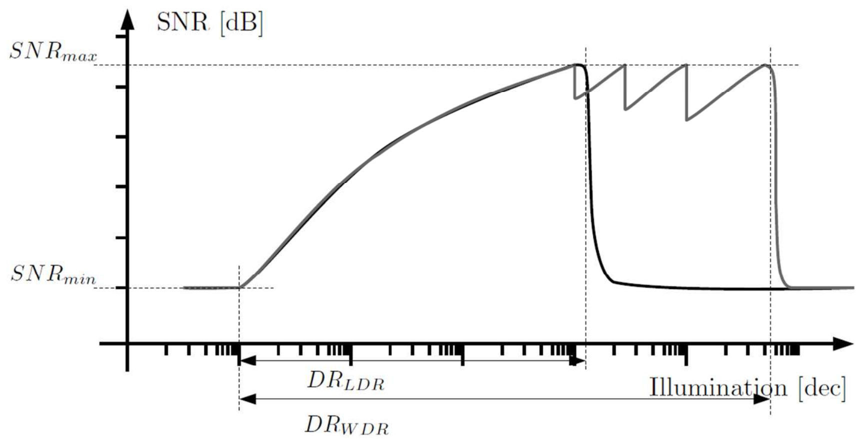

Figure 3: Illustrative comparison of the dynamic ranges of a LDR and a WDR CIS. In this case the WDR sensor operates with a multiple exposure WDR method.

Multiple-image capture using different exposure times with a conventional (LDR) CIS (Mase et al., 2005; Yadid-Pecht and Fossum, 1997) is the most common approach to extend the dynamic range of a CIS. The main advantage is the use of conventional imagers to acquire the image but post-processing is required, leading to low frame rates and other artifacts like ghosting and blurred images. Several other approaches have been presented, mostly introducing specific pixels topologies to address particular specifications. Those include logarithmic pixels (Choubey and Collins, 2007), multi-mode operations (Storm et al., 2006), capacitance adjustment, frequency-based and time-based pixel operation and selective integration time (Choubey, 2011; Yadid-Pecht, 1999).

In general, the upper limit of the dynamic range is defined by the FWC of the pixel, i.e., the amount of photo-generated charge that the photo-detector can store without blooming. As explained in the previous section, the reduction of the pixel size almost always reduces the well capacity and hence, the dynamic range. On the low end of this range, several noise sources (thermal noise, readout noise and others) are the limiting factors. Thermal noise is due to the thermal generation-recombination of electrons and holes on the silicon substrate. These carriers are then collected by the photo-detector in the same way as the carriers generated by the photon absorption. In astronomy and other fields a common practice is to cool the sensor and associated electronics to cryogenic levels, however this is not practical to other applications. Parasitic leakage currents due to defects near the isolation regions also generate noise. Diffusion implants or a polysilicon layer surrounding the photo-diode (Choubey and Collins, 2008), the use of buried photo-diodes and buried channel transistors (Wang et al., 2008) can be used to reduce the effect of these on the image sensor. Ultimately a number of noise sources can be partially reduced using high-gain column-level amplifiers and correlated multiple sampling (CMS) (Chen, Xu, et al., 2012).

2.3. Colors and more

Normally the representation of the light intensity in a scene is not the only important measurement. One needs to discriminate other characteristics of the light as well such as its wavelength. Light with different wavelengths in visible spectrum are categorized in colors and this information is fundamental not only for consumer application but also in a variety of process and quality control as well as detection cases such as spectroscopy.

In both CCD and CMOS image sensors color detection is commonly achieved with the application of filters with different transmission center frequency onto different pixels in the sensor resulting in a color filter array (CFA). Therefore pixels associated with the same filter constitutes a different color channel. These filters are mostly organic color dyes applied on the light path. The transmission coefficient ranges from about 70-90% on the band pass of the filter resulting in an overall 30-50% transmittance due the off-band transmission on visible spectrum (Nishiwaki et al., 2013). Therefore its application reduces the overall light absorption, i.e. its quantum efficiency (QE), and reduces its application in low light environments.

Ideally an image sensor should discriminate as many different colors as required. However, owing to the color theory and human's color detection mechanism (retina's cone cells), traditionally only three color filters, corresponding to the primary colors, are required for general photography with other colors being represented by weighted addition or subtraction in post-processing computations. One advantage of relying on just three color channels is that the reduction in the overall sensor resolution is small. In the popular Bayer color pattern (RGGB), each color "pixel" consists of a 2-by-2 array of photo-detectors where two are designated to green channel and each of the other two are for the blue and red channels, as shown in figure 4a. Therefore, the image sensor resolution due to this color pattern is a quarter of the original sensor. Using the same principle for color separation, increasing the number of different color channels implies further reduced spatial resolution.

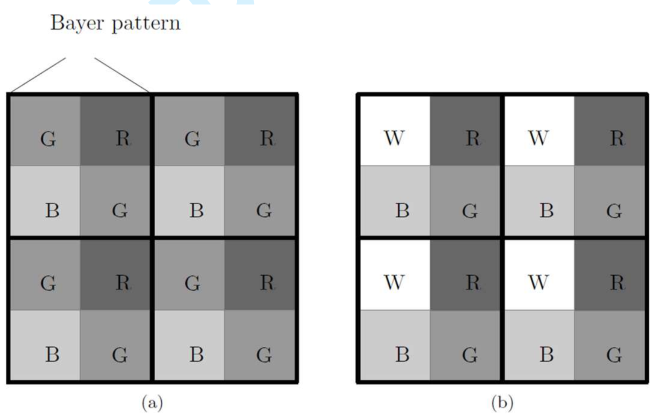

Figure 4: Different color patterns. Figure in (a) is the widely used Bayer pattern, i.e. the red-green-green-blue (RGGB), while the configuration in (b) shows an alternative color pattern (RGWB) to increase the quantum efficiency of the sensor.

Some variations of the Bayer pattern are used to increase the QE of the sensor. In RGBW/RGBC patterns, shown in figure 4b, one of the green filters are removed to better measurement of the illuminance while in RCCB pattern the green filters are removed completely (Fossum, 2011) with the green component being extracted from color subtraction. As in the case of monochromatic image sensors, cross-talk can limit the accuracy of the image. In the case of color cross-talk, it is the color fidelity that can be compromised. In addition to methods already cited to reduce cross-talk, the color filters must be placed as close as possible of the related photo-detector.

Color detection can also be accomplish using other methods. In diode stacking designs (Lyon and Hubel, 2002) every pixel can capture all three colors due to wavelength-dependent absorption depth on silicon. Three photo-detectors are precisely stacked and post-processing algorithms are used to extract color information and attenuate the inherent color cross-talk (Battiato et al., 2012). Another alternative to maintain the QE is using color splitters rather than color filters (Nishiwaki et al., 2013). On every second pixel, a splitter is placed resulting in white minus red (W-R) for this pixel and white plus red (W+R) for adjacent pixel. Adding a similar pattern with blue splitters and further post-processing, primary colors are obtained. More experimental approaches include implementation of selective color absorption using nanowires (Park et al., 2014) and plasmonic color filters (Chen, Das, et al., 2012). The former use silicon nanowires as photodiodes and relies on the variation of their wavelength sensitivity according to their diameter. The latter uses thin metal layers patterned in a way that light at a specific wavelength can couple with the metal surface plasmons and filtered from the photo-detector. This method has the advantage of being fully compatible with commercial CMOS process and do not require extra fabrication steps.

CMOS image sensors are primarily used for visible range (typically from 400nm to 700nm wavelength band) of the electromagnetic spectrum due to silicon physical properties, mainly its band-gap. However other spectral bands offer extra image information and specific image sensors are required to detect such wavelengths. Wavelengths shorter than the visible spectrum start with the ultra-violet (UV) band (10nm-400nm) which is used to detect scratches on materials and in biology, for instance. CIS are naturally sensitive to near-visible UV band but need extra manufacture processing (Wang and Wolfs, 2012) or well-controlled doping patterns (Kuroda et al., 2013) to work in deeper UV bands.

For even shorter wavelengths including X-rays, CMOS image sensors can be used though these detectors normally require large format arrays wherein a scintillator layer is applied onto the sensor. This layer allows for the conversion of the X-rays ionizing radiation into visible light. Furthermore CIS are now directly sensitive to X-rays over a good energy band without the need for a scintillator. This is due to the reduction in thickness of the polysilicon layer in typical CMOS process.

On the other side of the spectrum the first band after the visible is known as infrared (IR). IR detectors are used to trace sources of heat and are used in applications as defense, night vision, health and industrial monitoring (gas and heat leakage) for instance. Silicon is sensitive to near-IR region and therefore most CIS can be used as IR detectors (although most commercial cameras incorporate IR-cut filters to avoid IR detection).

For detection of mid- and far-IR spectrum the silicon 1.12eV band-gap implies that it is mostly transparent to wavelengths above 1.1µm. Although detection of longer wavelengths were reported using autocorrelation techniques on multi-photon absorption (Briggman et al., 2001) or tunneling mechanisms (Shalaby et al., 2015), those methods require high light intensities, typically from laser sources. Therefore indirect ways of detection have also being used, requiring integration of other materials with silicon or its replacement as the detector element altogether. For mid-IR, materials include intrinsic semiconductors such as MTC and InSb, extrinsic varieties as Si:As and Si:In, black silicon and micro-bolometers (using either Vanadium oxide compounds or amorphous silicon). Integration of such materials directly on CMOS process is difficult and expensive and normally require 3D integration using techniques such as flip-chip bonding, which reduces the overall resolution of such sensors. In far-IR band, also known as THz imaging, other mechanisms can be implemented as integrated antenna-based approach (Sherry et al., 2012) and integration of meta-materials with bolometers (Grant et al., 2013).

2.4. Acquisition Speed

In most imaging applications, common scenes are not static but change with time. This requires the sensor to capture a sequence of images (video) with a specified, mostly fixed, time period between those images (frames), defining the frame speed. When the composition of the scene can change during the capture of each frame, the capture method (shutter method) also impact the quality of the image. We first report on the shutter method and later we details the improvements on frame speed. The shutter method broadly refers to the synchrony between all sensor's pixels. In other words, it refers to the time when the pixels are exposed to the light. Originally CIS were designed to provide a rolling shutter mechanism due to its simpler scanning readout implementation. With this method, pixels in one row start and stop light capture (integration time) at slightly shifted time from the pixels in the previous row, for instance. This may generate a number of different distortion effects on fast changing scenes with one being exemplified in figure 5.

The time integration window in global shutter imagers are applied to all pixels simultaneously. Although this method requires more complex readout and pixel designs, it is essential in applications as 3D-vision, machine vision and automotive. On conventional scanning-based readout imagers, it requires the use of in-pixel memory to temporarily store the light-converted information. The efficiency of this memory relates to the shutter efficiency of the imager. Digital memories, as used in digital pixels, are more reliable than their analog counterparts but they require a prohibitive large in-pixel area.

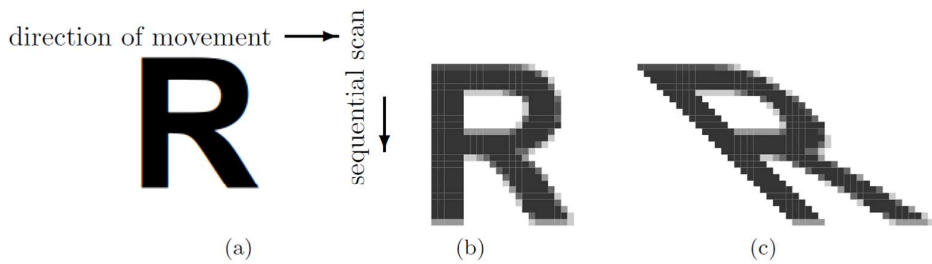

Figure 5: Examples of impact of different shutter techniques on fast changing images. In global shutter imagers the image (b) retains its original shape (a). Rolling shutter cameras, although benefiting from a simpler design, are prone to the image distortion as shown in (c).

In contrast, analog memory is prone to suffer from charge leakages including light-induced current leakage (parasitic light sensitivity) from the p-n junctions of the memory itself (in case of a storage diode) and from the MOS switches. Some techniques to reduce this leakage include light shielding on the memory area; doping profile to allow parasitic light generated carriers to be collect by the photo-diode rather than the memory; placement of the memory in an isolated well which compromises the fill-factor or other type of protection layer (Yasutomi et al., 2010); use of CDS techniques (Meynants et al., 2011) and the use of 3D stack designs, where the memory element is on a different, light insensitive substrate (Aoki et al., 2013).

Speed frame relates to the number of images that can be captured in a fixed time. This specification is crucial for video applications such as high-definition video, machine vision, 3D vision and scientific applications for instance. High-definition video, as defined by ITU recommendation 4k UHD and 8k UHD (ITU, 2012), requires both high resolution - 8.3 and 33.2 million pixels respectively - and high speed capture up to 120 frames per second (fps). Other applications, although less demanding on spatial resolution, require capture of millions of frames per second (Tochigi et al., 2011).

Most CIS are multiple-inputs, single-output (MISO) systems. Hence the frame speed is closely related to the processing speed on each step on the signal chain to reduce bottleneck situations. Successive improvements have been based on the analog-to-digital conversion (ADC) placement on the signal chain: from initial analog output systems, where digitalization was performed off-chip, to most common column-based ADCs, as shown in figure 6, to in-pixel ADC CIS. This ADC migration to as close as from the detector as possible increases digital parallelism. Different ADC architectures, from slower slope ADC to faster SAR-ADCs (Matsuo et al., 2009) and sigma-delta ADCs (Ignjatovic et al., 2012) are also used to increase the total output throughput.

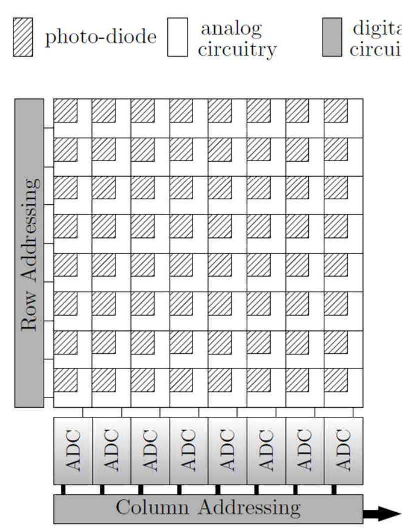

Figure 6: Diagram of a CIS with column-based ADCs. This topology allows for a good compromise between high speed operation and pixel quantum efficiency and it is adopted by most current CIS designs.

Multiple-inputs, multiple-outputs (MIMO) approach is also used to alleviate the bottleneck speed limitation but the output/input ratio is still very close to one as in MISO CIS case. For very fast acquisition CIS, this speed limitation is temporary avoided using internal data storage to implement frame storage. Usually located inside the pixel, this storage allows for burst mode operation where a small number of very fast sequences of images are captured (Tochigi et al., 2011). Optimization of the fabrication process also helps to design faster CIS. For example, in a time-of-flight 3D vision CIS (Takeshita et al., 2010), the photo-diode was implemented with a specific vertical diffusion profile to allow for fast charge transfers from the photo-diodes.

3. Advances in computational imaging

In addition to improving the quality of the image, the image sensors in CMOS processes have also pursued the design of computational imaging systems. Computational imaging relates to the ability of extracting relevant information from the images generated, either post-processing them or during their capture. Some examples of computational imaging applications are focal-point manipulation as in light fields or plenoptic cameras (Damghanian et al., 2014; Venkataraman et al., 2013) and feature extraction applications such as gesture-based user interfaces and eye-gaze tracking. In this section we will describe advances of CIS technology on the particular fields of image compression and 3D imaging.

CIS can promptly benefit from the CMOS process design and integrate signal processing on the same IC of the pixel array using design methods to avoid noise contamination, for instance. However this processing is generally performed outside the pixel array meaning that raw data have to be collected and then processed instead of being processed on the pixel itself. On most current CIS the pixels can, at best, provide a buffer in term of signal processing as the majority of the area of their pixels is reserved to the photo-detector to not compromise the imager resolution. A number of focal plane array circuits have been proposed; however, these circuits have a large number of transistors per pixel, which in turn, reduces the optically sensitive area and hence the fill factor of the pixel. As the result these pixels provide poor optical response.

An alternative is to use a new imaging stack to improve the performance of these pixels. This sensor consists of a BSI sensor flip-bonded to a processing chip as shown in figure 7, consisting of several circuits such as an ADC per small pixel sets to provide for more powerful image processing. Such designs also provide an opportunity to explore comparative pixels previously proposed (Cheng et al., 2007; Choubey, 2010). These pixels utilize a comparator inside each pixel, as shown in figure 8. An externally applied reference voltage is used to stop the recording of integrating pixel voltage. By suitably designing the pixel reference, one can obtain any monotonically increasing transduction function from this pixel. Of particular interest to us is the tone mapped response, wherein a wide dynamic range image can not only be captured, but also outputted on a format suitable to be directly displayed on a low dynamic range display as well (Gouveia et al., 2014).

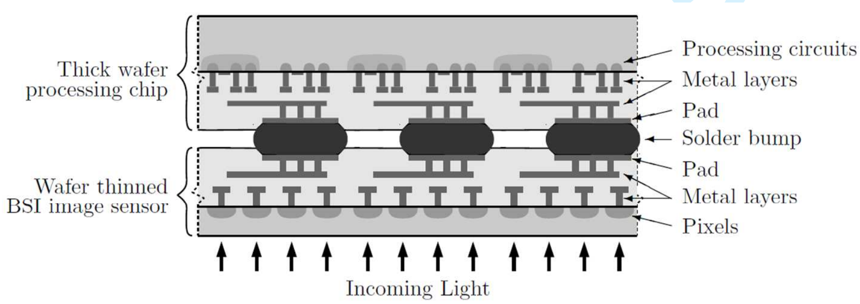

Figure 7: Imaging using stacked chip with different sensing and processing chips connected through flip-chip bonding (illustrated case) or through silicon vias.

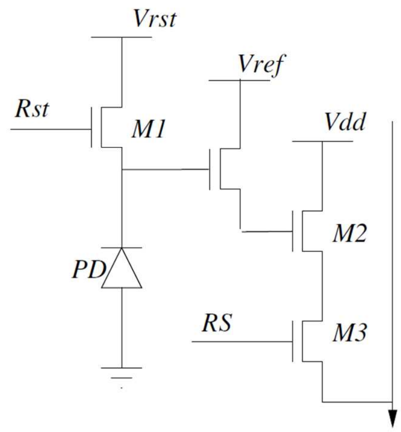

Figure 8: A comparative pixel with the ability to produce tone mapped response by applying a time-varying voltage to the pixel's reference input node V_{ref}. Several different tone mapping functions can be used with this pixel structure.

3.1. 3D imaging

Whereas traditional imaging capture a scene onto a two dimensional representation of it, some applications require information of the other spatial dimension (depth) as well for the determination of the relative distance of the objects presented in the scene. Such applications include virtual reality, navigation support, topography, biosensing and machine vision. This distance can be measure using either interferometry, triangulation or Time-of-Flight (ToF) techniques (Buttgen and Seitz, 2008). Interferometry requires very well defined and stable scene setup (avoiding vibrations for instance). Although it can use common CIS, some dedicated CIS has been developed to cope with their frame rate and sensitivity requirements (Beer and Seitz, 2005). Due to its short depth range in white light interferometry, it is used mainly in microscopy. Triangulation method uses geometrical measurements and can be active or passive (stereo vision). In its passive form, this system requires accurate synchrony of two or more conventional CIS, extensive post-capture signal processing. Furthermore, its chip integration is a challenge due the spatial distance of the CIS and its response depends on the object texture.

LiDAR (Light "radar") and ToF imagers use an active source of light to measure the distance of the object. This source of light needs to be synchronized with the sensor. In order to not interfere with the 2D image (when required), the light source and detectors operate in a different spectrum range, usually near-infrared. The light source can be modulated – when phase shift is detected – or pulsed (Piatti and Rinaudo, 2012) – with the elapsed time being measured. Current ToF imagers have low resolution mainly due the need of larger photo-diodes. ToF also requires fast readout and some imagers are based on Single-Photon Avalanche Diode (SPAD) devices working on time-correlated single-photon counting.

3.2. Compression

CIS technology allowed for substantial decrease of image sensor costs and, therefore, levered the massive use of image sensors these days. This led to an increasing pressure on both transmission and storage systems as the number of cameras and their individual resolution dramatically increases. It is worth noting that in many applications not every pixel in an image presents useful information. Several systems can extract just the relevant features for the targeted application leading to data compression. Traditional compression algorithms have been implemented on-chip such as discrete cosine transform (DCT) (Tan et al., 2012), predictive coding (Chen et al., 2006) and feature-extraction based (Massari et al., 2010). However those traditional compression algorithms are post-acquisition computation methods. In other words, the image is firstly captured in full resolution and compressed afterwards, penalizing both energy and time consumption.

Compressed sensing (CS) has a different approach for compression. The compression of the image is performed at the same time the sensor capture it (Donoho, 2006), sampling only the important k

components of the image. No previous assumptions on the image characteristics are required other than its sparsity. Compressed sensing outputs are composed of a series of M "measurements" $y_{M\times 1}$ produced by some transformation (known as a measurement matrix $\phi_{M\times N}$) onto the image with N pixels $x_{N\times 1}$ ($k < M \ll N$). It has been shown that the best measurement matrix ϕ has random coefficients. This CS approach alleviates the load on both storage and transmission but the computational requirements of reconstructing the image is highly increased.

As the compression and image acquisition are inseparable, traditional CIS cannot be used and hence specific CIS designs have to be used. One of the first CS oriented sensors are single-pixel sensors associated with an array of digital micro-mirror devices (DMD) (Duarte et al., 2008). Implementations using more conventional multi-pixel arrays have been implemented using coded aperture cameras, switched-capacitor integrators (Dadkhah et al., 2013) and column sigma-delta ADCs (Oike and Gamal, 2013). Such sensing has been applied to a wide range of applications but more specifically where images are known to be sparse as in medical (MRI and CT), security (radar) and astronomy.

4. Conclusion

CMOS image sensors have proved to be a fascinating technological challenge in the last decades. From overcoming initial limitations on image quality to implement additional functionalities to the system, much effort has been demanded by the one of the fastest expanding electronic markets. All of these have been achieved with the low-cost and highly-integrated CMOS process.

In this paper we have reviewed the evolution of CIS with a view on potential future impact of the technology. Advancements have been achieved in many areas of the image sensing, including increasing resolution and capture speed. However, due to product differentiation being even so difficult to achieve on traditional applications, many different application fields are being explored. These requires specific functionalities such as a wider dynamic range, extended spectrum detection and focal plane processing. These potential applications and their proposed technological advances have also been explored.

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