High bandwidth memory interface design based on DDR3 SDRAM and FPGA

Baopo Wang[1,2], Jinsong Du[1,3], Xin Bi[1,3*] and Xing Tian[1,3]
[1]Shenyang Institute of Automation, Chinese Academy of Sciences, China
[2]University of Chinese Academy of Sciences, China
[3]Key Laboratory of Liaoning Province on Radar System and Application, China
E-mail: wangbaopo@sia.cn
*Corresponding author: Xin Bi; E-mail: bixin@sia.cn

Abstract—**This work presented the high bandwidth memory interface design based on DDR3 SDRAM using external memory IP core provided by FPGA devices. The structure and configuration of IP core was introduced and the simulation on soft and hard IP was carried out with the access controller designed. The maximum transmission bandwidth of the memory interface based on the soft and hard IP respectively reached 19.2Gbps and 25.6Gbps. Finally, the reliability of the interface controller was verified by downloading the program to the DAQ board and observing the internal signals.**

Keywords-Memory interface; DDR3; FPGA; IP; High bandwidth

I. INTRODUCTION

Memory performance has become a key factor in improving the overall performance of the real time system[1], requirements on the data processing, the stability and the power consumption is being higher. The relatively mature memory technology is SDRAM, DDR, DDR2 and DDR3. The DDR3 has higher bandwidth and lower power consumption, and therefore become the preferred scheme in high speed and real-time data storage system design. As the operation timing sequence of DDR3 is rather complex, there are special interface for most common system chip, while system based on FPGA can be generally implemented with the IP core (Intellectual Property core) for external memory interface provided by the device. Apply the IP provided by the FPGA chips to the system design can reduce the workload and the development costs as well[2].

II. HARDWARE DESIGN OF MEMORY MODULE BASED ON DDR3

This paper shows the DDR3 interface design for the storage module of a high speed data acquisition board. The storage module of the acquisition board uses two chips of 16 bit DDR3 SDRAM to constitute the 32bit data width. The Cyclone V series FPGA device provided by Altera is used as system controller chip. On the hardware design aspects, the method in reference [3] is adopted to ensure the signal integrity of the fly-by signals.

Fig.1 shows the schematic of the data storage module, using two memory chips of DDR3 SDRAM which are unified addressing. The address bus consists of A[14:0] and BA[2:0], while the data bus including DQ[31:0] and the source synchronous clock DQS[3:0].

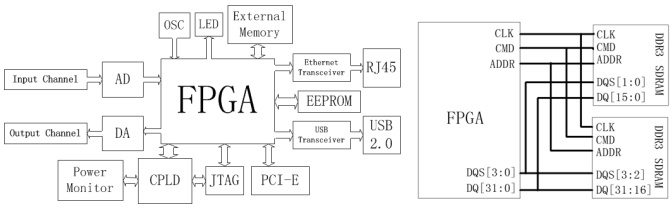

Figure 1. The schematic diagram of the DAQ board and the storage module

III. MEMORY INTERFACE DESIGN AND SIMULATION

A. Introduction and configuration of the IP core.

The devices of Cyclone V series provide available hard or soft IP for external memory interface including DDR3. The role of the IP core is actually a memory interface logic controller used to simplify the user's timing control of memory devices. Structural relationships are shown in Fig.2.

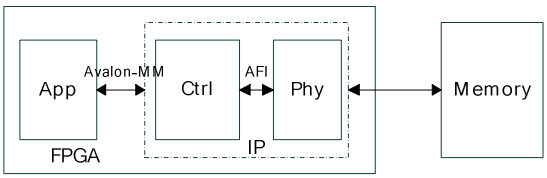

Figure 2. IP structure of the DDR3 interface

It can be can seen that the IP core is composed of Controller unit, PHY unit and some related interfaces. The Controller unit is responsible for the control of the initialization, refresh and other Memory command operation. The PHY unit works between the Controller unit and the external Memory. The AFI interface is simplified from the DFI interface[4] which serves as the PHY Interface of DDR. Cyclone V series devices provide available hard and soft IP for DDR3 interface[5].

With process layout and optimization, the hard IP could fit higher timing requirements. In addition of the difference on performance, there is still a important difference to users: the Hard IP provides a set of MPFE (Multi-Port Front End)[6] signals which can make the multiple processes of FPGA share

one Memory command queue. The MPFE architecture of the hard IP is shown in Fig.3.

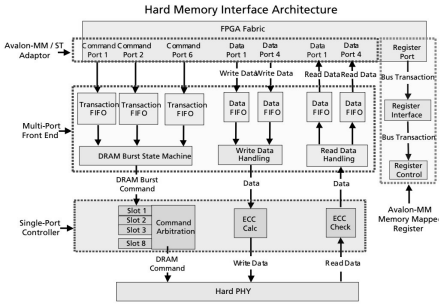

Figure 3. The MPFE architecture of the hard IP

As is shown in Fig.3, the MPFE make the hard IP can support up to six command ports, four read data ports and four write ports. A user port can be configured as bidirectional one, at which time the port will call one read FIFO and one write FIFO to achieve.

B. Memory controller logic design and simulation.

After completing the IP configuration, the access logic need to be designed according to the actual demand. The entire state machine for reading and writing of the memory is shown in Fig.4.

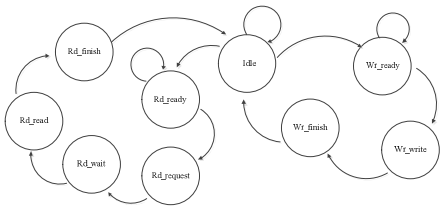

Figure 4. DDR3 read and write state machine

Fig.5 shows the read and write simulation results with Modelsim. At first, we do 10 times of consecutive burst write operations, and then do read operations, finally compare the data that be read and written.

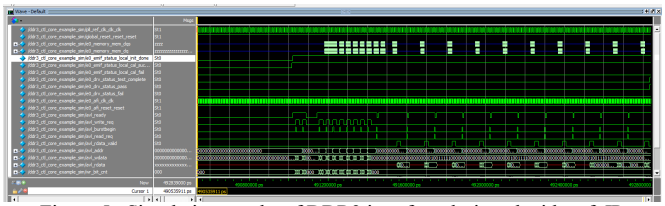

Figure 5. Simulation results of DDR3 interface designed with soft IP

It is required that the bandwidth on the Avalon side and the Memory side must be identical. As the DDR3 clock frequency is 300 MHz, the theoretical bandwidth of soft IP can be calculated to be $2\times32bit\times300MHz=19.2Gbps$.

When design with hard IP, MPFE act as a scheduler using the method of time division multiplexing to schedule the data and commands come from different ports. The simulation results of DDR3 interface designed with hard IP is shown in Fig.6.

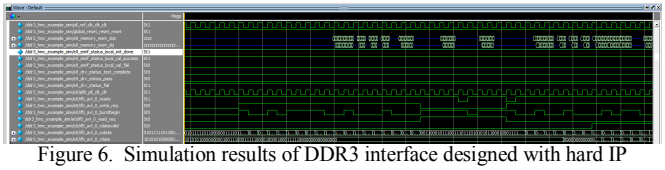

Figure 6. Simulation results of DDR3 interface designed with hard IP

From the simulation of the single port here, it can be seen that the DQ data bus has many free periods. The reason is that only one port was generated, therefore the schedule efficiency is not too high.The hard IP supports up to 400 MHz DDR3 clock frequency. The theoretical bandwidth can be calculated is $2\times32bit\times400MHz=25.6Gbps$.

IV. SYSTEM VERIFICATION

Set the sampling clock and the signal to be captured with the signalTap II logic analyzer to verify the inner signals of user interface, and then download the program to the DAQ board. The observed corresponding internal signals are shown in Fig.7. The data information read from DDR3 is displayed in the figure. As the data width is 128 bit, the figure only displays the signals of low byte.

Figure 7. The data information of user interface obtained by signalTap II

CONCLUSIONS

The Cyclone V soft and hard IP core for DDR3 respectively support the clock frequency up to 300 MHz and 400 MHz. In contrast, the hard IP has more advantages in terms of transmission rate, while the internal structure is more complex. It shows that the user customised DDR3 interface controller operates stably and reliably while accessing the storage module of the DAQ board. On the other hand, it verifies the reliability of hardware design on DDR3 memory with fly-by structure put forward in reference [3].

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