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Digital Assisted High-Order Multi-Bit Analog to Digital Ramp Converters

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***Abstract*—The concept of high-order ramp analog-to-digital converter and its design aiming at medium-high resolution (12-14 bits) are presented. Design methods that give rise to various Nyquist rate schemes resembling incremental converters are described. Since for Nyquist rate achieving noise shaping is not the goal, the design care is just maintaining good stability to avoid performance degradation. Different architectures for second and third-order ramp converters are presented and verified at the behavioral level. Simulation results show how the use of extra quantizers and multi-bit resolutions reduces integrators output swing and enhances overall performance. Finally, possible digital assistance actions are presented and discussed.**

I. Introduction

Instrumentation and measurement applications require monotonic analog-to-digital converters (ADCs) with high resolution and good linearity. Incremental converters, directly derived from $\Sigma\Delta$ schemes, are particularly suitable for those needs. Although showing the same structure of a $\Sigma\Delta$, the incremental ADC uses resets across each integrator of the architecture for erasing the history information at the beginning of each conversion cycle.

Since the reset prevents exploiting the information of past samples, there is no need to describe the quantization error as noise and to operate for giving rise to shaping of the quantization noise. Thus, indeed, an incremental converter is a Nyquist-rate type. The input is supposed constant during the entire conversion cycle, otherwise the digital converted output refers to a weighed average of input with an action that resembles the one of an input filter.

The incremental ADC concept based on high-order $\Sigma\Delta$ converters achieves very high resolution, [1], [2]. The use of feedforward paths leads to single digital-to-analog (DAC) schemes, thus avoiding possible limits caused by gain mismatch between DAC paths. However, if the modulator is 3rd-order or higher [1], the requirements of stability and high-order noise shaping reduce the resolution because it is necessary to use attenuations factors with different extents along the accumulating path.

This paper does not looks for noise shaping but just searches for architectures that have a limited swing at the output of sampled-data accumulators. The resulting schemes are named high-order ramp because that is the type of input waveform determined by a cascade of accumulators. There are many design options; an effective solution described below uses a digital filter assisted technique.

Depending on the resolution target, it is possible to employ multi-bit quantizers. The results are compact and potentially power efficient structures. The use of dynamic element matching (DEM), [3], or smart-DEM techniques moderates the limit of accuracy caused by unity element mismatch. The paper presents and studies at the behavioral level possible solutions for second and third order converters with single and multi-bit quantizers.

II. Incremental Converter Revisited

The incremental ADC was firstly introduced by van de Plassche in 1978, based on a $\Sigma\Delta$ architecture and implemented in bipolar technology [4]. In 1985, this concept was applied to a CMOS technology and, as far as we know, it is the first time that the term "incremental" was formally introduced, [5]. Fig. 1 shows a block digram of a 1st-order incremental ADC. This modulator consists of an integrator with one-clock-cycle delay, followed by a comparator and a 1-bit DAC along the feedback path.

At the beginning of a new conversion cycle, a periodical signal resets the output of the integrator. Supposing the input signal V_{in} constant, after N clock cycles, the residue value at the output of the integrator is

$$V_{res} = \sum_{i=1}^{N} V_{in}(i) - \sum_{i=1}^{N} V_{out}(i) \tag{1}$$

Since the loop filter is supposed to be stable, the value of V_{res} is limited within a limited range. The input signal can be, hence, estimated as follows

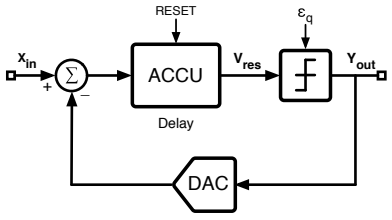

Fig. 1. A 1st-order incremental ADC.

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$$V_{in} = \frac{\sum_{i=1}^{N} V_{out}(i)}{N} - \frac{V_{res}}{N} \tag{2}$$

that gives the resolution 1st-order incremental scheme

$$R_{1-ord} = log_2(N). \tag{3}$$

The second term of the above equation gives the differential non-linearity

$$DNL = -\frac{V_{res}}{N} \tag{4}$$

it is lower than 1-LSB if the residual is less that the reference used by the DAC (the full scale of the converter).

Increasing the resolution requires augmenting the number of clock periods or using more effective schemes with cascade of accumulator, as done in high-order $\Sigma\Delta$. They become incremental converter by the simple addition of a reset of sampled-data integrators at the beginning of the conversion cycle. The key point is to increase the accumulation efficiency, while maintain the stability of conversion loop together with a minimized V_{res} [2] [6]. The maximum achievable resolution for a 2nd-order or 3rd-order modulator can be calculated as

$$R_{2-ord} = log_2 \frac{N(N+1)}{2!} + b_q \tag{5}$$

$$R_{3-ord} = log_2 \frac{N(N+1)(N+2)}{3!} + b_q \tag{6}$$

where b_q is the resolution of the quantizer and N is the number of conversion cycles.

An incremental converter can use a single or a multi-bit quantizer. With a single-bit quantizer, the modulator does not suffer from non-linearity of the DAC. Nevertheless, the modulator which uses a single-bit quantizer has a relatively large swings along the incremental paths and this may result in operational amplifiers working in slewing mode. The non-linearity of the multi-bit DAC can be compensated for with static or dynamic calibration methods. However, the well know DEM, [3], approach must be carefully considered. Its use in $\Sigma\Delta$ modulator achieves shaping of the spectrum of the mismatch error, but, as already stated, the incremental is a Nyquist-rate converter that does not increase the resolution with oversampling but just uses many clock periods to determine the conversion. Possible solutions to this issue are presented in [7], which uses an intrinsic linear DAC in a 2nd-order modulator, and in [8], where a smart dynamic element matching technique is proposed.

A $\Sigma\Delta$ architecture possibly uses distributed feedback and feedforward paths to make stable the loop. The errors in the feedforward coefficients affect the signal path and give rise to a signal error. Having a constant input signal ensures that the error is just a gain factor. Errors in feedback coefficients are more difficult to analyze because the feedback signal varies in time and with distributed feedback there are multiple injections.

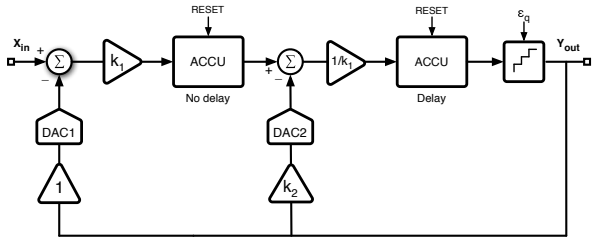

Fig. 2. A 2nd-order incremental ADC.

III. High-Order Ramp Converter

The above analysis of incremental converters determines indications on how to design optimal architectures. Results are high-order ramp converters, with possibly multi-bit quantizer, designed according to the following guidelines:

- The structure does not use analog feedforward paths which lead to extra analog blocks.
- The coefficients along the accumulation path should not decrease the resolution.
- There should be only one feedback path in which a DEM algorithm can be effectively used.

These guidelines lead to architectures in which digital filters perform digital assisted functions aimed at controlling the voltage swings at the output of the op-amp used. The following subsections describe architecture and features of possible schemes of high-order ramp converters.

A. The 2nd-Order Scheme

A second-order ramp converter is the cascade of two accumulators. As it happens for time-invariant schemes, it is necessary to control the cascade of more than one accumulator for keeping constrained the output of intermediate nodes. The request is not ensuring stability as needed in filters or $\Sigma\Delta$ architectures; however, since a similar action is required, the designer can take advantage of the method used in time-invariant schemes.

Second order $\Sigma\Delta$ architectures use an auxiliary injection at input of the second accumulator or employ feedforward branches toward the quantizer. The latter solution is not optimal, because for multi-bit schemes, it is necessary using extra analog efforts (and power) for adding the feedforward branches. The use of an auxiliary injection, as shown in Fig. 2, can be used at two purposes: optimize the output swing at the op-amp outputs or improve the feedback factor of integrators. There is an additional degree of freedom on the choice of the coefficients $k_1$and k_2. The real benefits are, indeed, limited. The use of $k_1 = 1/2$ and $k_2 = 0.75$ reduces the maximum swing of the op-amps by 15% and, obviously, improves the feedback factor of the second integrator, provided that the subtraction is performed with different SC circuits.

Fig. 3 shows an alternatively solution that avoids intermediate injection without feedforward paths. The use of a transversal filter and the proper choice of coefficients c_1 and c_2 control the signal swing of the two integrators. The choice

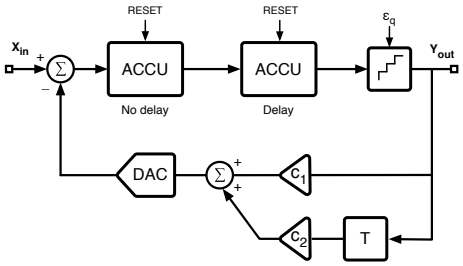

Fig. 3. A 2[nd]-order ramp ADC with 1-digital-feedback path.

of the coefficients can be done with the help of the z transfer function of the time-invariant equivalent.

The study in the z-domain gives rise to a denominator in the noise transfer function (NTF) and signal transfer function (STF) given by

$$D_2(z) = 1 + (c_1 - 2)z^{-1} + (c_2 + 1)z^{-2}. \quad (7)$$

The position of poles of the time-invariant counterpart inside the unity circle verifies stability. Moreover, their placement can bring about possible reduction of the op-amp swings.

Fig. 4 shows a third possible architecture. It uses two quantizers at the output of accumulators. The signal fed back at the input is the addition of the two digital outputs. The use of an extra quantizer is a limited cost because the power consumed by a comparator is much less than the one of an op-amp with same speed. Removing the intermediate injection improves the feedback factor of the second integrator, thus allowing to spare power.

The study of the time-invariant equivalent shows four zeros that are inside the unity circle if $k_1 < 1.5$. Simulations show that $k_1 = 0.75$ optimizes the variation of output swing at the input of the quantizer. Fig. 5 compares the output swings of an incremental converter (top), its version with k_1 and k_2 (see Fig. 2) (mid) and the scheme of Fig. 4 (bottom) with $k_1 = 0.8$ and $k_2 = 1$ (scheme of Fig. 3 does not grant benefits). The swing in the last case is almost half the one of the incremental converter. The waveform is around the input amplitude; however, simple circuitry enables an amplitude shift around zero. Therefore, a small swing corresponds to relaxed slewing request, low dynamic range and reduced number of comparators in the flash.

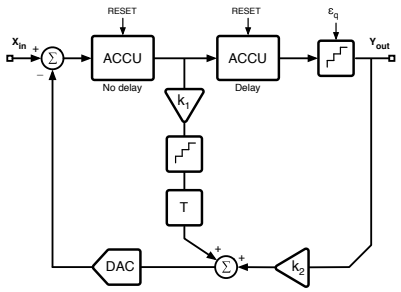

Fig. 4. A 2[nd]-order ramp ADC with two quantizers.

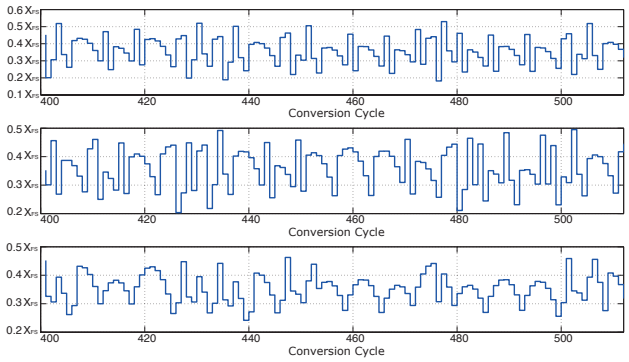

Fig. 5. Swing of the second integrator for three different second-order ramp converters. The input signal range is $\pm X_{FS}/2$.

B. The 3[rd]-Order Ramp ADC

Methods similar to the one discussed for the second-order ramp converter can be extended to higher order. Fig. 6 shows a 3[rd]-order ramp ADC scheme with single digital DAC and FIR filter along quantizer loop. The digital filter uses three taps with two delays. Parameters c_1, c_2 and c_3 of the filter can be critical for stability. The z transfer functions of the time-invariant counterpart has a denominator given by

$$D_3(z) = 1 + (c_1 - 3) + (c_2 + 3)z^{-2} + (c_3 - 1)z^{-3} \quad (8)$$

whose zeros must be in the unity circle.

Extensive simulations show that the choice of coefficients benefit the swing at the output of each integrator. With $c_1 = 3$, $c_2 = -3$ and $c_3 = 1$ there is an improvement with respect to the incremental counterpart of about 23%. The number of levels of the DAC remains unchanged but, as it happens for the incremental scheme, the DAC dynamic range must be larger than the input to accommodate the larger error due to the difficulty in controlling a cascade of three integrators.

Fig. 7 shows the block diagram of a 3[rd]-order ramp ADC with multiple quantizers. The strategy is more effective in controlling the integrator output voltages because there is a monitor of each of them. The resolution of the three ADCs is supposed to be the same.

The choice of the parameters k_1, k_2 and k_3 can give

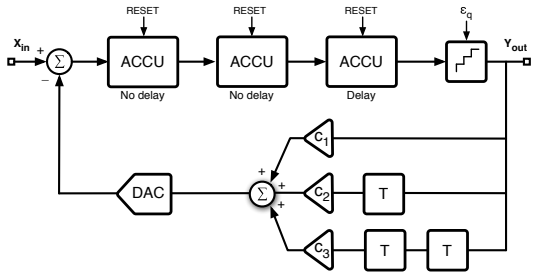

Fig. 6. A 3[nd]-order ramp ADC with 3-digital-feedback paths.

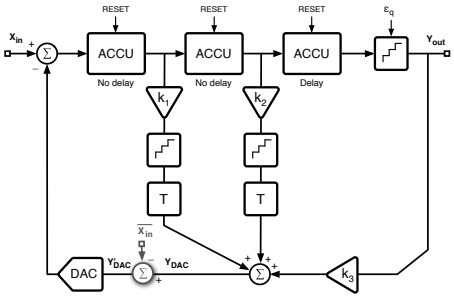

Fig. 7. A 3rd-order ramp ADC with three quantizers.

rise to unstable situations or reduce the swing at output of accumulators. The study of the time-invariant scheme outlines a denominator of the transfer functions whose zeros must be inside the unity circle. Simulations that change the parameters within the stability range identify the optimum set.

Notice that different values of the k parameters weight in a different manner the control of the accumulator outputs. Since a large swing in one of them affects the following, it is logical to assume $k_1 = k_2 = k_3$. Simulations with 3-bit ADCs give rise to minimum swings with $k_1 = k_2 = k_3 = 1$.

Fig. 8 compares the signal swing at the output of the third integrator for a conventional incremental converter (top) and the ramp converter of Fig. 7 (mid). It is the one with best results between the third-order ramp converters considered above. The obtained swing is less than 50% than the incremental counterpart. The bottom diagram of Fig. 8 reports the DAC signal. Despite the addition of three ADCs with three bits, the dynamic range of the DAC is not higher than the one of the incremental scheme. The reduction of the error at the output of the third accumulator gives rise to the room required by the errors at the output of the other accumulators. Moreover, overall limited swings require using a number of comparators that is less than the expected $3 \cdot 2^3$.

Remind that the output of the third accumulator after the last A/D conversion is a residual that, divided by the input amplification, measures the INL. The swing roughly indicates the DNL. Thus, the scheme of Fig. 8 ensures better INL and DNL than the incremental counterpart.

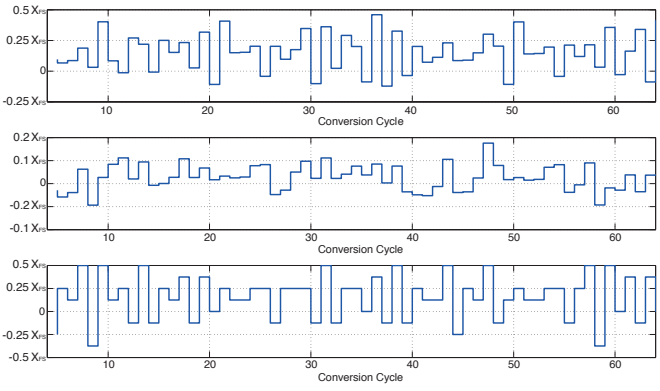

Fig. 8. Signal at the output of the third accumulator for a conventional 3rd-order incremental converter (top) and for the scheme of Fig. 7 (mid). Signal at the output of the DAC for the scheme of Fig. 7 (bottom). The input signal range is $\pm X_{FS}/2$.

IV. Digital Assisted Actions

The operation of the proposed high-order ramp converters, in addition to the foreseen processing, can be suitably assisted with a number of actions. They concern the digital measure of mismatches, digital calibration and the shift of signals to keep them in the most effective region.

An architecture with limited output swing in the integrators improves the overall performances.That result is naturally achieved by multi-bit quantizers that limit the error in the signal estimation. However, there are two key problems: the linearity of the DAC that must be better than the overall resolution; the need of shifting signals around the quiescent amplitude. The first issue involves the measure of the mismatch, possibly done in a foreground fashion using the converter itself. The digital measures of the mismatch, stored in a memory, are the input of a digital calibration. The method is a good alternative to the dynamic matching used in multi-bit $\Sigma\Delta$ modulators because the DEM technique is not for Nyquist-rate converters.

A level shift at the input of the flash results if the input of the DAC is

$$Y'_{DAC} = Y_{DAC} - \overline{X_{in}} \tag{9}$$

where $\overline{X_{in}}$ is a quantized version of input. This is done with the added gray subtractor of Fig. 7. Since the input is constant for the entire conversion cycle, its quantization can be performed before starting the conversion cycle. The conversion is done at zero cost by one of the two ADCs used by the architecture and stored in a temporary memory.

Acknowledgment

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