LETTER

A New Analog-to-Digital Converter BIST Considering a Transient Zone

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SUMMARY A new BIST (Built-in Self-test) method for static ADC testing is proposed. The proposed method detects offset, gain, INL (Integral Non-linearity) and DNL (Differential Non-linearity) errors with a low hardware overhead. Moreover, it can solve a transient zone problem which is derived from the ADC noise in real test environments.
key words: *static ADC built-in self-test, transient zone problem*

1. Introduction

Histogram method is one of the most popular test techniques for ADC testing [1]. With the histogram method, the test parameters can be acquired easily but long test time and additional area overhead are required. In [2], a new BIST structure is presented that compares the outputs of ADC with those of the reference counter without memory modules to reduce the hardware overhead and test time. However, it still has redundant area and a transient zone problem introduced below.

In a real ADC, output codes which zigzag up and down can be found near a transition from one code to the next, as illustrated in Fig. 1. When the input of an ADC is close to a decision level, the uncertainty exists in output codes caused by random noise [3]. For instance, it is possible to achieve an ADC output sequence 2, 2, 2, 2, 3, 2, 3, 3, 3 rather than the ideal sequence 2, 2, 2, 2, 3, 3, 3, 3, 3. The unintended transitions form a transient zone. This may affect the accuracy of the testing and cause wrong test result.

In the proposed BIST structure, an advanced transition detector is adopted to solve a transient zone problem. Furthermore, the detection and calculation modules are optimized to decrease the area overhead. The structure and simulation result of the proposed BIST scheme will be shown in the remainder of this paper.

2. Proposed Method

Figure 2 shows the block diagram of the proposed BIST. In test mode, a ramp signal is selected as a test input and its output is generated ($D_{n-1} \sim D_0$). The proposed response analyzer uses only lower 2-bit (D_1, D_0) of the ADC's output. With internal signals, INL/DNL detectors determine the static parameters of the ADC.

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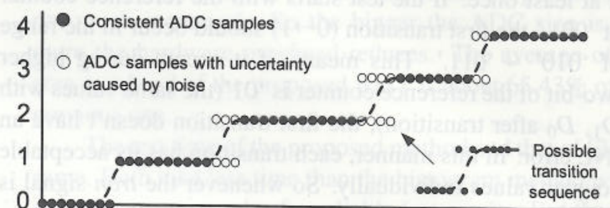

Fig. 1 Occurrence of the transient zone.

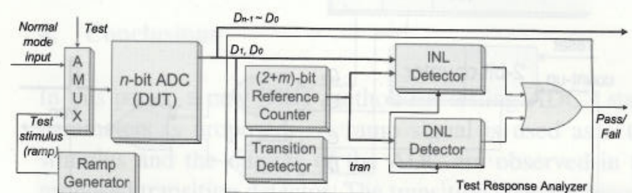

Fig. 2 The block diagram of the proposed method.

2.1 The Transition Detector

In [2], the transition detector watches the lowest bit only to detect transitions. If we consider a transient zone, however, it may unintentionally activate the *tran* signal too many times because a transient zone has several unintended transitions, as shown in Fig. 1. The *tran* signal should be activated once at each decision level because [2] determines the static parameters with the points of time and intervals of the activations. The proposed transition detector is designed to have immunity from a transient zone. A 2-bit up-counter is used for comparison and the *tran* signal is activated only when the 2-bit counter (C_1, C_0) and lower 2-bit (D_1, D_0) of the ADC have the same values. Its structure and the detecting procedure are shown in Fig. 3 and Fig. 4.

Initially, the 2-bit counter is set to '01' and waits for the first transition (D_1, D_0 = '01'). When the first transition occurs, the *tran* signal is activated and the counter performs a count. Then the counter is now '10' and waits for the second transition (D_1, D_0 = '10'), so '00' ↔ '01' transitions does not activate the *tran* signal. In this way, the proposed transition detector activates the *tran* signal once at each decision level.

2.2 The INL Detector

INL is concerned with the elapsed time since a test start for

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each transition. With the *tran* signal generated by the proposed transition detector, the INL detector decides whether the transition occurred within the given acceptable range. As shown in Fig. 2, a (2+*m*)-bit reference counter is used to provide timing references. (*m* is determined by the INL/DNL acceptable range.)

Figure 5 shows the acceptable range of INL when the acceptable range is ± 1/2 LSB. In this case, the minimum required value of *m* is 1 because we should divide 1 LSB by 2 at least once. If the test starts with the reference counter at '001,' the first transition (0→1) should occur in the range of '010' ~ '011.' This means, if it occurs during higher two-bit of the reference counter is '01' (the same values with D_1, D_0 after transition), the first transition doesn't have an INL error. In this manner, each transition has its acceptable counter values individually. So whenever the *tran* signal is activated, the INL detector checks if the activation is made in proper time, not early or late.

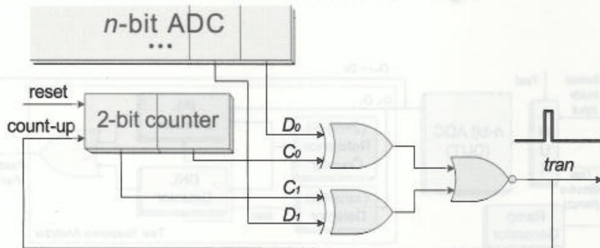

Fig. 3 The structure of the transition detector.

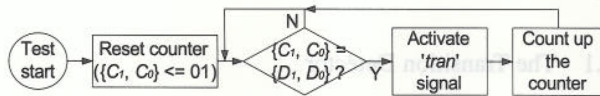

Fig. 4 The procedure of the transition detector.

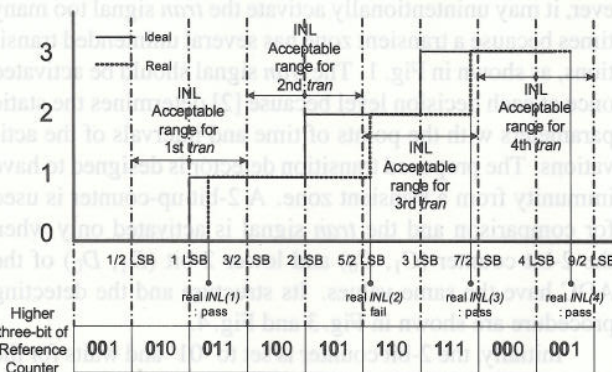

Fig. 5 The acceptable range of INL.

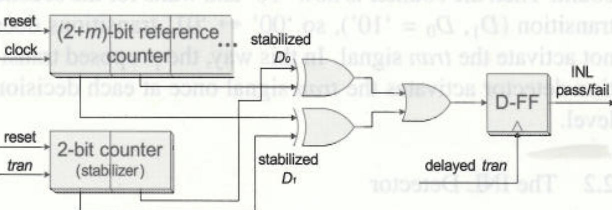

Fig. 6 The structure of the INL detector.

Figure 6 shows the schematic of the INL detector when the acceptable range is ± 1/2 LSB. The structure and the operations are similar to [2], but the proposed INL detector has a (2+*m*)-bit reference counter instead of a (*n*+*m*)-bit one. (*n* means the ADC size.) To stabilize the ADC output, a 2-bit counter is adopted. D_1, D_0 from ADC are not compatible for comparing the values because they have transient zones. The 2-bit counter performs an up-count whenever the *tran* signal is activated. Then the stabilized D_1, D_0 have the same values with D_1, D_0 from ADC, but without transient zones. When the *tran* signal is activated, stabilized D_1, D_0 are changed and compared with the higher two-bit of the reference counter. While they are the same, the output of the INL detector remains 0. Comparing only the lower 2-bit can determine the INL because the proposed transition detector guarantees that every transition means upward one. Moreover, gain and offset can be acquired with the first and the last INL values because they concern with the slope and the starting point of the ADC output.

2.3 The DNL Detector

In this paper, we used the same DNL detector as [2]. Both [2] and the proposed method use the *tran* signal and the reference counter, so the same DNL detector can be adopted. In [2], the DNL detector uses lower *m*-bit of the reference counter to determine DNL. Therefore, it does not effect the result whether we use the same DNL detector with a (2+*m*)-bit reference counter. The required value of *m* is also same as [2], then *m* has to be chosen for the larger value between the needed *m* from INL/DNL detectors.

3. Experimental Results

The experiments are made with simulations of a 12-bit flash ADC and performed independently for the transition/INL detectors only because the DNL detector has the same structure as [2].

To test the proposed transition detector, some unnecessary transitions were added intentionally because a transient zone is shown in real ADC but not in simulation. Figure 7 shows the waveforms of the previous and proposed transition detectors with transient zones.

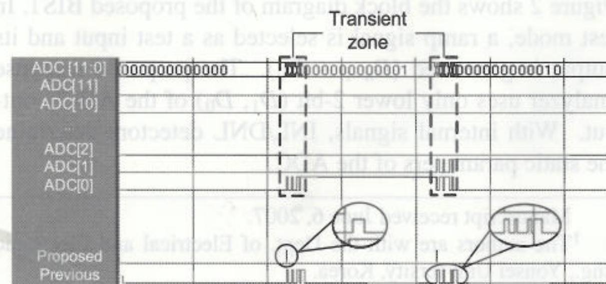

Fig. 7 Waveforms of the previous and proposed transition detectors.

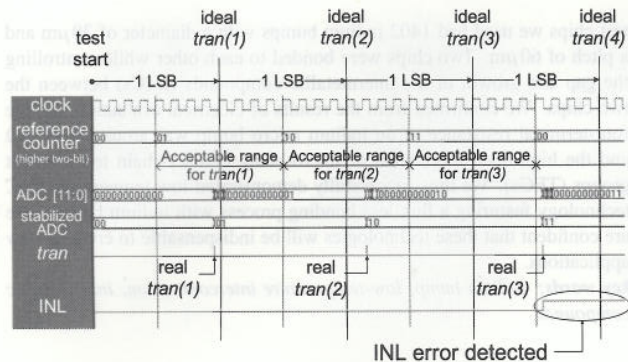

Fig. 8 Waveform of the proposed INL detector.

Table 1 The comparison of the hardware overhead.

		Previous method [2]			
		T.D.	I.D.	D.D.	Total
8-bit pipeline ADC	± 1/2 LSB	8.25	129.25	29.25	**166.75**
	± 1/4 LSB	8.25	141.50	38.50	**188.25**
	± 3/8 LSB	8.25	154.75	100.50	**263.50**
12-bit flash ADC	± 1/2 LSB	8.25	180.25	29.25	**217.75**
	± 1/4 LSB	8.25	192.50	38.50	**239.25**
	± 3/8 LSB	8.25	205.75	100.50	**314.50**
Average		8.25	167.33	56.08	**231.67**

		Proposed method			
		T.D.	I.D.	D.D.	Total
8-bit pipeline ADC	± 1/2 LSB	18.50	63.75	29.25	**111.50**
	± 1/4 LSB	18.50	77.25	38.50	**134.25**
	± 3/8 LSB	18.50	90.00	100.50	**209.00**
12-bit flash ADC	± 1/2 LSB	18.50	63.75	29.25	**111.50**
	± 1/4 LSB	18.50	77.25	38.50	**134.25**
	± 3/8 LSB	18.50	90.00	100.50	**209.00**
Average		18.50	77.00	56.08	**151.58**

In the previous transition detector, undesired activation of the *tran* signal occurs because of the unnecessary transitions in the transient zone. They can disturb the test results because the INL/DNL detectors check the nonlinearities whenever the *tran* signal is activated. The proposed transition detector holds the current state in a register, so it can distinguish the genuine transition. Therefore, though the proposed transition detector requires more hardware overhead than the previous one, it gives more reliable test results.

With this *tran* signal, the INL/DNL detectors check the static parameters. The simulation result of the INL detector is shown in Fig. 8.

Table 1 shows the hardware overhead of the proposed three detectors and the previous ones. For each 8-bit and 12-bit ADC, the acceptable ranges of ± 1/2, ± 1/4 and ± 3/8 LSB are considered. According to the given ranges, the size of the reference counter and comparing logic is changed. T.D./I.D./D.D. mean the transition/INL/DNL detector respectively.

The proposed transition detector is larger than the previous one but its size is relatively small and not influenced by the resolution of the ADC or the acceptable range. The hardware overhead of the previous INL detector varies because the size of the reference counter is determined by the size of the ADC. However, the size of the proposed one is not much increased. So the bigger the ADC size is, the more the hardware overhead reduces. The average of the area overhead of the proposed BIST is about 65.43% of the previous one.

The test time of the proposed method and that of [2] are same. Both take less time than the histogram method which requires many samples for reliable test results. But the proposed method and [2] can test the static parameters faster with the points of time and intervals of ADC's transitions.

4. Conclusions

In this paper, a new BIST method for testing ADC's static parameters is proposed. A ramp signal is used as a test stimulus and the outputs of the ADC are observed in the proposed transition detector. The transition detector ignores unnecessary transitions in a transient zone then activates the *tran* signal correctly. After that, the *tran* signal is transmitted to the INL/DNL detectors. They calculate the static parameters such as offset, gain, INL and DNL with the *tran* signal. The proposed method has immunity to a transient zone and less hardware overhead than the previous method.

Acknowledgments

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