Design of Low Power CMOS Crystal Oscillator with Tuning Capacitors

Shun Yao, Hengfang Zhu, Xiaobo Wu

Abstract—A low power CMOS crystal oscillator was proposed with high accuracy by tuning capacitors. Based on the analysis concerning power consumption, start-up time, and frequency stability of the crystal oscillator, an amplitude regulation circuit was employed to limit the current consumption. Simulation results showed the measured currents of 27 µA and 20 µA with and without the output stage under 1.5 V supply voltage, respectively.

Index Terms—amplitude regulation, low power, quartz crystal oscillator.

I. INTRODUCTION

Crystal oscillators are widely used to generate precise frequency standards for integrated electronic systems. Due to the continually increasing demands for the portable instruments, high performance crystal oscillators are embedded on the silicon chip where power supply is limited and frequency precision is of some concern. Furthermore, for the miniaturized portable devices, low power consumption is always a crucial requirement, which leads to the major consideration of this proposed crystal oscillator. In this paper, a low power CMOS crystal oscillator was realized with high accuracy through tuning the switched-capacitor banks.

In Section 2, the theoretical analysis of quartz crystal oscillators is presented and explored to clarify the start-up conditions for crystal oscillators, as well as the power consumption and the start-up time. Then, Section 3 gives one practical CMOS implementation of a crystal oscillator under low power and high accuracy consideration. And the simulation results are illustrated in Section 4. A final summary and further discussion follows in Section 5.

Shun Yao is with the Institute of VLSI Design, Zhejiang University Hangzhou, 310027, China, (phone: +86 571 87952047; fax: +86 571 87952486; e-mail: yaoshun@vlsi.zju.edu.cn).
Hengfang Zhu is with the Institute of VLSI Design, Zhejiang University Hangzhou, 310027, China, (e-mail: zhuhf@vlsi.zju.edu.cn).
Wu Xiaobo is with the Institute of VLSI Design, Zhejiang University Hangzhou, 310027, China, (e-mail: wuxb@vlsi.zju.edu.cn).

II. THEORETICAL ANALYSIS OF QUARTZ CRYSTAL OSCILLATORS

A. General Analysis

Among the various possible implementations of the basic three-point oscillator, the grounded source configuration, also called the Pierce oscillator, is preferred for high-precision oscillators [7]. The most common Pierce oscillator block is depicted in Fig. 1. Generally, the quartz crystal resonator can be represented as a series resonant branch of R_s, C_s, L_s, and a shunt capacitor C_p. The load capacitors C_1 and C_2 transform the g_m of the gain element into a negative equivalent resistance R_{com} and can be utilized to modulate the resonant frequency f_{osc}.

$$f_{osc} = \frac{1}{2\pi\sqrt{L_s \dfrac{C_s C_t}{C_s + C_t}}} \tag{1}$$

Here, C_t represents the total parallel capacitance to the resonator.

$$C_t = C_p + \frac{C_1 C_2}{C_1 + C_2} \tag{2}$$

An optimum method is employed for the detailed analysis [7] by splitting the whole oscillator into the linear motional impedance Z_m and the rest part of the circuit Z_c, as shown in Fig. 3, in which Z_c includes capacitances C_1, C_2 and C_p of the resonator and all the nonlinearities. Thus, the critical
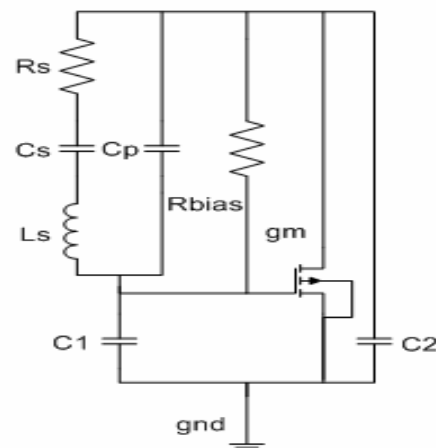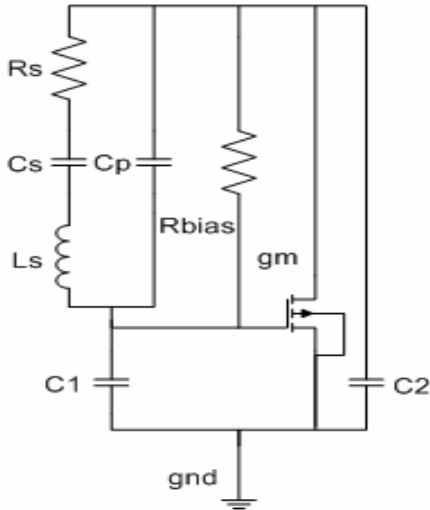

Fig. 1 Basic Pierce Oscillator Scheme

Fig. 2 Basic Pierce Oscillator Scheme

Fig. 3 Optimum Splitting for Analysis

Fig. 4 AC Diagram of Pierce Oscillator

Fig. 5 Complex Plane Representation of Loci $Z_c(g_m)$ and $-Z_m(p)$

condition for oscillation can be simply expressed as

$$Z_c + Z_m = 0 \tag{3}$$

The approximate expression for the motional impedance Z_m is presented below:

$$Z_m = R_s + j\frac{2p}{\omega C_s} \tag{4}$$

where p is the relative amount of frequency pulling above the mechanical resonant frequency ω_m of the resonator.

$$p = \frac{\omega - \omega_m}{\omega_m}(\ll 1) \tag{5}$$

Therefore, the real and imaginary components of Z_c should satisfy the following equations.

$$\begin{cases} -\operatorname{Re}(Z_c) = R_s \\ -\operatorname{Im}(Z_c) = \frac{2p}{\omega C_s} \end{cases} \tag{6}$$

As soon as $-\operatorname{Re}(Z_c)$ becomes larger than R_s, the oscillation will build up exponentially from noise.

The AC diagram of the most general Pierce oscillator is illustrated in Fig. 4. Impedance $Z_1 \sim Z_3$ include all the possible
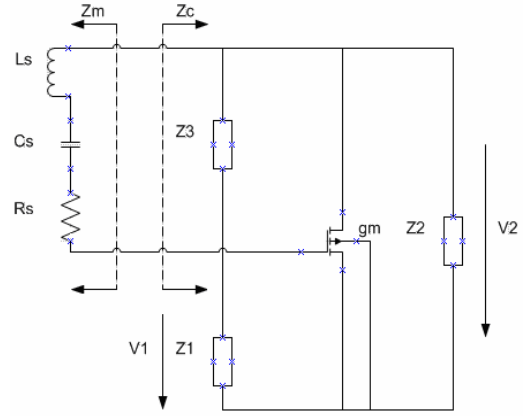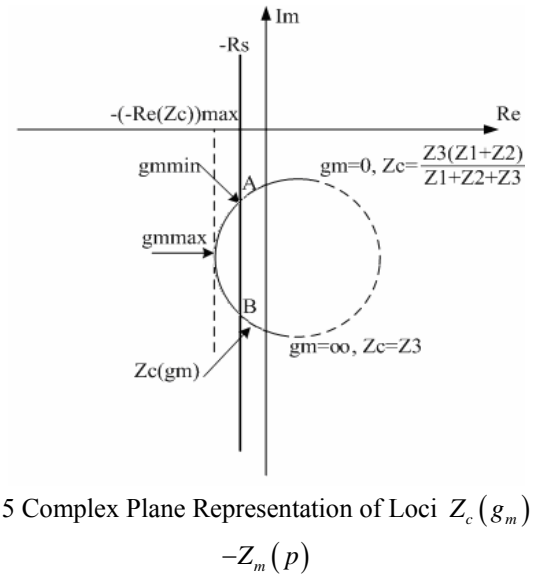
contributions except the g_m of the active device. By using the Thevenin Equivalent, the small-signal impedance of Z_c can be obtained as

$$Z_c = \frac{Z_1 Z_3 + Z_2 Z_3 + g_m Z_1 Z_2 Z_3}{Z_1 + Z_2 + Z_3 + g_m Z_1 Z_2} \tag{7}$$

Since Z_c is a bilinear function of g_m, the locus of Z_c at g_m values from zero to infinite is half a circle in the lower half of the complex circle, as shown in Fig. 5. The critical condition for oscillation to start up correspond to the intersections A and B of this locus with that of $-Z_m(p)$ [6]. For all values of g_m where $Z_c(g_m)$ lies between the A and B, the crystal oscillation will occur. Thus, the values of both $g_{m,\min}$ and $g_{m,\max}$ can be derived from the combination of (6) and (7).

The negative resistance $-\operatorname{Re}(Z_c)$ reaches a maximum for an intermediate value of $g_{m,opt}$, which should be greater than the motional resistance R_s for oscillation to start. Besides, the start-up time of CMOS oscillators is influenced by g_m [4]. The time constant τ of the exponential amplitude growth of

oscillation is given as [4].

$$\tau = -\frac{2L_s}{R_s + \text{Re}(Z_c)} \qquad (8)$$

In the meantime, the start-up time is also proportionate to the bias resistor R_{bias}, the shunt capacitor C_p, and the voltage ratio V_T/V_{DD} [4]. According to (8), the start-up time, which is usually comprised between 5τ to 15τ, attains a minimum for $g_{m,opt}$. Furthermore, Fig. 5 provides qualitative insight of the influence of $Z_1 \sim Z_3$ on the frequency stability, which is discussed in detail in [7].

B. Lossless Circuit

To achieve minimum trans-conductance and maximum frequency stability, all the losses except for the resonator should be minimized. Fig. 6 represents the ideal case with purely capacitive impedances $Z_1 \sim Z_3$ (neglect the R_{bias}). Then, the real and imaginary components of Z_c become

$$\begin{cases} \text{Re}(Z_c) = -\dfrac{g_m C_1 C_2}{(g_m C_3)^2 + \omega^2 (C_1 C_2 + C_2 C_3 + C_1 C_3)^2} \\[3mm] \text{Im}(Z_c) = -\dfrac{g_m^2 C_3 + \omega^2 (C_1 + C_2)(C_1 C_2 + C_2 C_3 + C_1 C_3)}{\omega\left((g_m C_3)^2 + \omega^2 (C_1 C_2 + C_2 C_3 + C_1 C_3)^2\right)} \end{cases} \quad (9)$$

The maximum negative resistance can be achieved by solving $\dfrac{d\,\text{Re}(Z_c)}{dg_m} = \infty$ for

$$g_{m,opt} = \omega\left(C_1 + C_2 + \frac{C_1 C_2}{C_3}\right) \qquad (10)$$

$$\left(-\text{Re}(Z_c)\right)_{\max} = \frac{1}{2\omega C_3 \left(1 + \dfrac{C_1 + C_2}{C_1 C_2} C_3\right)} \qquad (11)$$

If there is large enough margin between $\left(-\text{Re}(Z_c)\right)_{\max}$ and R_s, the minimum $g_{m,min}$ point A stays very close to the imaginary axis, which gives the following expression for
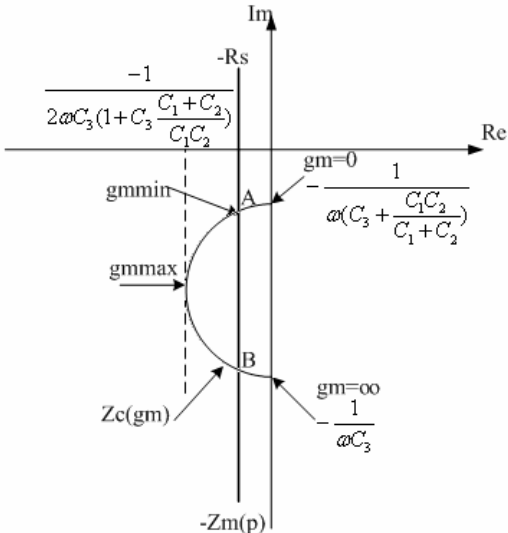

Fig. 6 Complex Plane Representation of Lossless Oscillator Condition

frequency pulling p with $g_m \to 0$.

$$p = \frac{C_s}{2\left(C_3 + \dfrac{C_1 C_2}{C_1 + C_2}\right)} \qquad (12)$$

By introducing (9) into (6), the minimum trans-conductance can be derived under the same assumption $g_m \to 0$.

$$g_{m,min} = \frac{\omega}{Q C_s} \cdot \frac{(C_1 C_2 + C_2 C_3 + C_1 C_3)^2}{C_1 C_2} \qquad (13)$$

Here, Q is the quality factor of the resonator.

$$Q = \frac{1}{\omega_m C_s R_s} \qquad (14)$$

Combining (12) and (13) illustrates the trade-off between the power consumption and the frequency stability.

$$g_{m,min} = \frac{\omega C_s}{Q p^2} \cdot \frac{(C_1 + C_2)^2}{4 C_1 C_2} \qquad (15)$$

with $C_1 = C_2$ to obtain minimum g_m under certain p, or minimum p under certain g_m.

C. Nonlinear Analysis

When the applied DC bias current I is above the critical value I_{crit}, the minimum trans-conductance $g_{m,min}$ is exceeded for oscillation to start up. Nonlinearity begins to appear when the amplitude of the sinusoidal driving voltage on the active device becomes so large that harmonic frequency is generated in the output current i_D. Such nonlinear behavior by distortion not only causes power inefficiency, but also degrades frequency stability [7].

$$P_{\max} < \frac{2 Q C_s}{\omega C_{load}^2} I^2 \qquad (16)$$

Above is the estimation of the maximum power dissipated in the resonator.

These problems can be eliminated by limiting the amount of distortion to acquire high performance. Theoretically, restricting the bias current just above the critical condition for oscillation to build up would make the most efficient power consumption and excellent frequency stability. However, due to the variation in the process, as well as the resonator and the environment, the oscillation may not attain the minimum g_m to start up. Therefore, enough margins should be remained to achieve reliable function. In addition, if the g_m during start-up period can be greater than the critical value; the oscillation would be built up rapidly to meet specific requirement for start-up time.

III. PRACTICAL CMOS IMPLEMENTATION

A. Oscillator Block

A possible practical CMOS implementation of the Pierce oscillator is illustrated in Fig. 7. The gain element is realized by means of an NMOS transistor biased in the active region. Although using an inverter can supply larger g_m than a single
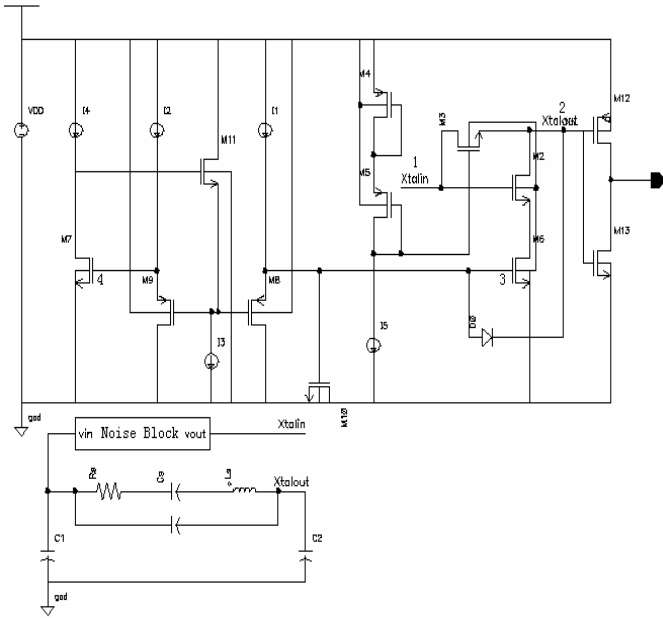
Fig. 7 Simplified Scheme of A Possible CMOS Implementation of Pierce Oscillator

transistor when biased with the same current, the inverter based implementation can also introduce some problems. First, the current consumption increases with the amplitude of oscillation, which results in strong nonlinear effects and huge waste of power. Second, since the capacitor C_n which grounds the source of the NMOS for AC signals cannot be infinite, the locus of Z_c would be distorted. In the vicinity of the imaginary axis, the slope of the tangent to the Z_c locus is increased, that means the frequency stability is therefore degraded. Therefore, the preferred solution employs a single NMOS transistor biased by a current mirror for the active element.

The bias resistor R_{bias} is implemented by a transistor M_3 operating in the weak inversion [8]. Its value should be high enough for the sake of frequency stability and power consumption. Moreover, the start-up condition can be satisfied more easily due to larger bias resistor [6]. In this realization, R_{bias} is around $100\,M\Omega$ by the biasing transistors M_4 and M_5.

In the case of a rail-to-rail sine wave, an interface amplifier is necessary to produce logic signal output. In order to realize low power consumption, the W/L ratio of this inverter should be optimized for high slew rate, low shoot-through current and etc.

B. Amplitude Regulation

An amplitude regulation circuit is employed to reduce g_m of the NMOS transistor when the amplitude of oscillation exceeds the critical value. Therefore, the crystal oscillator can operate close to the critical condition for oscillation, and avoid distortion of the sine wave to reduce power consumption. According to Fig. 7, the trans-conductance can be modulated through regulating the voltage at node 3. During the start-up period, the amplitude of oscillation at node 2 is relatively small and thus the diode is reversely biased. Through the accurate

matching between I_1 and I_2, and between M_8 and M_9, the voltage at node 3 will be equal to the voltage at node 4. As a result, the bias current of the NMOS is related to the reference current I_4 by the ratio $W_6/L_6 : W_7/L_7$. This guarantees a well-defined g_m which is independent of supply voltage during the start-up period. Since the oscillation builds up, the diode will eventually become forward biased at the bottom peak of oscillation. Thus, the voltage at node 3 drops to low level and thereby causes the g_m to decrease. The transistors M_8 and M_9 are biased in the sub-threshold region to ensure that M_8 is turned off sharply when the voltage at node 3 starts to drop. As a result, all the current I_1 will flow through the diode in equilibrium. To minimize the disturbance to the output signal, I_1 should be very low. Here M_{10} serves as a capacitor to form a first-order integrating function with the large impedance of M_8. Finally, the amplitude of oscillation has been regulated since the lower extremes of the sine wave are restrained to be equal to the voltage at node 3 minus the forward voltage of the diode. In order to realize symmetric output signal of the NMOS without any distortion, the V_{gs} of M_6 should be slightly higher than the sum of the forward voltage of the diode and the drain voltage of M_6 under equilibrium condition. Therefore, the power consumption of the harmonics introduced by nonlinear behavior is quite low due to the reduction of the g_m in the NMOS transistor.

C. Frequency Trimming

When the frequency accuracy is a requirement for some applications, the resonant frequency can be trimmed by tuning capacitor banks. Since the resonant frequency f_{osc} is related to the load capacitors C_1 and C_2 as (1) reveals, conventional Pierce oscillator utilizes two identical capacitor banks to accomplish variable load capacitance. Fig. 8 presents an "on chip" realization of tuning capacitors, which adjusts the total capacitance through switching on and off parts of the bank by means of transmission gates. Every stage of this structure
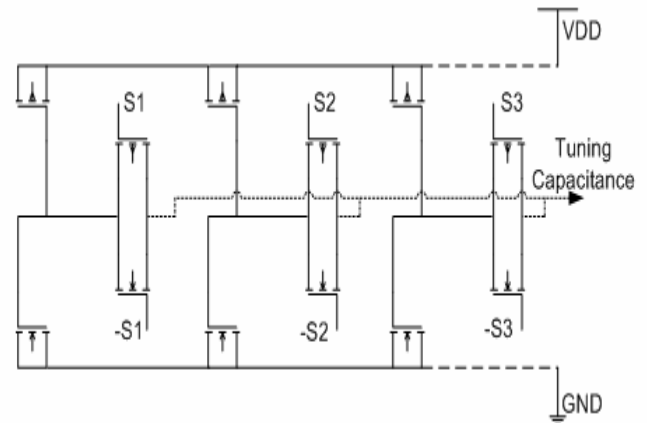

Fig. 8 Tuning Capacitance Scheme

consists of both a PMOS transistor connected to V_{DD} and an NMOS transistor connected to V_{SS} in order to reduce voltage dependency of these capacitors. The on-resistance of the transmission gates is introduced directly into the resonant loop, causing the losses to increase and thus the g_m required for oscillation to rise. When the dimensions of the switches are kept large for low losses, the stray capacitance becomes a problem to the accurate calculation of load capacitance. Therefore, this is another tradeoff between the power consumption and the frequency accuracy.

IV. SIMULATION RESULTS

A 10 MHz crystal oscillator was simulated in a 0.35-µm standard CMOS process under Cadence simulation environment. The electrical equivalent parameters of the crystal resonator were summarized in Table I . Both of the load capacitors C_1 and C_2 were 10pF, and a 1.5 V supply voltage was used. Fig. 9 shows the simulation result of the logic output signal. The measured current consumption with and without the output stage was 27 µA and 20 µA, respectively. It was indicated that the output stage contributes significantly to the total current consumption.

Table I Parameters of Crystal Resonator

Parameter	Symbol	Value	Unit
Frequency	$\omega/2\pi$	10	MHz
Motional Resistance	Rs	50	Ω
Motional Capacitance	Cs	2	fF
Shunt Capacitance	Cp	2	pF
Quality Factor	Q	1.6	10^5

V. CONCLUSION

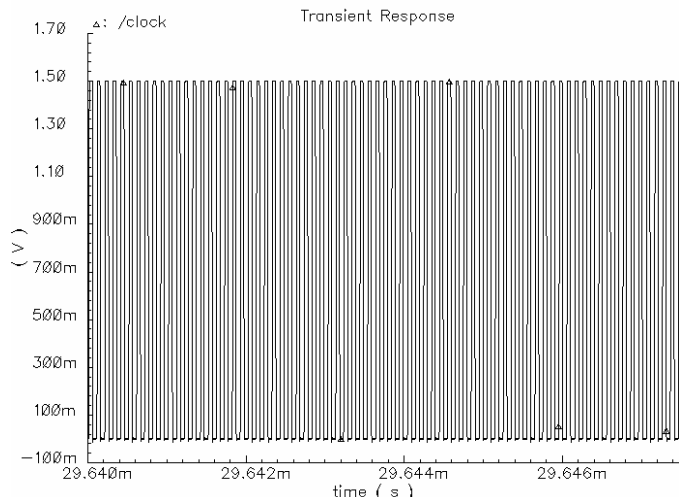Various characteristics of the crystal oscillator including power consumption, start-up time, and frequency stability were analyzed with respect to the trans-conductance g_m of the active device. A practical CMOS implementation of the Pierce oscillator was realized with high accuracy through tuning the switched-capacitor banks. Due to the amplitude regulation circuit, total current consumption was limited to 27 µA and 20 µA with and without the output stage, respectively.

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Fig. 9 Logic Output Signal