20 GHz High Performance VCO Design Methodology

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***Abstract*—The design and analysis of fully integrated Voltage Controlled Oscillators (VCO) for 20 GHz low cost and low power communication system is presented in this paper. Our work is based mainly on the optimization of phase noise and buffer stage specifications. SiGe:C heterojunction bipolar transistors of f_T=55 and 200 GHz have been used and produced with a monolithic BiCMOS technology.**

***Index Terms*—Heterojuntion bipolar transistors, MMICs, phase noise, SiGe BiCMOS, voltage controlled oscillator (VCO).**

I. Introduction

It is well known that full integration in a standard process is a key point for the design of modern telecommunication systems. An important microwave function in transceiver is the millimeter wave generation. However, there is no generic method to design a low phase noise oscillator. Usually people use their home made "know how" and the low phase noise character is only achieved through some prototype that is difficult to reproduce for an industrial implementation. Moreover, oscillator features such as power consumption, output power, tuning range are very important and are optimized, too. It is then very important to research methods to develop a generic method that will permit to obtain a good accuracy of integrated circuit design.

In this paper, we present a full analysis and a design methodology of 20 GHz low phase noise VCO using a 200-GHz-f_T BiCMOS SiGe:C [1] and a 0.25µm 55-GHz-f_T BiCMOS SiGe:C technology, developed by ST Microelectronics. Possible applications include the broad band optical fibre reception circuits with 20Gb/s and 40Gb/s or the broadband transmissions by satellites and radars in Ka band (20/30GHz).

II. HICUM Model

This section presents in a detailed way the transistor modeling for both technologies. However, only the results related to the transistors of 200-GHz-f_T BiCMOS SiGe:C technology are deferred here.

HICUM [3] (fig. 1) is an advanced model intended for high frequencies applications. The equivalent circuit of HICUM model considers all important physical effects for the current processes of bipolar technologies. The conception of high speed digital and analog circuits requires an exact description of the loads, the capacitances and also of transit time compared to polarization (I_C, V_{CE}).

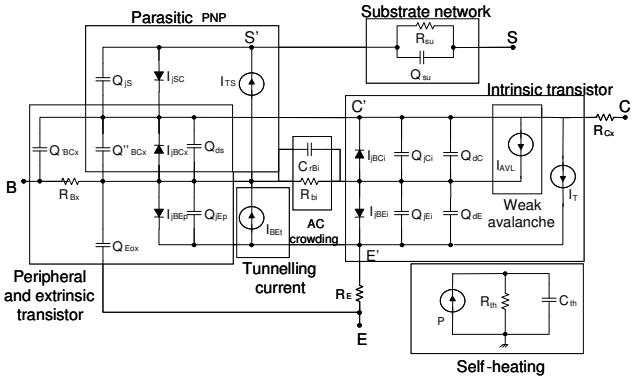


Fig. 1 Electric diagram of HICUM model

The transfer current of a homo or hetero-junction vertical transistor can be described by a general form ICCR (Integral Control of Charges Relation):

$$i_T = \frac{c_{10}}{Q_{p,T}}\left[\exp\left(\frac{v_{B'E'}}{V_T}\right) - \exp\left(\frac{v_{B'C'}}{V_T}\right)\right] = i_{Tf} - i_{Tr} \qquad (1)$$

where the constant C_{10} is expressed as

$$c_{10} = (qA_E)^2 V_T \overline{\mu_{nB} n_{iB}^2} \qquad (2)$$

and where $V_{B'E'}$ and $V_{B'C'}$ are the tensions (depending on the time) in the transistor terminals if the flow of charge variation holes $Q_{p,T}$, is carried out between its transmitter and its collector. $\overline{\mu_{nB} n_{iB}^2}$ is the average value of the base area.

The depletion capacities values and the transit time of mobile carriers and of the associated charges, which determine the dynamic behavior, are considered basic quantities in the model. The depletion capacitance base emitter with forward bias consists of a classic part, an average and a strong bias component

$$C_{jEi} = \frac{C_{jEi0}}{\left(1 - v_j / V_{DEi}\right)^{z_{Ei}}} \cdot \frac{e}{1+e} + a_{jEi} C_{jEi0} \frac{1}{1+e} \qquad (3)$$

with $$e = \exp\left(\frac{V_f - v_{B'E'}}{V_T}\right) \quad (4)$$

and the auxiliary tension $v_j = V_f - V_T \ln[1+e] < V_f \quad (5)$

where V_f is the voltage in which the capacitance of the classic expression (at strong forward bias) intercepts the maximum constant value. The base collector junction is normally polarized inversely. If the internal tension $v_{B'C'}$ exceeds the rupture voltage, the epitaxial region of collector becomes completely exhausted. The depletion capacitance is constituted of three components:

$$C_{jCi} = C_{jCi,cl} + C_{jCi,PT} + C_{jCi,fb} \quad (6)$$

where $C_{jCi,cl}$ represents the part due to average bias, $C_{jCi,fb}$ is the part due to maximum bias and $C_{jCi,PT}$ represents the strong bias component around and beyond rupture. In addition, all the basic model parameters as the capacitances and the transit time are easily measured with the standard equipment and methods of parameters extraction.

A. Parameter extraction

Reference [1] gives the DC and HF measurements of a HBT SiGeC with cut-off frequencies f_T and f_{max} higher than 200 GHz in 300 K and 65 K. By using Advanced Design System software (ADS), the parameters values of HICUM model are obtained for the transistor used in [1] with an emitter surface A_E = 0.17 µm x 6.2 µm. Fig. 2 shows the Gummel curves:

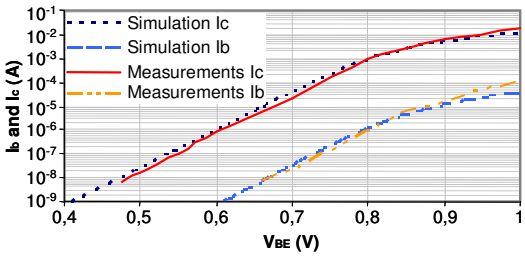


Fig. 2 Gummel curves

A good agreement is observed between simulated and measured data. Therefore, it is affirmed that the HICUM parameters values used in simulation correspond well to those of the hetero-junction bipolar transistor SiGeC to 200 GHz of [1]. Fig. 3 and 4 show f_T-I_C and f_{max}-I_C curves obtained at V_{CB} = 0.5V for the same device.

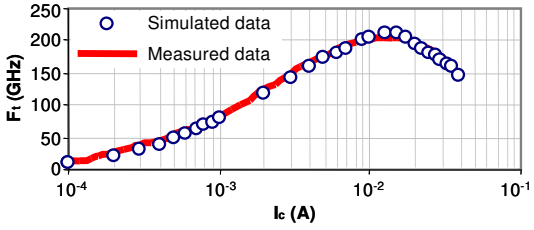


Fig. 3 Cut-off frequency f_T versus collector current I_C

To reiterate, this device exhibits cut-off frequencies f_T and f_{max} around 200 GHz. A very good agreement is observed between measured and simulated data where the best performance is reached for a collector current near 13 mA/µm².

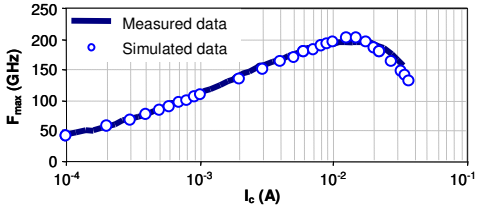
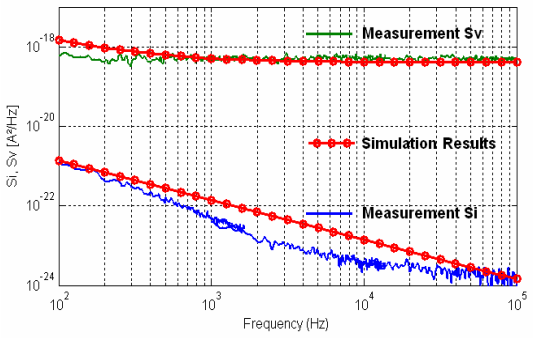
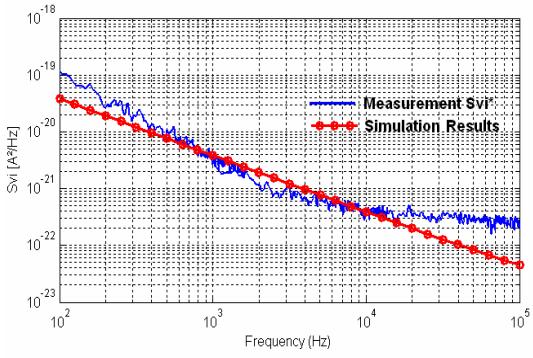


Fig. 4 Cut-off frequency f_{max}-versus collector current I_C

To design low phase noise microwave oscillator, an accurate low frequency noise model of active device is also a critical design issue. In a bipolar device the noise behaviour is fully described by the determination of both the tension and current fluctuations including their correlation [4]. Fig. 5 reports the spectra of S_V and S_I together with their cross-spectrum S_{VI^*} for bias points: I_B=1µA and I_C=1.3 mA.



a)



(b)

Fig. 5 (a) S_V and S_I spectra and (b) their cross-spectrum S_{VI^*}, simulated and measured. The spectra obtained with the HBT, respectively, biased at I_B=1µA, I_C=1.3mA. The HBT under test features an emitter area of 0.17 µm x 6.2 µm

The precision of HICUM is well verified in ADS software. We have used this reliable model of bipolar transistors, in the high performances VCO architectures design.

III. TECHNOLOGY

The available SiGe:C Heterojonction Bipolar Transistors (HBTs) exhibit a graded Ge et C profiles within the base in order to reduce the base transit time. ST Microelectronics founder keeps the 200-GHz-f_T BiCMOS SiGe:C technology as confidential research information. For this reason, we present only in this part the 55 GHz-f_T BiCMOS SiGe:C technology. The low voltage version dedicated to the RF applications (break-down voltage, BV_{CEO} = 3.3V – transition frequency, f_T = 55 GHz) associated to a low noise figure of merite is selected. These transistors have typical performances, for a surface of emitter A_E=0.4x12.8 µm², a current gain β of 200, an Early voltage of about 200 V, also a transition frequency f_T and an oscillation maximal frequency f_{max} of 55 GHz and 100 GHz respectively. For this type of TBH, the emitter width, W_E, and the emitter length, L_E, may change of 0.4 µm to 1.6 µm and of 0.8 µm to 30 µm respectively, always with $L_E \geq W_E$. Finally, we can use until 6 fingers of base (5 for the emitter and the collector). Therefore, it is important to realize an analysis to keep the best candidate for the oscillator application, where low phase noise and optimal output power are important criterions. High frequency simulations in small signal and low frequency noise study must be done to verify the waited evolutions. These simulations have to be associated to the performances analysis of the oscillator [2]. In our work, the HBT used is the NN232A128. It consists of 2 fingers of emitter, 3 of base and 2 of collector. Its emitter width is W_E=A=0.4 µm and its emitter length is L_E=12.8 µm.

According to passive elements, the technology features 5 metal levels, which makes possible the realization of MIM capacitors and spiral inductors. Inductors are realized with patterned ground shield topology, featuring reasonable quality factor at the frequency of 20 GHz if an optimal value and an appropriate geometry are chosen.

IV. DESIGN CONSIDERATIONS

Two oscillator topologies have been studied and compared in details: Cross-Coupled Differential Pair and Balanced Colpitts.

The differential structure using crossed transistors is presented in Fig. 6. It exhibits a positive feedback caused by a capacitive connection (C_1, C_2) crossed between the base and collector terminals of transistors in differential pair.

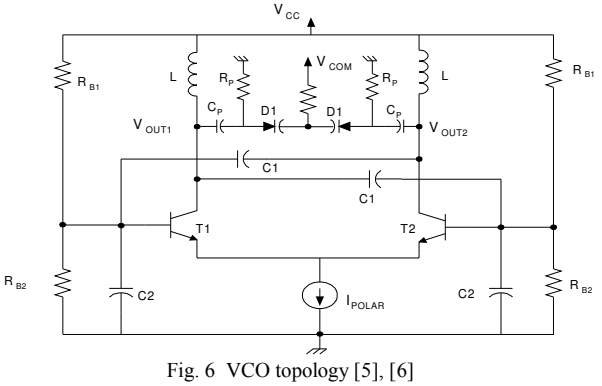


Fig. 6 VCO topology [5], [6]

These capacitive connections allow independent bias of the collector of T_2 (respectively T_1) of the base of T_1 (respectively T_2), thus enabling the control of the voltage excursion on the base of transistors.

The transistors in commutation associated to the positive feedback provide a negative resistance which compensates the resonator LC losses and thus the birth of an oscillating regime is caused [5]. The capacitances C_p are used to reduce non linearity's of varactors.

A stable oscillation demands that *Barkhausen criterion* is simultaneously satisfied. The oscillation frequency depends mainly on the values of "LC" components in the resonator, but also on the capacitive bridge C_1, C_2 and the parasites capacitances in the transistors.

The operating conditions of the transistors are determined by the feedback capacitances ratio n and the bias current I_{POLAR}.

with $$n = \frac{C_1 + C_2}{C_1} = 1 + \frac{C_2}{C_1} \qquad (7)$$

Three operating modes *(dynamic modes)* can be distinguished: linear, nonlinear and very strongly nonlinear. The "slightly nonlinear" mode allows an optimization of the output voltage excursion and a relatively low level of harmonics. At fixed I_{POLAR}, the capacitances ratio n controls the transistors operating conditions of the differential pair. A weak capacitance relation increases the gain compression of transistors, and then supports the influence of their non-linearity, trans-conductance and capacitances (junction capacitance, transition capacitance and trans-capacitances). This operating mode also reduces the conduction time of transistors. Usually this last point is a key to reduce the phase noise, due to the cycle-stationary properties of noise sources associated with the collector current.

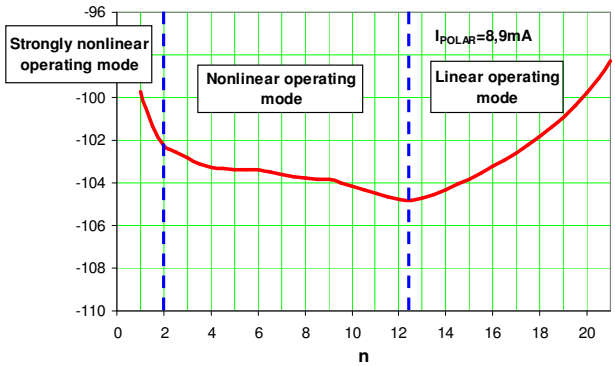


Fig. 7 Phase noise at 1 MHz (dBc/Hz) offset (carrier frequency is 20 GHz) versus capacitances ratio n (bias current I_{POLAR} = 8.9 mA). The HBT used is NN232A128.

In fig. 7, phase noise at 1 MHz offset versus capacitances ratio *n* is reported for oscillator designed in 55-GHz-f_T BiCMOS SiGe:C technology.

An absolute nonlinear region can be observed for $2 < n < 12.5$. When n is larger than 2, we see an improvement of the phase noise to move away from non-linearities on the transistor, that

deteriorate the phase noise. However, if n is too weak (n < 2), an increase of noise is noted. The phase noise then tends to increase while the conduction time of the transistors diminishes.

Fig. 8 presents the VCO schematic of a balanced Colpitts topology in common base configuration.

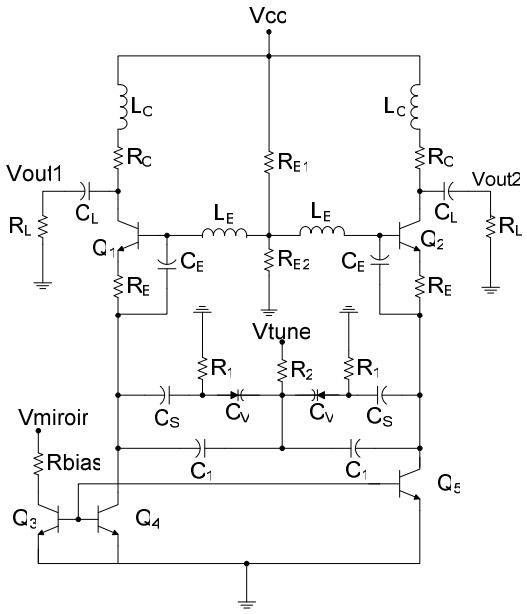


Fig. 8 Balanced Colpitts VCO

This circuit can oscillate at frequencies greater than common emitter Colpitts oscillator because its gain in high frequency is larger. The fundamental frequency signal is taken at the differential exits V_{out1} and V_{out2}. The oscillators with a cross-coupled differential pair use an LC resonator circuit which imposes a limit on the maximum possible oscillation frequency. In addition the resonant tank is loaded directly by the buffer, thus increasing the noise current in the resonator. The size reduction is an advantage of the common base Colpitts design compared to the cross differential pair oscillators [7], [8], with the size reduction almost of half circuit. In addition the tank circuit, located in the base of transistor, is readily isolated from the collector load. The architecture ensures a low noise minimizing the number of transistors in the circuit. The negative resistance is the result of capacitive loading (due to the varactor C_v) of the emitter.

V. Results and Discussion

For the same reasons already mentioned in section III, the majority of the results and numerical data is related to the f_T=55 GHz BiCMOS SiGe:C technology.

The two different VCO circuits operate with supply voltages from 2.5V. The cross differential pair topology provides a constant bias-current of 4.45 mA (in the case of the Balanced Colpitts, it is equal to 2.50 mA). The weak second harmonic rejection and a large instability in the output power have been observed. The incorporation of a buffer improve the VCO output characteristics: a good isolation between the oscillator and the load (50Ω) to reduce the pulling factor in the circuit; a linear operation of the transistor on the buffer to control the output signal distortion; an input impedance that varies very weakly with the frequency which guarantees a constant level output power on the VCO tuning range and a better power consumption.

To optimize VCO features, two configurations (emitter following and common emitter) have been studied and compared in details. The second harmonic rejection was not sufficient (about 22 dB) to satisfy the initial requirements (25 dB) and so, a simple pass-band filter was placed in the buffer output. This filter increases the rejection of the second harmonic. At the same time it conserves the VCO initial performances. To prevent the degradation of the small fundamental output power variations a wide filter tuning range and a very effective second harmonic filtering are necessary. The common emitter configuration exhibits a greater power output (7 dBm) than the following emitters (4 dBm). The output power is almost constant over the tuning voltage for both buffer configurations. A good tuning range value has been obtained, 395 MHz and 420 MHz for the following emitter and the common emitter respectively. However, the common emitter configuration uses an inductor additional of 1.26 nH, which produce a bigger size in the final circuit.

Pushing and pulling factors were also simulated in SPectreRF and ADS, by varying the supply voltage and the load resistance, respectively, and observing the change in oscillation frequency.

The layout of the LC-VCO cross-coupled differential pair occupies 430 x 480 μm² of chip area and consumes 22.3 mW at 2.5V. Special attention was paid to making the layout of the differential circuits a symmetrical as possible. This is clearly visible in Fig. 9.

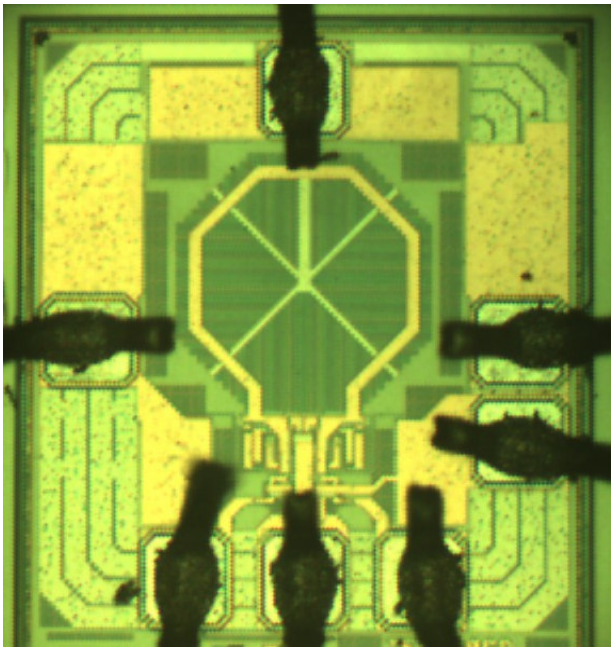


Fig. 9 20 GHz SiGe:C LC-VCO cross-coupled differential pair layout measuring 305 μm x 405 μm

In addition, the inductors layout and their placement relative to the core of the VCO were carefully evaluated. The distance between the inductors was also optimized using the concept of coupling inductance coefficient.

Finally, both VCO exhibits very good performance (table I) in terms of phase noise (-105 and -96.5 dBc/Hz at 1 MHz offset), power consumption (with 22.3 mW at 2.5 V supply without output buffer contribution), output signal power (4 dBm and 1.1 dBm with respectively by the two topologies) and second harmonic rejection of 27 et 25 dBm (with a output filter for the cross-coupled differential pair topology).

The simulation results for both oscillators and the comparison with the 200 GHz technology simulation results are summarized in Table I.

TABLE I
SUMMARY OF VCO PRINCIPAL SIMULATION PERFORMANCES WITH THE TWO ANALYSED TECHNOLOGIES

	Cross-coupled differential pair		Common Base Balanced Colpitts	
	f_T=200 GHz	f_T=55 GHz	f_T=200 GHz	f_T=55 GHz
Oscillation frequency f_{osc} (GHz) at V_{tune}=1V	21.78	19.9	19.9	20.06
Tuning range (MHz) [V_{tune}=0-5V]	2 972	415	215	130
Phase noise at 1 MHz (dBc/Hz)	-112.4	-106	-93	-96.5
Supply voltage (V)	3.3	2.5	3.3	2.5
Output power (dBm)	7.1	-10	4.2	1.1
Second harmonic rejection (dB)	26.1	25	30	27
Power consumption (mW)	46	22.35	13.2	12.5
Figure of Merit (FOM)	-182	-179	-168	-172

According to phase noise performance measure, for the cross-coupled differential pair topology with the f_T=55 GHz BiCMOS SiGe:C technology, very good levels have been noted, as shown in Fig. 10.

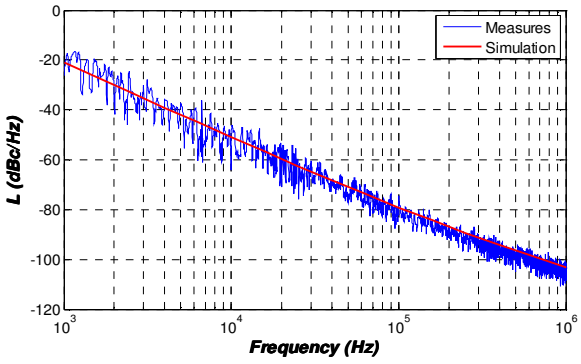


Fig. 10 Measured phase noise @1MHz offset at 20GHz

The spectrum of the single-ended output power at a center frequency of about 20.483 GHz is shown in fig. 11 for the same oscillator.

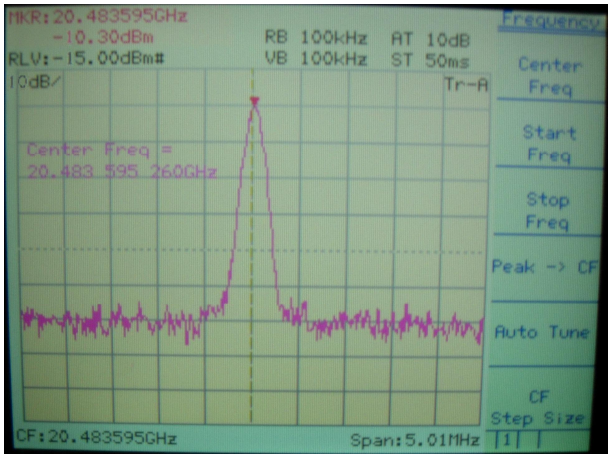


Fig. 11 Measured single-ended output power spectrum at a center frequency of 20.483 GHz. Due to the losses of the coaxial measurement cable and the adapted transmission line, 10 dBm must be added to this plot to obtain the real output power

The accuracy of the HICUM transistor model and the design methodology is really very good. Indeed, all measured results are in rather good agreement with the simulated results, except for the output power. As explained in Fig. 11, for this characteristic, losses due mainly to a bad adaptation are responsible for low power level (-10dBm).

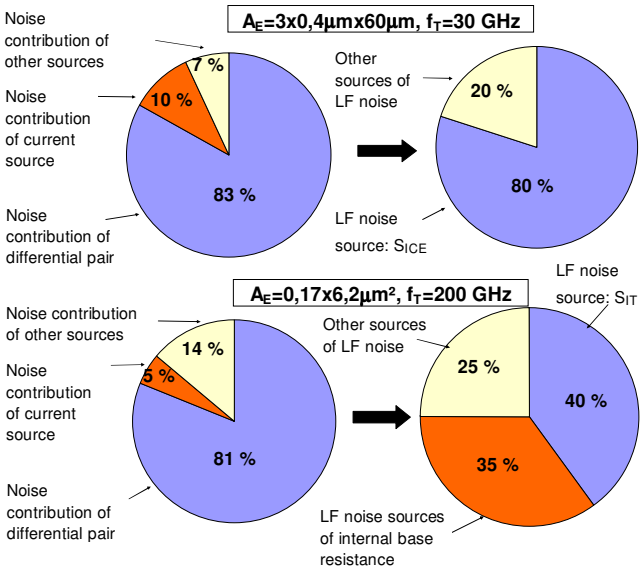


Fig. 12 Phase noise due to noise sources of cross-coupled transistors for the two buffers configurations

We have already developed this design methodology in a 0.35 µm BiCMOS SiGe technology with good agreement between simulated and measured data [5]. A low frequency (LF) noise model using an original method based on the correlation

resistance concept had been developed and associated to a non-linear non-quasi-static transistor model [9]. Comparative results related to the noise sources contributions for a 5 and 20 GHz VCO using a HBT emitter surface A_E = 3 x 0.4 µm x 60 µm and A_E = 0.17 µm x 6.2 µm respectively are presented in Fig. 12.

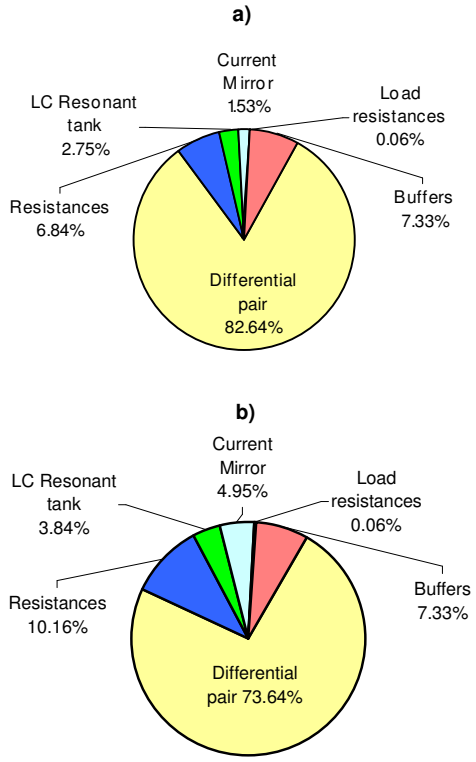


Fig. 13 Comparison of low frequency noise sources contributions on the VCO phase noise for the 20 GHz VCO BiCMOS SiGe:C a) NN252A128 (2 emitter, 3 base, 2 collector, fingers respectively), b) NN562A256 (5 emitter, 6 base, 2 collector, fingers respectively)

For both VCOs, the dominating LF noise is the differential pair noise (~ 80%). It is effectively generated by the transfer current noise and the internal base resistance noise for the 20 GHz VCO (~ 75%) of transistors T_1 and T_2. For the 5 GHz VCO, the principal LF noise source is the shot noise source S_{ICE}.

There is a reduction of the noise contribution of differential pair when we increase the quantity of base fingers, because that generates a reduction of the base resistance (fig. 13). Nevertheless, the increase of base fingers also produces an increase of the consumption power, for that it is not necessary to raise too much the fingers quantity.

VI. Conclusion

A complete analysis and design considerations of 20 GHz low phase noise VCO using a 55-GHz-f_T BiCMOS SiGe:C and a 200-GHz-f_T BiCMOS SiGe:C technologies have been presented. To author's knowledge, a measured phase noise of -106 dBc/Hz at 1MHz offset associated to a output power of -10 dBm and a FOM of -179 are the best obtained for a fully integrated VCO, designed in a commercial monolithic integrated circuit (I_C) SiGe bipolar technology. The major limit of MMIC circuits is the circuit layout. It imposes a chip obstruction the most reduced. Nevertheless, the fundamental electric characteristics of the VCO could be optimized by a judicious choice of the values of the components constituting the complete circuit.

Acknoledgment

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