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NTE4164
Integrated Circuit
NMOS, 64K Dynamic RAM, 150ns
16–Lead DIP Type Package

Description:

The NTE4164 is a high speed Dynamic Random Access Memory (DRAM) in a 16–Lead DIP type package organized as 65,536 words of one bit each.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 74TTL. All address lines and data–in are latched on chip to simplify system design. Data–out is unlatched to allow greater system flexibility. Pin1 has no internal connections to allow compatibility with other 64K RAMs using this pin for an additional function.

Features:

- 65,536 x 1 Organization
- Single +5V Supply (10% Tolerance)
- Upward Pin Compatible with 4116 (16K Dynamic RAM)
- Max Access Time from RAS: Less than 150ns
- Min Cycle Time (Read or Write): Less than 260ns
- Long Refresh Period: 4 milliseconds
- Low Refresh Overhead Time: As Low As 1.8% of Total Refresh Period
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3–State Unlatched Outputs
- Page–Mode Operation for Faster Access
- Low Power Dissipation:
  Operating . . . . 135mW (Typ)
  Standby . . . . . 17.5mW (Typ)

Absolute Maximum Ratings: (T_A = 0° to +70°C unless otherwise specified)

Voltage on any Pin except V_{DD} and Data Out (Note 1) . . . . . –1.5V to 10V
Voltage on V_{DD} Supply and Data Out with respect to V_{SS} . . . . . –1V to 6V
Short Circuit Output Current 50mA
Power Dissipation, P_D 1W
Operating Ambient Temperature Range, T_A . . . . . 0° to +70°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C

Note 1. All voltage values in this data sheet are with respect to V_{SS}.

Recommended Operating Conditions:

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		4.5	5.0	5.5	V
	V_{SS}		–	0	–	V
High–Level Input Voltage	V_{IH}		2.4	–	V_{DD}+00.3	V
Low–Level Input Voltage	V_{IL}		–1	–	0.8	V
Refresh Time	$t_{refresh}$		–	–	4	ms
Operating Ambient Temperature	T_A		0	–	+70	°C

Electricall Characteristics: (Over full ranges of recommended operating conditions unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High–Level Outpu Voltage	V_{OH}	I_{OH} = –5mA	2.4	–	–	V
Low–Level Output Voltage	V_{OL}	I_{OL} = 4.2mA	–	–	0.4	V
Input Current (Leakage)	I_I	V_I = 0V to 5.8V, All Other Pins = 0V	–10	–	+10	μA
Output Current (Leakage)	I_O	V_O = 0.4V to 5.5V, CAS High	–10	–	+10	μA
Average Operating Current during Read or Write Cycle	I_{DD1}	Minimum Cycle Time	–	40	48	mA
Standby Current	I_{DD2}	After 1 Memory Cycle, RAS and CAS High	–	3.5	5.0	mA
Average Refresh Current	I_{DD3}	Minimum Cycle Time, RAS Low, CAS High	–	28	40	mA
Average Page–Mode Current	I_{DD4}	Minimum Cycle Time, RAS Low, CAS Cycling	–	28	40	mA

Capacitance: (T_A = +25°C, V_{DD} = 5V, f = 1MHz unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Capacitance, Address Inputs	$C_{I(A)}$		–	4	5	pF
Input Capacitance, Data Inputs	$C_{I(D)}$		–	4	5	pF
Input Capacitance, Strobe Inputs	$C_{I(RC)}$		–	6	8	pF
Input Capacitance, Write Enable Inputs	$C_{I(W)}$		–	6	8	pF
Output Capacitance	C_O		–	5	6	pF

Switching Characteristics: (T_A = +25°C, V_{DD} = 5V, C_L = 100pF unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Access Time from Column Address Strobe	t_{CAC}	Load = 2 Series 74TTL Gates	–	–	70	ns
Access Time from Row Address Strobe	t_{RAC}	t_{RACL} = Max, Load = 2 Series 74TTL Gates	–	–	120	ns
Output Disabl Time	t_{OFF}	Load = 2 Series 74TTL Gates	0	–	40	ns

Timing Requirements: (T_A = +25°C, V_{DD} = 5V unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit
Page Mode Cycle Time	t_{PC}	130	–	–	ns
Read Cycle Time	t_{RC}	230	–	–	ns

Timing Requirements (Cont'd): (T_A = +25°C, V_{DD} = 5V unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit
Write Time Cycle	t_{WC}	230	–	–	ns
Read–Write/Read–Modify–Write Cycle Time	t_{RWC}	256	–	–	ns
Pulse Width, Column Address Strobe High (Precharge Time, Note 2)	t_{CP}	50	–	–	ns
Pulse Width, Column Address Strobe Low	t_{CAS}	70	–	10,000	ns
Pulse Width, Row Address Strobe High (Precharge Time)	t_{RP}	80	–	–	ns
Pulse Width, Row Address Strobe Low	t_{RAS}	120	–	10,000	ns
Write Pulse Width	t_{SP}	40	–	–	ns
ransition Times (Rise and Fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	–	50	ns
Column Address Setup Time	t_{ASC}	–5	–	–	ns
Row Address Setup Time	t_{ASR}	0	–	–	ns
Data Setup Time	t_{DS}	0	–	–	ns
Read Command Setup Time	t_{RCS}	0	–	–	ns
Write Command Setup Time before $\overline{CAS}$ High	t_{CWL}	50	–	–	ns
Write Command Setup Time before $\overline{RAS}$ High	t_{RWL}	50	–	–	ns
Column Address Hold Time after $\overline{CAS}$ Low	t_{CAH}	40	–	–	ns
Row Address Hold Time	t_{RAH}	15	–	–	ns
Column Address Hold Time after $\overline{RAS}$ Low	t_{AR}	95	–	–	ns
CAS Hold Time after $\overline{RAS}$ Low	t_{CSH}	150	–	–	ns
Data Hold Time after $\overline{CAS}$ Low	t_{DHS}	40	–	–	ns
Data Hold Time after $\overline{RAS}$ Low	t_{DHR}	85	–	–	ns
Data Hold Time after $\overline{W}$ Low	t_{DHC}	40	–	–	ns
Read Command Hold Time	t_{RCH}	0	–	–	ns
Write Command Hold Time after $\overline{CAS}$ Low	t_{WCH}	40	–	–	ns
Write Command Hold Time after $\overline{RAS}$ Low	t_{WCR}	85	–	–	ns
Delay Time, Column Address Strobe High to Row Address Strobe Low	t_{CRP}	0	–	–	ns
Delay Time, Column Address Strobe Low to Row Address Strobe High	t_{RSH}	70	–	–	ns
Delay Time, Column Address Strobe Low to $\overline{W}$ Low (Read, Modify–Write–Cycle Only)	t_{CWD}	40	–	–	ns
Delay Time, Row Address Strobe Lo to Column Address Strobe Low (Maximum Value Specified Only to Guarantee Access Time)	t_{RCD}	15	–	50	ns
Delay Time, Row Address Strobe Low to $\overline{W}$ Low (Read, Modify–Write–Cycle Only)	t_{RWD}	11	–	–	ns
Delay Time, $\overline{W}$ Low to Column Address Strobe Low (Early Write Cycle)	t_{WCS}	–5	–	–	ns

Note 2. Page Mode Only.

Operation:

Address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage cell locations. Eight row−address bits are set up on pins A0 through A7 and latched onto the chip by the row−address strobe ($\overline{RAS}$). Then the eight column−address bits are set up on pins A0 through A7 and latched onto the chip by the column−address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

Write Enable ($\overline{W}$)

The read or write mode is selected through the write enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write enable pin can be driven from standard TTL circuits without a pull−up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data−out will remain in the high−impedance state for the entire cycle permitting common I/O operation.

Data−In (D)

Data is written during a write or read−modify write cycle. The falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on−chip data latch. This latch can be driven from standard TTL circuits without a pull−up resistor. In an early write cycle $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read−modify write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

Data−Out (Q)

The three state output buffer provides direct TTL compatibility (no pull−up resistor required) with a fan−out of two Series 74TTL loads. Data−out is the same polarity as data−in. The output is in the high−impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high−impedance state. In an early write cycle, the output is always in the high−impedance state. In a delayed write or read−modify−write cycle, the output will follow the sequence for the read cycle.

Refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffer is in the high−impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$ only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

Page Mode

Page mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on a single RAM, the row address and $\overline{RAS}$ are applied to multiple 64K RAMs. $\overline{CAS}$ is then decoded to select the proper RAM.

Pin Connection Diagram