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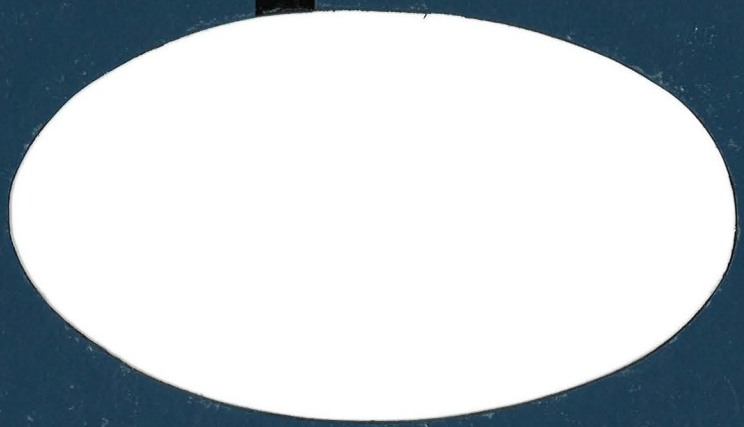
APOLLO

GUIDANCE, NAVIGATION AND CONTROL



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USERS' GUIDE TO THE AGC MONITOR (CORE ROPE SIMULATOR)

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September 1966

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USERS' GUIDE TO THE AGC MONITOR (CORE ROPE SIMULATOR)

ABSTRACT

This report contains a description of the operation of the Apollo Guidance Computer Monitor, also know as the Core Rope Simulator, which was designed and built by M.I.T. Instrumentation Laboratory, Cambridge, Massachusetts.

The purpose of the AGC Monitor is: (1), to provide a computer monitor to aid in computer troubleshooting and program debugging, and (2), to provide core rope simulation, i.e., replacement of the AGC fixed memory with an erasable memory which can be loaded automatically by using a tape or manually by using a keyboard.

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September 1966

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CHAPTER I

DESCRIPTION

1.1 Introduction

This manual contains a description of the operation of the Apollo Guidance Computer Monitor (Fig. 1.1). The Monitor was designed and built by MIT Instrumentation Laboratory, Cambridge, Massachusetts.

1.2 Purpose of the Monitor

The AGC Monitor has two functions, the first of which is implied by its name, that is, it can be used as a computer monitor which can be very helpful in debugging AGC programs.

The second function of the Monitor is core rope simulation. The Monitor is capable of replacing all or part of the fixed memory of the AGC with a erasable memory. It is because of this second function that the Monitor is also known as the CRS (Core Rope Simulator). At the risk of some confusion, the piece of equipment under consideration here will be referred to as either the CRS or the Monitor.

1.3 Physical Description

The Monitor is a single-bay console consisting of a paper tape unit and a magnetic tape unit; display and control panel; three power supplies; up to ten memory units; and several racks of micrologic assembly and wiring. The sides of the console fold out in accordion fashion to give additional area for micrologic modules. The memory units are located inside the main body of the console and are reached by opening the side panels of the console. A rear door allows access to the magnetic tape unit.

The interface connection from the AGC to the Monitor is on the front near the bottom right.

The erasable memory of the Monitor is used to replace all or part of the AGC core ropes. Loading the Monitor memory is accomplished automatically, using perforated paper tape or magnetic tape, or manually, using the keyboard on the control panel. Tape loading allows a rapid loading of the entire memory, whereas manual loading can be used to load small programs or to revise data already loaded.

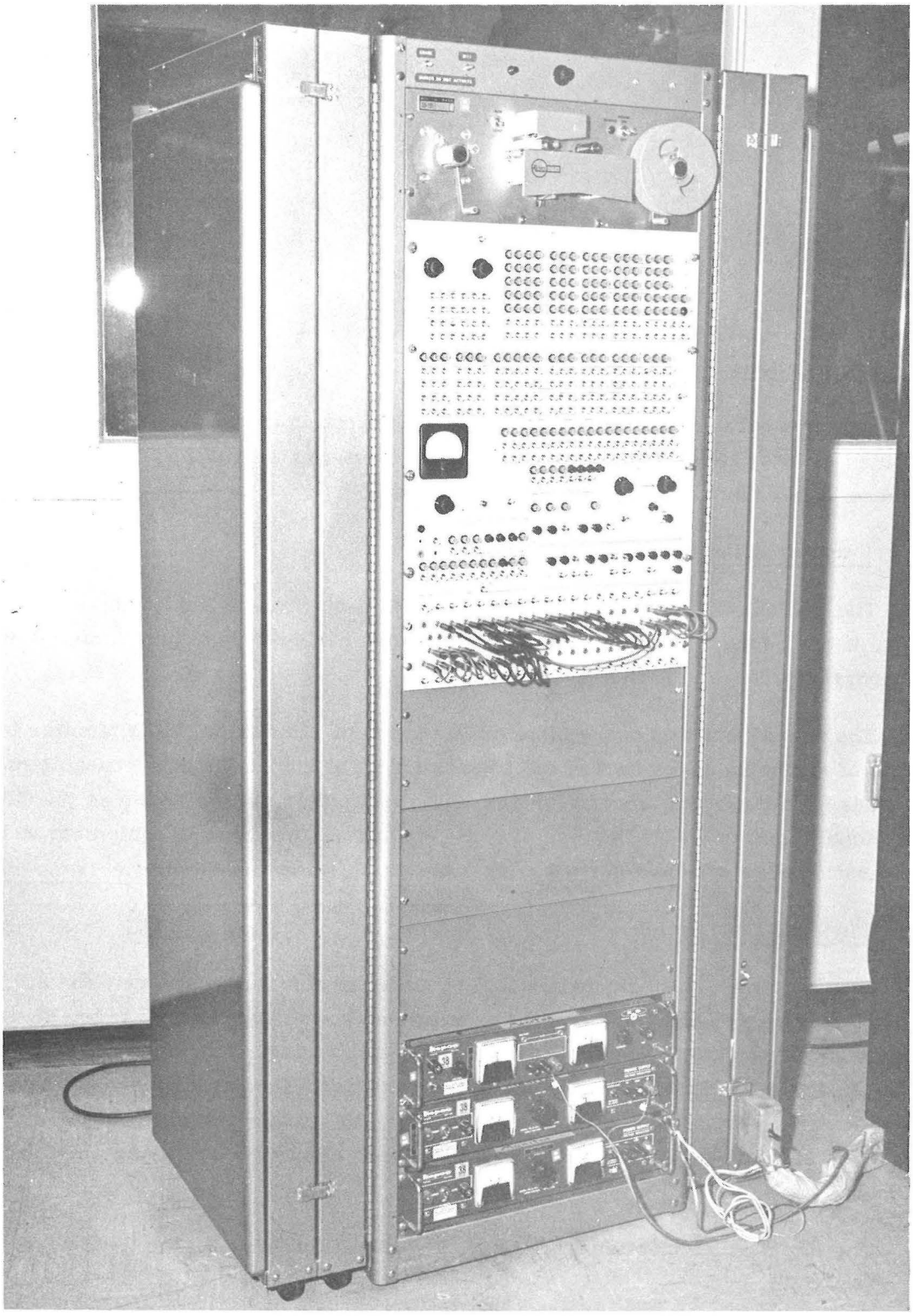

Fig. 1.1 Apollo Guidance Computer Monitor

The Monitor may be used with either the Block I or Block II AGC. It has control and monitor capabilities over the operation of the AGC. The AGC time counter can be stopped under a variety of conditions, data within the AGC can be monitored, and a transfer of control can be initiated from the Monitor.

In addition, the Monitor may be used to load and read the AGC erasable memory using paper or magnetic tape, or to dump the contents of the AGC erasable memory onto magnetic tape.

1.4 Operating Controls and Indicators

The operating controls and indicators are shown in Fig. 1.2 and are listed and described in Table 1.1.

In all the registers on the main panel (A, Z, L, G, W, and S), binary representation of octal numbers in used. This is illustrated below. In each register, the lights are divided up into groups of three, with an extra light in the left-hand group and (in the case of G and W) two extra lights on the right end. The S register is an exception and will be dealt with later. Each group of three lights represents one octal digit.

SG	US	14	13	12	11	10	9	8	7	6	5	4	3	2	1
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O

It is easier to think about at first if each group of three is thought of like this;

3	2	1
④	②	①

Simply add up the values on the lights that are lit, and the octal value of the digit is obtained. With practice, one is soon able to automatically associate a given combination of lights with its proper octal digit.

As an example

SG	US	14	13	12	11	10	9	8	7	6	5	4	3	2	1
●	O	O	●	O	●	●	●	O	O	O	O	O	●	●	●

is the octal number 53407.

Note that the bit marked US is not used in reading the number. This is the uncorrected sign bit and is used when all sixteen bits of the word are used as value bits, such as for overflow. When reading the register, care should be taken not to use this bit.

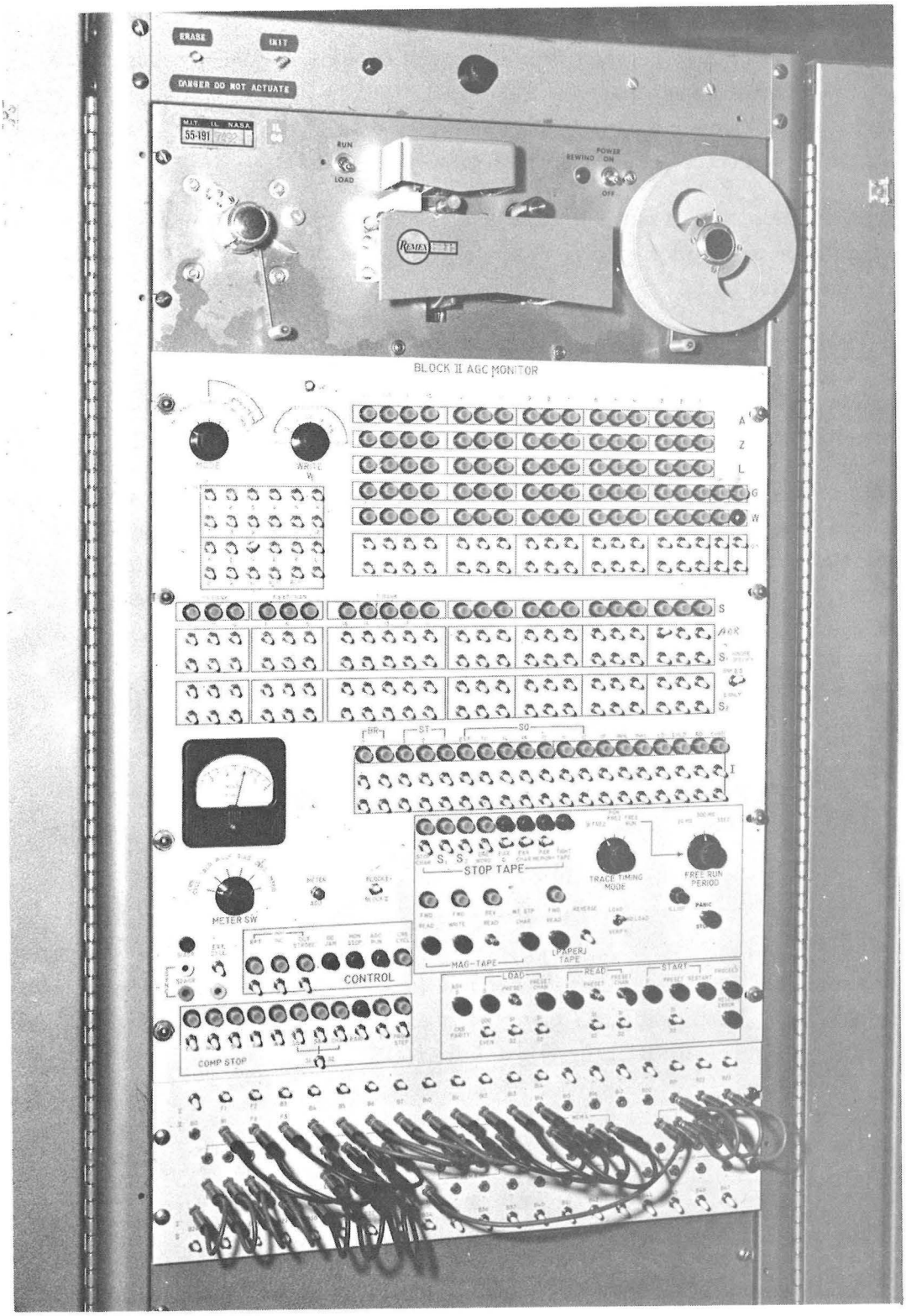

Fig. 1.2 Operating Controls and Indicators

TABLE 1.1

OPERATING CONTROLS AND INDICATORS

Control or Indicator	Function
MODE switch	Selects one of five modes of operation.
WRITE W switch	Selects display for W register
S1 - S2 switch	Selects either S1 or S2 COMPARATOR switches for use in S, S & I, and P & S positions of WRITE W.
T1 through T 12 switches	Select time for display in W register.
WRITE PULSE switches	Select write pulse for display in W
A REGISTER indicators	Display contents of A register
Z REGISTER indicators	Display contents of Z register
L REGISTER indicators	Display contents of L register
G REGISTER indicators	Display contents of G register
W REGISTER indicators	Display contents of W register
W COMPARATOR switches (two rows of switches below W)	Sets data for AGC time counter stop. The top row is also used when manually changing the contents of a location.
S REGISTER indicators	Display contents of ER BANK, F EXTCHAN, F BANK, and S registers.
S1 COMPARATOR switches S2 COMPARATOR switches	Set address to be read or loaded or for AGC time counter stop.
BANK S-S ONLY switch	In S ONLY position, keeps the contents of the bank indicators from being altered while performing a Load Preset, Read Preset, or Start Preset.
I REGISTER indicators	Display various sequence generator functions.
I COMPARATOR switches	Select function for AGC time counter stop.
VOLTMETER	Shows the percentage of time that a condition set on the switch below it is occuring.
Voltmeter Display Switch	Selects CRS cycling, I, W, S1, S2, or magnetic tape strobe for display on the meter.
METER ADJUST	Adjusts the meter.
BLOCK I - BLOCK II switch	Selects Block I or Block II operation.
EXT. CYCLE switch and four plugs	Allow memory to be exercised externally for trouble shooting purposes.

INH RPT switch and indicator	Enables or disables and monitors inhibit interrupt to AGC.
INH INC switch and indicator	Enables or disables and monitors inhibit increment to AGC.
INH OUT STROBE switch and indicator.	Enables or disables and monitors timing inhibit to AGC.
GO JAM indicator	Indicates signal GOJAM has occured.
MON STOP indicator	Indicates that the Monitor has requested an AGC time counter stop.
AGC RUN indicator	Indicates that the AGC is operating.
CRS CYCL indicator	Indicates that the Monitor is performing a memory cycle (simulating).
TAPE CONTROLS & INDICATORS	
STOP CHAR switch and indicator	Stops tape on stop character at end of each bank
S1 switch and indicator	Stops tape on S1 agreement
S2 switch and indicator	Stops tape on S2 agreement
ONE WORD switch and indicator	Stops tape after each word
PAR G switch and indicator	Stops tape when G register has incorrect parity. (This indicates an incorrect word was read from tape).
PAR CHAR switch and indicator	Stops tape when a tape frame has incorrect parity.
PAR MEMORY switch and indicator	Stops tape or AGC when Monitor memory has incorrect parity.
TIGHT TAPE indicator	Indicates that magnetic tape is tight and in danger of tearing.
MAG TAPE:	
FWD READ switch and indicator	Reads mag. tape into memory
FWD WRITE switch and indicator	Writes contents of memory on mag. tape.
REV READ switch and indicator	Rewinds mag. tape
WT STP CHAR switch	Writes a stop character on mag. tape.
PAPER TAPE:	
FWD READ switch and indicator	Reads paper tape into memory.
REVERSE switch	Rewinds paper tape
LOAD-NO-LOAD-VERIFY switch	Allows paper tape to be loaded into memory or to be just run through. The VERIFY position is used to check memory contents.
ILLIOP indicator	Indicates that the operator has performed an illegal operation on the keyboard.
PANIC STOP switch	Stops the tapes.

TRACE TIMING MODE AND FREE RUN PERIOD switches	Used for recording W register contents on mag tape.
COMPARISON STOP switches	Produces time counter stop for 11 different conditions.
ADV S switch	Increments register S once each time depressed.
LOAD S switch	Loads the location on the S indicators
LOAD PRESET switch	Loads the location on the S1 or S2 switches.
LOAD PRESET CHAN switch	Loads the channel set on the S1 or S2 switches.
READ S switch	Reads the location on the S indicators.
READ PRESET switch	Reads the location on the S1 or S2 switches.
READ PRESET CHAN switch	Reads the channel set on the S1 or S2 switches.
START S switch	Starts the AGC at the location on the S indicators.
START PRESET switch	Starts the AGC at the location on the S1 or S2 switches.
RESTART switch	Sends signal WMSTART to the AGC, causing a GOJAM.
PROCEED switch	Lifts time counter stop. Resets the MON STOP indicator and all STOP indicators except PAR STOP.
RESET ERROR switch	Resets PARITY STOP indicator and the three STOP TAPE parity indicators and allows the tape to be restarted. Also resets the ILLIOP indicator.
CRS PARITY switch	Selects even or odd parity for CRS words.
S1 - S2 switches	Select either S1 or S2 COMPARATOR switches for use with the corresponding switch.
BANK SELECTION switches	Select CRS locations to be used.

The two bits marked SP and GP in the G and W registers are parity bits. The SP bit is the Sensed Parity bit and is the parity bit sensed from bit 15 of the memory. The GP bit is the Generated Parity bit which comes from the parity tree in the computer and is checked with the Sensed Parity for agreement.

In general, then, bit 16 from a memory word is written into the SG and US positions and bit 15 is written into SP. However, if all sixteen bits of the word are value bits, as is sometimes the case, then bit 15 is written into US and bit 16 into SG.

CHAPTER 2

OPERATING THEORY

2.1 Introduction

This chapter sets forth information which is essential to the understanding of the operation of the Monitor.

2.2 Monitor Registers

The A, Z, and L registers perform a strict monitoring function only. The A register displays the contents of the accumulator of the AGC. The Z register displays the address of the instruction to be executed next. The L register performs different functions in Block I and II. In Block I, it displays the contents of the Q register; in Block II it displays the contents of the L register or lower accumulator. The L register is an extension of the A register and is used in multiprecision operations.

The S register displays on 23 lights an octal location in fixed or erasable memory. The 12 lights farthest to the right contain the address (for Block II a number between 4000 and 7777 for fixed - fixed; between 2000 and 3777 for fixed; and 0000-1777 for erasable).

The next five lights to the left contain the fixed bank address (a number between 00 and 37). Only two lights are needed for the first digit since it has a maximum value of three.

The next three lights are the fixed extension channel number (a number between 0 and 7). This is also known as the Super Bank Register.

The last three lights on the left display the erasable bank number (a number between 0 and 7).

There are four rows of switches below the S indicators. Two rows are designated S1 and two rows as S2. These groups of switches will be referred to as comparator switches. The operation of the S1 and S2 comparator switches is identical, so only S1 will be discussed.

The first (upper) row of S1 switches is used to set up the address which is to be read or loaded or which is to be used in connection with WRITE W (to be discussed later). The second row of S1 switches (called the ignore-specify switches) is used to ignore any bits of the address. That is, when an ignore-specify switch is set to the ignore position, it makes no difference if that bit is a one or a zero when the comparison is made between the contents of the register and the setting of the first row of switches. The use of these sets of comparator switches will be further discussed later.

The G register displays on 18 lights the contents of the location shown on the S indicators. The two parity bits are discussed above. The first row of switches below the W register is used in conjunction with the G register when loading data into the Monitor or AGC manually.

The W register or wild register also has 18 indicators. Using the WRITE W seven-position switch, the 24 timing and write pulse switches, and the S and I comparator switches, the W register can be used to display a great variety of items within the AGC. The two rows of comparator switches below the W register function in the same manner as the S1 and S2 comparator switches. The top row is used to set up the desired data for comparison with the W indicators. When agreement is reached, the AGC time counter can be stopped. The second row of switches is used to ignore any bits in the determination of the agreement.

The I register, or instruction register, displays several AGC sequence generator functions which allow the monitoring of any subinstruction performed by the AGC. The two rows of switches below it are used for designating a function or subinstruction which can be used for W register displays or for stopping the AGC time counter. Their use is similar to that of the S1, S2, and W comparator switches.

The following is an explanation of the various I register indicators.

The seven indicators labeled SQ indicate the order code of the instruction being executed. They are the contents of the SQ register in the sequence generator. In Block I, only EXT, SG, 14, and 13 are used to indicate the order code. In Block II, all seven bits may be used, depending on the particular instruction.

The three ST indicators show the state of the staging bits, ST3, ST2, and ST1 from the control pulse generator. They adjust the subinstruction code as required during changes of subinstructions within a machine instruction. In Block I, only ST2 and ST1 are used; in Block II, all three are used.

The two BR indicators show the state of the branch bits BR 2 and BR 1 which are the results of tests for overflow, underflow, sign, and for the quantity minus zero during subinstructions which require their use. These signals are applied to the control pulse generator to produce specific control pulses.
Note: The BR indicators do not copy the status of the AGC branch bits unless at least one of the WRITE W time pulse switches is enabled, in which case it will copy the branch bit status at that particular time only.

Signal IIP (interrupt in progress) is set during subinstruction RUPT I. It prevents an interrupting program from being interrupted by inhibiting the signal which enables interrupts in the sequence generator. It stays on until subinstruction RESUME is performed.

Signal INHL (inhibit interrupt) is turned on by instruction INHINT and turned off by RELINT.

Signal INKL indicates the occurance of a counter incrementing subinstruction or an input-output subinstruction.

The LD, RD, CHLD, and CHRD indicators come on when a load, read, load channel, or read channel operation is done from the keyboard.

2.3 Monitor Memory

The Monitor has nine memory units (plus the capability for a tenth) each of which has four banks of 1024 sixteen-bit words or a total of 4096 words per memory unit. This gives the Monitor a 36,864-word capacity which makes it capable of entirely replacing the core ropes of the AGC (Block I or Block II).

The Monitor memory units each consist of a core array (16 cores per word, or approximately 64,000 cores per memory unit, or about 585,000 cores total in the nine units), selection circuits, read and write drivers, inhibit drivers, and sense amplifiers. Their operation is similar to that of the erasable memory of the AGC. (see ND 1021001, pp. 4-271 to 291).

In the AGC fixed memory the sense amplifiers receive the outputs from the core array sense lines. When a location is addressed by the selection circuits, the 16 sense lines receive the information stored in that location. The sense amplifiers strengthen the signals and transmit them to the write lines when the output transistor is strobed by a timing pulse from the timing circuits.

A similar process takes place in the Monitor memory. But, in addition, an inhibit strobe signal is sent to the AGC which inhibits the strobing of the fixed memory sense amplifiers. Thus, the Monitor memory takes precedence over the core ropes and the core ropes need not be removed from the AGC when the Monitor memory is being used.

The patch cord assembly and the bank selection switches at the bottom of the main panel are used to select the banks of the core ropes to be replaced with Monitor memory and to select the memory units to be used.

There are two rows of plugs with corresponding switches which are labeled with their Block I and Block II bank designations. Note that some of the plugs are not used in Block I and some have the same designation in both Block I and Block II.

There are also ten groups of four plugs each labeled MEM 1 through MEM 10. These refer to the memory units 1 through 10 (there is no memory 10 installed).

Any bank of the program may be patched into any memory. Care must be taken, however, to see that any bank used in the program is connected to some memory and that the associated bank switch is turned on (up). The bank switches can be turned off to inhibit access to certain banks and cause the computer to use the core ropes for those banks.

The bank switches should be turned off (down) when connecting and disconnecting the CRS to the AGC and when turning the tape reader on and off in order to protect the memory contents from noise signals.

2.4 Tape Format

The Monitor uses an eight-channel paper tape. Channels 1 and 8 are control channels that determine which operation is to be performed (refer to Table 2.1). Channel 7 contains the parity of each line on the tape.

Depending on what the operator intends to do (load erasable, load switchable erasable, load fixed-fixed, or load fixed switchable), a tape is prepared with the proper instructions. For purposes of discussion, assume that a load fixed switchable routine is to be done. In this case character D is present first on the tape. This character sets the Fixed Ext. bits and sets $S_{10-1} = 0$ and $S_{12,11} = 11$ (Block I) or 01 (Block II). The next character on the tape is character E; it sets the Fixed Bank bits to the bank number of the bank to be loaded.

The first increment of data (character X) clears the G register, loads G_1 through G_5, and advances the tape and keyboard counter. The next increment of

TABLE 2.1 - MONITOR TAPE FORMAT

CHAR-ACTER	TAPE CHANNEL 8	7	6	5	4	SP	3	2	1	DESCRIPTION
A	1	P	1	-	-		-	-	0	PREPARE TO LOAD ERASABLE SETS S = 0000 RESETS COUNTER
B	1	P	0	-	X_4		X_3	X_2	0	PREPARE TO LOAD SWITCH-ABLE ERASABLE $X_{4,3,2} \longrightarrow E\ BANK_{11,10,9}$ SETS S = 01400 RESETS COUNTER
C	1	P	1	0	-		X_3	X_2	1	PREPARE TO LOAD FIXED-FIXED $X_{3,2} \longrightarrow S_{12,11}$ SETS $S_{10-1} = 0$ RESETS COUNTER
D	1	P	1	1	X_4		X_3	X_2	1	PREPARE TO LOAD FIXED SWITCHABLE $X_{4,3,2} \longrightarrow FIXED\ EXT_{7,6,5}$ SETS $S_{10-1} = 0$ RESETS COUNTER, SETS ENWB (NEXT CHARACTER = E)
E	0	P	X_6	X_5	X_4		X_3	X_2	1	SET FIXED BANK $X_{5-2} \longrightarrow F\ BANK_{15-11}$ RESETS COUNTER RESETS ENWD
F	1	P	0	-	-		-	-	1	STOP CHARACTER RESETS COUNTER
X,Y	0	P	X_6	X_5	X_4		X_3	X_2	1	$\underline{X}$ COUNTER = 0 $\underline{Y}$ COUNTER = 1 CLEARS G $X_{2-6} \longrightarrow G_{1-5}$ $X_{2-6} \longrightarrow G_{6-10}$ ADVANCES COUNTER ADVANCES COUNTER
Z	X_8	P	X_6	X_5	X_4		X_3	X_2	1	COUNTER = 2 $X_{2-6} \longrightarrow G_{11-15}$, X_8 = PARITY OF G_{1-15} RESETS COUNTER, ADVANCES S EXECUTES LOAD

data (character Y) loads G_6 through G_{10} and advances the tape and keyboard counter. The last increment of data (character Z) loads G_{11} through G_{15}, contains the parity of G_{1-15}, resets the tape and keyboard counter, advances the S register, and causes the data in G to be transferred to the Monitor memory.

2.5 Parity

The Monitor checks parity in three different ways. These are indicated by the three red indicators marked PAR G, PAR CHAR, and PAR MEMORY.

The PAR G indicator comes on when an error is detected in a word read from the tape.

The PAR CHAR indicator comes on when an error is detected in a single line on the tape. Each word is divided into three lines on the tape, and each of these lines has its own parity bit.

The PAR MEMORY indicator comes on when an incorrect word is read from memory.

A fourth parity error indicator is located among the stop switches on the Monitor control panel. This parity check is accomplished within the AGC. It checks the words coming into the G_1 register of the AGC from its own memory or from the Monitor.

CHAPTER 3

OPERATING PROCEDURES

3.1 Introduction

This chapter contains a description of the procedures for operating the Monitor. Detailed procedures and switch settings are given for loading the memory from tape and from the keyboard; for reading the contents of locations in the Monitor memory, the core ropes, and the AGC erasable memory; for transfering control to a location; and for using the W register display and the comparison - stop circuits for program debugging.

The Monitor has five modes of operation, selected by the MODE switch on the upper left corner of the main panel.

In the Computer mode, the Monitor becomes a part of the AGC. It can replace the core ropes with an erasable memory and serve as an aid in debugging programs.

In the Keyboard mode, the Monitor memory can be manually loaded or read.

The Load Tape mode permits the loading of the Monitor or the AGC memory, using paper or magnetic tape.

In the Dump Tape mode, the contents of the Monitor or the AGC memory can be "dumped" or stored on magnetic tape. This enables the memory to be reloaded using the magnetic tape which is much faster than the paper tape.

In the Trace Tape mode, it is possible to record the W register contents on magnetic tape.

3.2 Connecting the Monitor to the AGC

The Monitor uses the same interface cable and buffer box for both Block I and Block II. However, the cable between the AGC and the buffer box is different for Blocks I and II. The Monitor may or may not be energized, while the connection is made, but if energized, the bank selection switches should be turned off (down) to protect the memory contents.

1. Set the NISQ stop switch to (up).

2. Set all bank selection switches to off (down).

3. Connect the interface cable assembly to the connector on the lower right front of the Monitor.

4. Connect the interface cable assembly to the Test Connector on the AGC.

3.3 Energizing the Monitor

To energize the Monitor rotate the switch on the top edge of the console clockwise one position at a time. This turns on the power supplies in the proper sequence.

3.4 Operation in the Load Mode

In the Load mode, the Monitor memory or the AGC erasable memory may be loaded using the paper tape or the magnetic tape. The MODE switch should be set to the LOAD position. Load the paper tape onto the tape reader making sure that it is threaded properly and that the guide is up. Turn on the paper tape power switch (toggle switch to the right of tape reader) and set the RUN -LOAD switch (toggle switch to left of tape reader) to the RUN position.

Plug patch cords into all the bank plugs corresponding to the banks of memory to be loaded, and plug the opposite end of each cord into a memory plug. Set the corresponding bank switches to on (up).

To start the tape, push the PAPER TAPE FWD READ switch. The light above it will come on while the tape is running. The addressed locations will be displayed on the G indicators.

The LOAD-NO LOAD-VERIFY switch should be in the Load position to put the contents of the tape into the memory. In the NO LOAD position the S and G indicators display the addresses and the information on the tape, but the information is not put into memory. This is useful for verifying tapes or omitting parts of tapes.

The VERIFY position is for checking the Monitor memory or AGC memory contents with a tape. The tape content is displayed on the W indicators and the memory content on the G indicators. Disagreement will cause the tape to stop.

The STOP CHAR switch is used to stop the tape on a stop character which is punched into the tape at the end of each bank. When coming to the end of a tape,

the stop character can be used to stop the tape so that it will not have to be re-threaded.

The S1 and S2 stop switches are used to stop the tape when it reaches the address which has been set on the S1 or S2 comparator switches.

The ONE WORD stop switch will stop the tape after each word. By turning on this switch, the tape can be stepped through word-by-word by depressing the FWD READ switch.

The three parity alarm switches are used to stop the tape if there is a parity error. If a parity error is detected and the switches are on, the tape is automatically stopped and the corresponding alarm light comes on. If the switches are off when a parity error is detected, the lights will come on but the tape will not stop.

The switch and light marked PAR G are for detecting parity errors in a complete word read from the tape. The switch and light marked PAR CHAR indicate errors in one of the three lines on the tape which make up each data word and those marked PAR MEMORY indicate that an incorrect word has been read from memory.

The parity alarm lights can be reset by depressing the RESET ERROR switch. The tape can then be restarted by depressing FWD READ.

The TIGHT TAPE indicator comes on and the tape is automatically stopped if the magnetic tape becomes too tight. This condition must also be corrected before the paper tape can be run.

The REVERSE switch is used to rewind the paper tape after it has been stopped. Also, the REWIND button to the right of the tape reader may be used to rewind a tape.

Handle all paper tapes with care. Do not bend them or roughen the edges. The tape reader will not usually read correctly a tape that has been torn and then taped back together.

While running the reader, be careful to keep all dust, lint, hair, and other small particles off the reader and the tapes. By blowing sharply on the reader occasionally while the tape is running, many of these small particles can be kept out of the reader. Following these simple hints can save much time which might otherwise be lost due to faulty reading of the tape by the reader.

After loading the Monitor Memory by paper tape, the information may be stored on magnetic tape. Then, when it is necessary to reload the Monitor Memory, the magnetic tape may be used; and since the magnetic tape is much faster than the paper tape, time is saved. The "dumping" of the information onto magnetic tape is described in the succeeding section.

To load the Memory using the magnetic tape, the same procedures may be followed as for loading with paper tape. The only difference is that the MAG TAPE FWD READ switch is used to start the tape, and the MAG TAPE REV READ switch is used to rewind it. All the STOP TAPE switches function in the same manner.

When rewinding the magnetic tape, the tape will stop at the beginning of each bank and the bank number will be displayed in the G register.

The indicator labelled ILLOP indicates the operator has performed an illegal operation in the operation of the tapes. The ERROR RESET switch will reset it.

When the operator finds that he has made a mistake and the tape is running and he can't get it stopped and he has that sinking feeling of panic, the switch labeled PANIC STOP may be frantically depressed to stop any tape operation.

Now to generally sum up the loading of the Monitor Memory or AGC Erasable Memory by tape:

1. T12 stop switch on (up).
2. MODE switch to LOAD.
3. All needed banks connected to Memory and corresponding switches on (up).
4. LOAD-NO LOAD-VERIFY switch to LOAD.
5. STOP CHAR switch on (up) to stop at end of bank.
6. S1 or S2 switch on (up) and desired stopping address set on S1 or S2 Comparators.
7. ONE WORD switch on (up) to step through word-by-word.
8. PAR G, PAR CHAR, PAR MEMORY switches on (up) to stop tape on parity error.
9. For loading the AGC Erasable memory, the address minus one of the first address to be loaded should be preset on the S indicators.
10. Depress FWD READ (MAG TAPE or PAPER TAPE).

The tape will now run until one of the stop conditions is fulfilled.

3.5 Operation in the Dump Mode

As stated in the previous section, the Memory contents may be stored on magnetic tape, after first loading with paper tape, in order to speed up any future loadings.

After the Memory has been loaded from the paper tape, the MODE SELECTION switch is set to DUMP. Then, using the S1 or S2 switches and the READ PRESET switch, the content of the S REGISTER is set to contain the starting address of the bank to be dumped onto the magnetic tape. Then the MAG TAPE FWD WRITE switch is depressed and the content of the bank is dumped onto magnetic tape. The tape stops automatically at the end of the bank. The S REGISTER is then set for the starting address of the next bank to be dumped and so on until all the banks are dumped on the tape.

In order to determine if the magnetic tape is running, without opening the rear door of the console, set the six-position switch below the meter to the Magnetic Tape Strobe (MTSB) position. If the tape is running, the meter will be deflected.

3.6 Operation in Keyboard Mode

In the keyboard mode data can be manually loaded into or read out of the Monitor Memory.

3.6.1 Manual Loading of CRS

To manually load the Monitor, the following procedure is used. Set the NISQ stop to on (up) if the computer is running, and set the MODE switch to the KYBD position. Next set the word to be loaded on the top row of the W Comparator switches. The second row of switches has no bearing on this operation. Also, the switches below the SP and GP bits have no effect here. Parity for words manually loaded is generated automatically within the Monitor.

Now set the address of the location which is to be loaded on the first row of switches in either the S1 or S2 Comparator groups. The second rows again have no meaning in this case. Set the S1-S2 switch below the LOAD PRESET button to S1 or S2, depending on which set of S switches was used. Depress the LOAD PRESET switch to load the data into the chosen location. The G and the S indicators should now agree with the setting of their corresponding switches.

If the address into which it is desired to load a word is already displayed on the S indicators, it is not necessary to set up the address on the S1 or S2 switches. In this case, depress the LOAD S switch instead of the LOAD PRESET switch.

To summarize the operation of manually loading the Monitor Memory:

1. Set NISQ stop switch to on (up).
2. Set MODE switch to KYBD.
3. Set data to be loaded on the top row of W switches.
4. Set address to be loaded into on the top row of S1 or S2 switches.
5. Set S1-S2 switch to corresponding position.
6. Depress LOAD PRESET switch.
7. To load into a location which is already displayed on the S indicators, depress LOAD S instead of LOAD PRESET.

3.6.2 Manual Reading of CRS

To read out the contents of a given location in Memory, the following procedure is used.

First, turn on the NISQ stop switch if the computer is running and set the MODE switch to KYBD. Set the location to be read out on the top row of either the S1 or S2 comparator groups. Then set the S1-S2 switch below the READ PRESET switch to the corresponding position, and depress the READ PRESET switch. The S indicators should now agree with the S switches, and the G indicators should display the contents of that location.

If the address to be read is already displayed on the S indicators, depress the READ S switch instead of READ PRESET.

To summarize the manual reading of a given location:

1. Set NISQ stop switch to on (up).
2. Set MODE switch to KYBD.
3. Set address to be read out on the top row of S1 or S2 switches.
4. Set S1-S2 switch to corresponding position.
5. Depress the READ PRESET switch.
6. To read the location displayed on the S indicator depress READ S instead of READ PRESET.
7. Read the word on the G indicators.

If it should be necessary to read or load a series of locations, it is not necessary to set up each location on the S switches. Simply depress the ADV S switch to advance the contents of the S register by one. Thus, by depressing ADV S and then READ S (or LOAD S) a series of locations can be read (or loaded). Of course, when loading, the word to be loaded must be set each time on the top row of W switches.

3.7 Operation in the Computer Mode

Up to now the operating procedures which have been presented applied generally to operation with both Block I and Block II computers. However, in the Computer mode, the Monitor becomes an extension of the AGC; thus, operating procedures have slight differences, depending on whether a Block I or Block II AGC is being used.

In the Computer mode the Monitor can be used to read and load the Monitor Memory or the Erasable Memory in the computer. Also, the core ropes in the AGC may be read. The Monitor can be used to transfer control to a specified location, to display various quantities within the AGC using the wild register, and to stop the AGC time counter under almost any conceivable combination of conditions within the AGC.

It should be emphasized that there is no specific procedure for operation in the computer mode since there are so many options which depend on the particular problems involved. Therefore, the general function of all the controls is discussed.

To put the Monitor in Computer mode, first set the Block I-Block II switch to the desired setting. Then, set the MODE switch to COMP. Turn off any STOP switches which are on. Depress the PROCEED switch to lift the time counter stop and reset the stop indicators.

3.7.1 Reading and Loading

Any location in fixed or erasable memory may be read or loaded and the core ropes may be read while the Monitor is in Computer mode. Also, in Block II, the channels may be read or loaded. All these operations may be done with the AGC stopped (using T12) or "on the fly" with computer running since the AGC has a 12 μ s MCT and the Monitor uses about a 4 μs MCT.

Set the location (in Monitor memory, core rope, erasable memory, or channel) to be read or loaded on either the S1 or S2 comparator switches, iggoring all bits not used in the address determination. (For example, the ER-bank bits are ignored for any fixed memory location). If it is desired to read a core rope location, turn off the corresponding bank switch to give access to the rope.

Now set the T12 STOP switch to on (up). This will stop the computer and allow the desired location(s) to be read or loaded by depressing the appropriate read or load switch (to read and load channels, use READ PRESET CHANNEL and LOAD PRESET CHANNEL). Read the contents of the location on the G indicators in Block I. In Block II operation the W register must be used to read the content of the G register because the G register is updated to the next instruction before the AGC is stopped.

If it is desired to read or load a location "on the fly" without stopping the AGC, or if the Monitor is operating with a Block II AGC, set the WRITE W seven-position switch to the S position. Set the S1-S2 switch above it to correspond with the set of S comparator switches used to set up the location. Set the G write pulse switch to on (up) and all other write pulse switches and all the time pulse switches to off (down). The exception here is for the case of reading or loading a channel. In this case the WCH or RCH write pulse switches are used instead of G. Use WCH for loading a channel and RCH for reading a channel.

Note: When reading core ropes in Block I, it is necessary to have the desired bank number in the Bank Register of the AGC. The F BNK indicators on the Monitor may not always represent the contents of the AGC Bank Register (especially if a LOAD or READ PRESET has just been performed with the BANK & S-S ONLY switch in the BANK & S position). To load or verify the content of the Bank Register, load or read location 0015. In Block II operation the desired address is always read since the E BNK and F BNK registers in the AGC are set automatically during the read operation.

Next, depress either the READ PRESET or LOAD PRESET switch to read or load the location. The contents of the location will be displayed in the W register.

3.7.2 Transfering Control

Use the following procedure to force the AGC to transfer control to a given location.

1. Stop the AGC, using one of the stop conditions (see Section 3.7.4).
2. Turn off the stop switch used in step 1.
3. For Block I operation, manually load the AGC Bank Register (location 0015) with the bank number of the desired starting address. In Block II operation, the Bank Register is automatically changed when Step 6 or 7 is performed.
4. Set the desired starting address on either the S1 or S2 comparator switches.
5. Set the S1-S2 switch located below the START PRESET switch to the corresponding position.
6. Depress the START PRESET switch to complete the transfer.
7. If the desired starting location is already displayed on the S indicators, disregard steps 3, 4, and 5 and depress the START S switch.

Depressing START PRESET automatically performs the function of the PROCEED switch. The time counter stop is lifted, and the stop indicators are reset. Depressing START S does not allow the AGC to proceed after performing the transfer control.

3.7.3 The Wild Register

The wild register of the Monitor can be used to display various quantities within the AGC. A specified quantity in the W register can, in turn, be used to stop the AGC using the comparison stop switch W or S & W.

The seven-position WRITE W switch specifies what is displayed in the wild register. The use of each position will be described separately.

In the ALL position the contents of the W register is determined only by the four rows of switches beneath the WRITE W switch. Those numbered 1 through 12 refer to the 12 timing pulses which occur during each MCT. The others each have a letter designation which refers to a write pulse from the AGC. The last switch is a spare. (Note: the WX switch is operational only in Block I, and the RU switch is operational only in the Block II).

Setting a time pulse switch to on (up) will allow the W register to be written into at that time. Setting a write pulse switch to on (up) will display in the W register the content of the write lines during that write pulse. Thus, to observe the content of the G register, set the G switch to on. The twenty-four switches are "OR"ed together: thus, the occurence of the control pluse associated with any of the switches which is in the "on" position will cause the W register to be updated.

In each of the other six settings of the WRITE W switch, these timing and write pulse switches can be used as an added condition for display or for stopping the AGC.

The S position of the WRITE W switch allows the display in the W register of the content of any location in fixed or erasable memory. However, the location must be exercised in order for the display to appear. Set the S1-S2 switch above the WRITE W switch to the corresponding position.

In this case, and in all cases involving the WRITE W switch or the STOP conditions switches, the second row of switches in S1 and S2 have meaning. These switches are used to ignore any bits of the address.

For example, suppose it is desired to monitor a location in erasable memory. The five F BANK bits and the 3 F EXT CHAN bits in the address should be ignored since they are not used in addressing erasable memory (unless it is desired to monitor the erasable location only when the program is in a particular fixed bank). Therefore, set the eight switches in the second row of S1 or S2 to ignore (up). The desired location in erasable memory can then be set up on the top row of switches. (Note: in Block I the ER BANK bits would also be ignored in this case).

As another example, suppose it is desirable to monitor all locations which are being used in fixed bank 7 and that have bits 7, 9, 10, and 11 equal to ones and bits 8 and 12 equal to zero. Thus, it is desired to monitor all locations of the form 07.35 XX. In this case, set bits 7 through 12 and the five bank bits on the first row of the S1 comparator switches. Ignore all the rest of the bits in S1 by setting the corresponding switches in the second row to ignore (up).

The I setting of the WRITE W switch allows the display in the W register of the contents of a given register during a specified subinstruction and during a specified time.

The S & I position of the WRITE W switch allows the contents of a location to be observed during a given subinstruction. The location is set up on either the S1 or S2 comparator switches and the subinstruction is set on the I comparator switches.

The P position, or program step position, of WRITE W is much the same as the S position. The difference is that here the display continues until the next NISQ pulse. Thus, for example, the content of the accumulator might be observed during an entire program step. The program step must be set on the S1 switches. The position of the S1-S2 switch above the WRITE W switch has no effect here.

The P & I position of WRITE W allows the display of the content of a register during a specified subinstruction and during a specified program step.

The P & S position of WRITE W allows the display in the W register of the content of the location specified on S2 during a program step specified on S1. The S1-S2 switch must be set to S2. The location specified on S2 is normally a location in erasable memory.

3.7.4 The Stop Condition Switches

The eleven STOP switches allow the AGC time counter to be stopped under a variety of conditions. The general use of each switch will be explained, and some examples will be given. Note: The ALGA switch on the buffer box must be set to ONE STEP (off) to inhibit restarts which will be caused by stopping the computer.

The T12 STOP causes a time counter stop at the next time 12 or, in other words, at the end of the next MCT after the switch is turned on.

The NISQ STOP causes a time counter stop at the next NISQ command or, in other words, after the present instruction has been completed. It is useful for stepping through a program.

The S1 STOP causes a stop at an address which has been specified on the S1 comparator switches. In this case the bottom row of switches can be used to ignore any parts of the address. Thus, for example, the AGC could be stopped when bit three is present in the address by ignoring all bits except number three, and then specifying bit three as a one.

The S2 STOP is the same as the S1 STOP except that it uses the S2 comparator switches.

Note that, when an S1 or S2 stop is made (in Block II), the S register indicators do not agree with the setting of the switches. The S indicators in this case will actually display the content of the program step on which the stop was made. This is due to a quirk in the computer timing, and it can be confusing when stepping through a program. However, if it is remembered that the Z register always contains the next address, it is possible to determine on which step in the program the AGC has been stopped.

The W STOP causes a time counter stop when the contents of the W register agrees with the value specified on the W comparator switches. This is a very versatile stop condition. As an example, suppose that it is desired to stop the AGC during subinstruction CCSO when the contents of G is plus zero at time 7 (Block I operation). Referring to Appendix A, note that, if the I register is set up with the SQ, ST, and BR bits as shown and all other bits ignored, WRITE W set to I, all the W comparator switches (except the two parity bits) set to specify and "0", the time 7 and write pulse G switches set to on, and the W STOP switch set to on, then a time counter stop will occur when the content of G is plus zero during subinstruction CCSO and only then.

The S & W STOP causes a stop when the S and W registers both agree with the values set up on their respective comparator switches. The S1-S2 switch below it allows the use of either the S1 or S2 comparator switches for the specification of S. Suppose that it is desired to know whether during subinstruction CCSO the contents of G is ever plus zero at time 7, as in the previous example, but this time during a specific CCSO subinstruction. The location of the particular CCSO is taken from the program. The Monitor controls are set exactly as before except that the S & W STOP is used and the address is set up on the S1 or S2 comparators.

The CHAN STOP (Block II only) allows the AGC to be stopped when a particular channel is used. The channel may be set on either S1 or S2 by setting the S1-S2 switch to the corresponding position.

The PARITY STOP causes a stop when a word going to the G register from memory in the AGC has incorrect parity. The parity error test for this stop condition is accomplished within the AGC, which tests the parity of each word as it is taken form memory and written into the G register in the AGC. If a parity error is detected, a signal is generated which indicates a parity alarm on the DSKY (Block I only), This same signal is sent to the PARITY STOP circuit in the Monitor which generates a signal which causes an AGC time counter stop (Block I and Block II).

The I STOP causes a stop when the I register agrees with the setting of the I comparator switches. Thus, for example, the computer can be stopped when a specified subinstruction occurs.

The PROG STEP STOP causes a stop at the end of a program step which has been specified on the S1 comparator switches.

After stopping the AGC time counter with one of the stop condition switches, the stop can be lifted by depressing the PROCEED switch, This also resets the light above the stop switch, except in the case of the PARITY STOP. This indicator is reset by depressing the ERROR RESET switch.

3.7.5 The Meter

The meter on the control panel is used to indicate the percentage of time that the computer is doing whatever is specified by the setting of the six-position switch below it.

With the switch set to CRS CYCLE, the meter indicates the percentage of time that the CRS memory is being strobed.

When the switch is set to the I AGR, W AGR, S1 AGR, or S2 AGR, the meter indicates what percentage of time the I, W, or S registers are in agreement with whatever values have been set on their respective comparator switches.

When set to the MTSB (Magnetic Tape Strobe) position, the meter is deflected when the magnetic tape is running. Thus, it is not necessary to open the rear door to see whether or not the magnetic tape is running.

3.8 Operation in the Trace Mode

The TRACE MODE is used to record on magnetic tape the AGC function which is displayed in the W register.

1. Set the NISQ switch to on to stop the AGC.
2. Set the MODE switch to TRACE.
3. Set up the W register to display the desired AGC function.
4. Set the TRACE TIMING MODE switch to the desired setting.
5. Depress PROCEED.

The three positions of the TRACE TIMING MODE switch are described as follows.

The W FREZ position "freezes" the W register display while the recording is being done. The PGM FREZ position "freezes" or stops the program until the recording is done. In the W FREZ and PGM FREZ position the content of the W register is recorded only after the W register has been updated, whereas in the FREE RUN position the operator can choose a sampling rate at which the W register is recorded. This is done with the FREE RUN PERIOD switch. The operator may select 20-ms, 300-ms, or 3-second intervals.

APPENDIX A - BLOCK I SUBINSTRUCTION CODES AND CONTROL PULSE SEQUENCES

Subinstruction Command	C (SQ) 16,15,14,13	C (ST) 2,1	Action Time	BR Commands	CONTROL PULSE SEQUENCE
STD 2	X X X X	1 0	1.		R~~Z~~ WS WY CI
			3.		CLG*
			4.		RU W~~Z~~
			7.		RSC RG WB WP
			8.		GP TP
			9.		RB WSC WG
			11.		NISQ
TC 0	0 0 0 0	0 0	1.		RB WS WY CI
			3.		CLG*
			4.		RA WOVI
			7.		RG RSC WB WP
			8.		GP TP R~~Z~~ WQ
			9.		RB WSC WG
			10.		RU W~~Z~~
			11.		NISQ
XCH 0	0 0 1 1	0 0	1.		RB WS
			2.		RA WP
			3.		CLG*
			4.		WP2
			7.		RSC RG WB WP
			8.		GP TP
			9.		RA WSC WG RP2
			10.		RB WA WOVI
			11.		ST2

CS 0	1 1 0 0	0 0	1.		RB WS
			3.		CLG*
			7.		RSC RG WB WP
			8.		GP TP
			9.		RB WSC WG
			10.		RC WA WOVI
			11.		ST2
TS 0	1 1 0 1	0 0	1.		RB WS
			2.		RA WB WP TOV
			3.		CLG*
			4.	0 0	----
			4.	1 1	----
			4.	0 1	RZ WY CI
			4.	1 0	RZ WY CI
			5.	0 0	----
			5.	1 1	----
			5.	0 1	R1B WA
			5.	1 0	R1C WA
			7.	0 0	----
			7.	1 1	----
			7.	0 1	RU WZ
			7.	1 0	RU WZ
			8.		GP
			9.		RB WSC WG
			10.		RA WOVI
			11.		ST2

MSK 0	1 1 1 1	0 0	1.		RB WS
			2.		RA WB
			3.		CLG*
			4.		RC WY
			7.		RSC RG WB WP
			8.		RU RC WA GP TP
			10.		RA WB
			11.		RC WA WOVI ST2
AD 0	1 1 1 0	0 0	1.		RB WS
			2.		RA WY
			3.		CLG*
			7.		RSC RG WB WP
			8.		GP TP RB WX
			9.		RB WSC WG
			11.		RU WA WOVI WOVC ST2
NDX 0	0 0 1 0	0 0	1.		RB WS
			3.		CLG*
			4.		RA WOVI
			7.		RSC RG WB WP
			8.		GP TP
			9.		RB WSC WG
			10.		TRSM
			11.		ST1

NDX 1	0 0 1 0	0 1	1.		RZ WS WY CI
			3.		CLG*
			4.		RU WZ
			6.		RB WY
			7.		RSC RG WB WP
			8.		GP TP RB WX
			9.		RB WSC WG
			11.		RU WB WOVI NISQ
CCS 0	0 0 0 1	0 0	1.		RB WS
			2.		RZ WY
			3.		CLG*
			6.		RSC RG WB WP TSGN
			7.	X 0	RC TMZ
			7.	X 1	RB TMZ
			8.	0 0	GP TP
			8.	1 0	R1 WX GP TP
			8.	0 1	R2 WX GP TP
			8.	1 1	R1 R2 WX GP TP
			9.		RB WSC WG
			10.	0 0	RC WA
			10.	1 0	R1C WA
			10.	0 1	RB WA
			10.	1 1	R1C WA
			11.		RU ST1 WZ

CCS 1	0 0 0 1	0 1	1.		R~~Z~~ WS WY CI
			3.		CLG*
			4.		RU W~~Z~~
			5.		RA WY CI
			7.		RSC RG WB WP
			8.		RU WB GP TP
			10.		RC WA WOVI
			11.		RG RSC WB NISQ
SU 0	1 0 1 1	0 0	1.		RB WS
			2.		RA WY
			3.		CLG*
			7.		RSC RG WB WP
			8.		GP TP RC WX
			9.		RB WSC WG
			11.		RU WA WOVI WOVC ST2
MP 0	1 0 0 1	0 0	1.		RB WS
			2.		RA WB CLG* TSGN
			3.		RSC WG
			4.	X 0	RB WLP
			4.	X 1	RC WLP
			5.		RLP WA
			7.	X 0	RG WY WP
			7.	X 1	RG WB WP
			8.	X 0	GP TP
			8.	X 1	RC WY GP TP
			9.		RU WB TSGN2
			10.	X 0	RA WLP TSGN

			10.	X 1	RA RB14 WLP TSGN
			11.	0 0	WALP ST1
			11.	0 1	R1 R1C WALP ST1
			11.	1 0	RU WALP ST1
			11.	1 1	RU WALP ST1
MP 1	1 0 0 1	0 1	1.		RA WY
			2.		RLP WA TSGN
			3.	X 0	----
			3.	X 1	RB WX
			4.		RA WLP
			5.		RLP TSGN
			6.		RU WALP
			7.		RA WY
			8.	X 0	----
			8.	X 1	RB WX
			9.		RLP WA
			10.		RA WLP CTR
			11.		RU WALP ST1
MP 3	1 0 0 1	1 1	1.		R~~Z~~ WS WY CI
			2.		RLP TSGN
			3.		CLG*
			4.		RU W~~Z~~
			5.		RA WY
			6.	X 0	----
			6.	X 1	RB WX
			7.		RG RSC WB WP
			8.		RLP WA GP TP
			9.		RB WSC WG

			10.		RA WLP
			11.		RU WALP NISQ
DV 0	1 0 1 0	0 0	1.		RB WS
			2.		RA WB CLG* TSGN
			3.		RSC WG
			4.	X 0	RC WA
			4.	X 1	----
			5.	X 0	R1 WLP
			5.	X 1	R2 WLP
			6.		RA WQ
			7.		RG WB WP TSGN
			8.		RB WA GP TP
			9.	X 0	RLP R2 WB
			9.	X 1	----
			10.	X 0	RB WLP
			10.	X 1	RC WA
			11.		R1 WB ST1
DV 1	1 0 1 0	0 1	1.		R22 WS CLG*
			2.		RQ WG
			3.		RG RSB WQ WY
			4.		RA WX
			5.		RLP TSGN2
			7.		RU TSGN
			8.	X 0	----
			8.	X 1	RU WQ
			9.	X 0	RB RSB WG
			9.	X 1	RB WG
			10.		RG WB TSGN

			11.	0 0	RC WA ST1 ST2
			11.	0 1	RB WA ST1 ST2
			11.	1 0	RC WA ST2
			11.	1 1	RB WA ST2
RUPT 1	0 0 1 1	0 1	1.		R24 WS WY CI
			3.		CLG*
			9.		R$\not{Z}$ WG
			10.		RU W$\not{Z}$
			11.		ST1 ST2
RUPT 3	0 0 1 1	1 1	1.		R$\not{Z}$ WS
			2.		RRPA W$\not{Z}$
			3.		R$\not{Z}$ KRPT CLG*
			9.		RB WSC WG
			11.		ST2
RSM	0 0 1 0	1 1	1.		R24 WS
			3.		CLG*
			7.		RG W$\not{Z}$
			11.		NISQ
GO	0 0 0 0	0 1	1.		RSTRT WS WY CI
			3.		CLG*
			4.		RA WOVI
			7.		RG RSC WB WP
			8.		GP TP R$\not{Z}$ WQ
			9.		RB WSC WG
			10.		RU W$\not{Z}$
			11.		NISQ

TCSA	0 0 0 0	1 1	1.		RSA WS WY CI
			3.		CLG*
			4.		RA WOVI
			7.		RG RSC WB WP
			8.		GP TP RZ WQ
			9.		RB WSC WG
			10.		RU WZ
			11.		NISQ
PINC	X X X X	X X	1.		RSCT WS
			3.		CLG*
			4.		RB1 WY
			6.		RG* WX* WP
			7.		TP
			8.		WP
			9.		RU* CLG* WP*
			10.		RU* WG* WOVR*
MINC	X X X X	X X	1.		RSCT WS
			3.		CLG*
			4.		R1C WY
			6.		RG* WX* WP
			7.		TP
			8.		WP
			9.		RU* CLG* WP*
			10.		RU* WG* WOVR

SHINC	X X X X	X X	1.		RSCT WS
			3.		CLG*
			4.		WY
			6.		RG* WY* WX* WP TSGN3
			7.		TP
			8.		WP
			9.		RU* CLG* WP*
			10.		RU* WG* WOVR
SHANC	X X X X	X X	1.		RSCT WS
			3.		CLG*
			4.		WY
			6.		RG* WY* WX* WP TSGN3
			7.		TP CI
			8.		WP
			9.		RU* CLG* WP*
			10.		RU* WG* WOVR
OINC	X X X X	X X	1.		WS
			3.		CLG*
			7.		RSC RG
LINC	X X X X	X X	1.		WS
			3.		CLG*
			7.		WSC WG WP
			8.		GP

APPENDIX B - BLOCK II SUBINSTRUCTION CODES AND CONTROL PULSE SEQUENCES

Subinstruction Command	C (SQ) EXT	16,14,13	12,11,10	C (ST) 3,2,1	Action Time	BR Commands	CONTROL PULSE SEQUENCE
STD 2	X	X X X	X X X	0 1 0	1.		RZ WY12 CI
					2.		RSC WG NISQ
					6.		RU WZ
					8.		RAD WB WS
TC 0	0	0 0 0	X X X	0 0 0	1.		RB WY12 CI
					2.		RSC WG NISQ
					3.		RZ WQ
					6.		RU WZ
					8.		RAD WB WS
GOJ 1	0	0 0 0	X X X	0 0 1	2.		RSC WG
					8.		RSTRT WS WB
TCSAJ 3	0	0 0 0	X X X	0 1 1	2.		RSC WG
					8.		WS WZ ST2
CCS 0	0	0 0 1	0 0 X	0 0 0	1.		RL10BB WS
					2.		RSC WG
					5.		RG WB TSGN TMZ TPZG
					7.	0 0	RZ WY12
					7.	0 1	RZ WY12 PONEX
					7.	1 0	RZ WY12 PTWOX
					7.	1 1	RZ WY12 PONEX PTWOX
					8.		RU WZ WS
					9.		RB WG
					10.	0 0	RB WY MONEX CI ST2
					10.	X 1	WY ST2

		10.	1 0	RC WY MONEX CI ST2
		11.		RU WA
TCF 0	0 0 0 1 0 1 X	0 0 0	1.	RB WY12 CI
	0 0 0 1 1 0 X		2.	RSC WG NISQ
	0 0 0 1 1 1 X		6.	RU WZ
			8.	RAD WB WS
DAS 0	0 0 1 0 0 0 X	0 0 0	1.	RL10BB WS WY12 MONEX CI
			2.	RSC WG
			3.	RA WB
			4.	RL WA
			5.	RU WL
			6.	RG WY A2X
			7.	RB WA
			8.	RL WB
			9.	RU WSC WG TOV
			10.	0 0 RA WY ST1
			10.	0 1 RA WY ST1 PONEX
			10.	1 0 RA WY ST1 PONEX
			10.	1 1 RA WY ST1
DAS 1	0 0 1 0 0 0 X	0 0 1	1.	RL10BB WS
			2.	RSC WG
			3.	RU WA
			5.	RG WY A2X
			6.	RU WG WSC TOV
			7.	0 0 WA
			7.	0 1 WA RB1
			7.	1 0 WA R1C

			7.	1 1	WA
			8.		RZ WS ST2
			9.		RC TMZ
			10.	X 0	WL
			11.	X 1	RU WA
LXCH 0	0 0 1 0 0 1 X	0 0 0	1.		RL10BB WS
			2.		RSC WG
			3.		RL WB
			5.		RG WL
			7.		RB WSC WG
			8.		RZ WS ST2
INCR 0	0 0 1 0 1 0 X	0 0 0	1.		RL10BB WS
			2.		RSC WG
			5.		RG WY TSGN TMZ TPZG
			6.		PONEX
			7.		RU WSC WG WOVR
			8.		RZ WS ST2
ADS 0	0 0 1 0 1 1 X	0 0 0	1.		RL10BB WS
			2.		RSC WG
			5.		RG WY A2X
			6.		RU WSC WG TOV
			7.	0 0	WA
			7.	0 1	WA RB1
			7.	1 0	WA R1C
			7.	1 1	WA
			8.		RZ WS ST2
			9.		RC TMZ
			11.		RU WA

CA 0	0 0 1 1 X X X	0 0 0	2.		RSC WG
			7.		RG WB
			8.		RZ WS ST2
			9.		RB WG
			10.		RB WA
CS 0	0 1 0 0 X X X	0 0 0	2.		RSC WG
			7.		RG WB
			8.		RZ WS ST2
			9.		RB WG
			10.		RC WA
NDX 0	0 1 0 1 0 0 X	0 0 0	2.		RSC WG
			5.		TRSM
			7.		RG WB
			8.		RZ WS
			9.		RB WG
			10.		ST1
NDX 1	0 1 0 1 0 0 X	0 0 1	1.		RZ WY12 CI
			2.		RSC WG NISQ
			3.		RB WZ
			4.		RA WB
			5.		RZ WA
			6.		RU WZ
			7.		RG WY A2X
			8.		RU WS
			9.		RB WA
			10.		RU WB

RSM 3	0 1 0 1 0 0 X	0 1 1	1.	R15 WS
			2.	RSC WG NISQ
			5.	RG WZ
			6.	RB WG
			8.	RAD WB WS
DXCH 0	0 1 0 1 0 1 X	0 0 0	1.	RL10BB WS WY12 MONEX CI
			2.	RSC WG
			3.	RL WB
			5.	RG WL
			7.	RB WSC WG
			8.	RU WS WB
			10.	ST1
DXCH 1	0 1 0 1 0 1 X	0 0 1	1.	RL10BB WS
			2.	RSC WG
			3.	RA WB
			5.	RG WA
			7.	RB WSC WG
			8.	RZ WS ST2
TS 0	0 1 0 1 1 0 X	0 0 0	1.	RL10BB WS
			2.	RSC WG
			3.	RA WB TOV
			4.	0 0 RZ WY12
			4.	0 1 RZ WY12 CI
			4.	1 0 RZ WY12 CI
			4.	1 1 RZ WY12
			5.	0 1 RB1 WA
			5.	1 0 R1C WA
			6.	RU WZ

									7.		RB WSC WG
									8.		RZ WS ST2
XCH 0	0	1	0	1	1	1	X	0 0 0	1.		RL10BB WS
									2.		RSC WG
									3.		RA WB
									5.		RG WA
									7.		RB WSC WG
									8.		RZ WS ST2
AD 0	0	1	1	0	X	X	X	0 0 0	2.		RSC WG
									7.		RG WB
									8.		RZ WS ST2
									9.		RB WG
									10.		RB WY A2X
									11.		RU WA
MSK 0	0	1	1	1	X	X	X	0 0 0	2.		RSC WG
									3.		RA WB
									4.		RC WA
									7.		RG WB
									8.		RZ WS ST2
									9.		RC RA WY
									10.		RU WB
									11.		RC WA
READ 0	1	0	0	0	0	0	0	0 0 0	1.		RL10BB WS
									2.		RA WB
									3.		WY
									4.		RCH WB
									5.		RB WA
									6.		RA WB

		8.		RZ WS ST2
WRITE 0	1 0 0 0 0 0 1 0 0 0	1.		RL10BB WS
		2.		RA WB WG
		3.		WY
		4.		RCH WB
		5.		RA WCH
		6.		RA WB
		8.		RZ WS ST2
RAND 0	1 0 0 0 0 1 0 0 0 0	1.		RL10BB WS
		2.		RA WB
		3.		RC WY
		4.		RCH WB
		5.		RC RU WA
		6.		RA WB
		7.		RC WA
		8.		RZ WS ST2
WAND 0	1 0 0 0 0 1 1 0 0 0	1.		RL10BB WS
		2.		RA WB
		3.		RC WY
		4.		RCH WB
		5.		RC RU WA
		6.		RA WB
		7.		RC WA WCH
		8.		RZ WS ST2
ROR 0	1 0 0 0 1 0 0 0 0 0	1.		RL10BB WS
		2.		RA WB
		3.		RB WY
		4.		RCH WB

			5.		RB RU WA
			6.		RA WB
			8.		RZ WS ST2
WOR 0	1 0 0 0 1 0 1	0 0 0	1.		RL10BB WS
			2.		RA WB
			3.		RB WY
			4.		RCH WB
			5.		RB RU WA WCH
			6.		RA WB
			8.		RZ WS ST2
RXOR 0	1 0 0 0 1 1 0	0 0 0	1.		RL10BB WS
			2.		RA WB
			3.		RC RCH WY
			4.		RCH WB
			5.		RA RC WG
			7.		RG WB
			8.		RZ WS ST2
			9.		RC WG
			10.		RU WB
			11.		RC RG WA
RUPT 0	1 0 0 0 1 1 1	0 0 0	1.		R15 WS
			2.		RSC WG
			9.		RZ WG
			10.		ST1
RUPT 1	1 0 0 0 1 1 1	0 0 1	1.		R15 RB2 WS
			2.		RSC WG
			3.		RRPA WZ

			8.		RZ WS ST2
			9.		RB WG KRPT
DV 0	1 0 0 1 0 0 X	0 0 0	1.		RA WB TSGN TMZ
			2.	0 X	RC WA TMZ DVST
			2.	1 X	DVST
			3.		RU WB STAGE
DV 1	1 0 0 1 0 0 X	0 0 1	4.	X 0	RL WB
			4.	X 1	RL WB TSGN
			5.	0 X	RB WY B15X
			5.	1 X	RC WY B15X Z16
			6.		RU WL TOV
			7.		RG RSC WG TSGN
			8.	X 0	RA WY PONEX
			8.	X 1	RA WY
			9.	0 X	RB WA
			9.	1 X	RC WA Z15
			10.		RU WB
			11.		RL WYD
			12.		RU WL
			1.		L2GD RB WYD A2X PIFL
			2.	0 X	RG WL TSGU DVST CLXC
			2.	1 X	RG WL TSGU DVST RB1F
			3.		RU WB STAGE
DV 3	1 0 0 1 0 0 X	0 1 1	4.		L2GD RB WYD A2X PIFL
			5.	0 X	RG WL TSGU CLXC
			5.	1 X	RG WL TSGU RB1F
			6.		RU WB

			7.		L2GD RB WYD A2X PIFL
			8.	0 X	RG WL TSGU CLXC
			8.	1 X	RG WL TSGU RB1F
			9.		RU WB
			10.		L2GD RB WYD A2X PIFL
			11.	0 X	RG WL TSGU CLXC
			11.	1 X	RG WL TSGU RB1F
			12.		RU WB
			1.		L2GD RB WYD A2X PIFL
			2.	0 X	RG WL TSGU DVST CLXC
			2.	1 X	RG WL TSGU DVST RB1F
			3.		RU WB STAGE
DV 7	1 0 0 1 0 0 X	1 1 1	4.		L2GD RB WYD A2X
			5.	0 X	RG WL TSGU CLXC
			5.	1 X	RG WL TSGU RB1F
			6.		RU WB
			7.		L2GD RB WYD A2X PIFL
			8.	0 X	RG WL TSGU CLXC
			8.	1 X	RG WL TSGU RB1F
			9.		RU WB
			10.		L2GD RB WYD A2X PIFL
			11.	0 X	RG WL TSGU CLXC
			11.	1 X	RG WL TSGU RB1F
			12.		RU WB
			1.		L2GD RB WYD A2X PIFL
			2.	0 X	RG WL TSGU DVST CLXC
			2.	1 X	RG WL TSGU DVST RB1F

			3.		RU WB STAGE
DV 6	1 0 0 1 0 0 X	1 1 0	4.		L2GD RB WYD A2X PIFL
			5.	0 X	RG WL TSGU CLXC
			5.	1 X	RG WL TSGU RB1F
			6.		RU WB
			7.		L2GD RB WYD A2X PIFL
			8.	0 X	RG WL TSGU CLXC
			8.	1 X	RG WL TSGU RB1F
			9.		RU WB
			10.		L2GD RB WYD A2X PIFL
			11.	0 X	RG WL TSGU CLXC
			11.	1 X	RG WL TSGU RB1F
			12.		RU WB
			1.		L2GD RB WYD A2X PIFL
			2.	0 X	RG WL TSGU DVST CLXC
			2.	1 X	RG WL TSGU DVST RB1F
			3.		RU WB STAGE
DV 4	1 0 0 1 0 0 X	1 0 0	4.		L2GD RB WYD A2X PIFL
			5.	0 X	RG WB WA TSGU CLXC
			5.	1 X	RG WB WA TSGU RB1F
			6.		RZ TOV
			7.	0 1	RC WA
			7.	1 X	RC WA
			8.		RZ WS ST2 TSGN RSTSTG
			9.		RU WB WL
			10.	0 X	RC WL

BZF 0	1 0 0 1 0 1 X	0 0 0	1.	RA WG TSGN TMZ
	1 0 0 1 1 0 X		2.	TPZG
	1 0 0 1 1 1 X		3.	RSC WG
			5. X 1	RB WY12 CI
			6. X 1	RU WZ
			8. X 0	RZ WS ST2
			8. X 1	RAD WB WS NISQ
MSU 0	1 0 1 0 0 0 X	0 0 0	1.	RL10BB WS
			2.	RSC WG
			5.	RG WB
			6.	RC WY CI A2X
			7.	RUS WA TSGN
			8.	RZ WS ST2
			9.	RB WG
			10. 1 X	RA WY MONEX
			11.	RUS WA
QXCH 0	1 0 1 0 0 1 X	0 0 0	1.	RL10BB WS
			2.	RSC WG
			3.	RQ WB
			5.	RG WQ
			7.	RB WSC WG
			8.	RZ WS ST2
AUG 0	1 0 1 0 1 0 X	0 0 0	1.	RL10BB WS
			2.	RSC WG
			5.	RG WY TSGN TMZ TPZG
			6. 0 X	PONEX
			6. 1 X	MONEX
			7.	RU WSC WG WOVR

		8.		RZ WS ST2
DIM 0	1 0 1 0 1 1 X	0 0 0	1.		RL10BB WS
			2.		RSC WG
			5.		RG WY TSGN TMZ TPZG
			6.	0 0	MONEX
			6.	1 0	PONEX
			7.		RU WSC WG WOVR
			8.		RZ WS ST2
DCA 0	1 0 1 1 X X X	0 0 0	1.		RB WY12 MONEX CI
			2.		RSC WG
			7.		RG WB
			8.		RU WS
			9.		RB WG
			10.		RB WL ST1
DCA 1	1 0 1 1 X X X	0 0 1	2.		RSC WG
			7.		RG WB
			8.		RZ WS ST2
			9.		RB WG
			10.		RB WA
DCS 0	1 1 0 0 X X X	0 0 0	1.		RB WY12 MONEX CI
			2.		RSC WG
			7.		RG WB
			8.		RU WS
			9.		RB WG
			10.		RC WL ST1
DCS 1	1 1 0 0 X X X	0 0 1	2.		RSC WG
			7.		RG WB

		8.		RZ WS ST2
		9.		RB WG
		10.		RC WA
NDXX 0	1 1 0 1 X X X	0 0 0	2.		RSC WG
			7.		RG WB
			8.		RZ WS
			9.		RB WG
			10.		ST1
NDXX 1	1 1 0 1 X X X	0 0 1	1.		RZ WY12 CI
			2.		RSC WG NISQ
			3.		RB WZ
			4.		RA WB
			5.		RZ WA
			6.		RU WZ
			7.		RG WY A2X
			8.		RU WS
			9.		RB WA
			10.		RU WB EXT
SU 0	1 1 1 0 0 0 X	0 0 0	2.		RSC WG
			7.		RG WB
			8.		RZ WS ST2
			9.		RB WG
			10.		RC WY A2X
			11.		RU WA
BZMF 0	1 1 1 0 0 1 X	0 0 0	1.		RA WG TSGN TMZ
	1 1 1 0 1 0 X		2.		TPZG
	1 1 1 0 1 1 X		3.		RSC WG

			5.	0 1	RB WY12 CI
			5.	1 0	RB WY12 CI
			5.	1 1	RB WY12 CI
			6.	0 1	RU WZ
			6.	1 0	RU WZ
			6.	1 1	RU WZ
			8.	0 0	RZ WS ST2
			8.	0 1	RAD WB WS NISQ
			8.	1 0	RAD WB WS NISQ
			8.	1 1	RAD WB WS NISQ
MP 0	1 1 1 1 X X X	0 0 0	2.		RSC WG
			3.		RA WB TSGN
			4.	0 X	RB WL
			4.	1 X	RC WL
			7.		RG WB TSGN2
			8.		RZ WS
			9.	0 0	RB WY
			9.	0 1	RB WY CI
			9.	1 0	RB WY CI
			9.	1 1	RC WY
			10.		RU WB TSGN ST1 NEACON
			11.	0 X	WA
			11.	1 X	WS RB1 R1C L16
MP 1	1 1 1 1 X X X	0 0 1	1.		ZIP
			2.		ZAP
			3.		ZIP
			4.		ZAP

			5.		ZIP
			6.		ZAP
			7.		ZIP
			8.		ZAP
			9.		ZIP
			10.		ZAP ST1 ST2
			11.		ZIP
MP 3	1 1 1 1 X X X	0 1 1	1.		ZAP
			2.		ZIP NISQ
			3.		ZAP
			4.		RSC WG
			5.		RZ WY12 CI
			6.		RU WZ TL15 NEACOF
			7.	1 X	RB WY A2X
			8.		RAD WB WS
			9.		RA
			10.		RL
			11.	1 X	RU WA
PINC	X X X X X X X	X X X	1.		RSCT WS
			2.		RSC WG
			5.		RG WY TSGN TMZ TPZG
			6.		PONEX
			7.		RU WSC WG WOVR
			8.		RB WS
PCDU	X X X X X X X	X X X	1.		RSCT WS
			2.		RSC WG
			5.		RG WY TSGN TMZ TPZG

			6.		CI
			7.		RUS WSC WG WOVR
			8.		RB WS
MINC	X X X X X X X	X X X	1.		RSCT WS
			2.		RSC WG
			5.		RG WY TSGN TMZ TPZG
			6.		MONEX
			7.		RU WSC WG WOVR
			8.		RB WS
MCDU	X X X X X X X	X X X	1.		RSCT WS
			2.		RSC WG
			5.		RG WY TSGN TMZ TPZG
			6.		MONEX CI
			7.		RUS WSC WG WOVR
			8.		RB WS
DINC	X X X X X X X	X X X	1.		RSCT WS
			2.		RSC WG
			5.		RG WY TSGN TMZ TPZG
			6.	0 0	MONEX POUT
			6.	1 0	PONEX MOUT
			6.	X 1	ZOUT
			7.		RU WSC WG WOVR
			8.		RB WS
SHINC	X X X X X X X	X X X	1.		RSCT WS
			2.		RSC WG
			5.		RG WYD TSGN
			7.		RUS WSC WG WOVR
			8.		RB WS

SHANC	X X X X X X X	X X X	1.		RSCT WS
			2.		RSC WG
			5.		RG WYD TSGN CI
			7.		RUS WSC WG WOVR
			8.		RB WS
INOTRD	X X X X X X X	X X X	1.		WS
			2.		RSC WG
			5.		RCH
			8.		RB WS
INOTLD	X X X X X X X	X X X	1.		WS
			2.		RSC WG
			5.		RCH
			7.		WCH
			8.		RB WS
FETCH 0	X X X X X X X	0 0 0	1.		R6 WS
			2.		RSC WG WY ST1
			4.		WSC
			8.		WS
FETCH 1	X X X X X X X	0 0 1	2.		RSC WG
			7.		RG
			8.		RB WS U2BBK
			10.		RBBK
STORE 0	X X X X X X X	0 0 0	1.		R6 WS
			2.		RSC WG WY ST1
			4.		WSC
			8.		WS
STORE 1	X X X X X X X	0 0 1	2.		RSC WG

			4.		WSC
			7.		RG
			8.		RB WS U2BBK
			9.		WG
			10.		RBBK

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