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Multi-scale, Multi-physics Modeling and Simulation of Single Event Effects in Digital Electronics: from Particles to Systems

J.L. Autran and D. Munteanu

Abstract— **This review paper aims to provide a survey of modeling and simulation of single-event effects (SEEs) in digital electronics at device, circuit and system levels. It primarily focuses on the specific multi-scale, multi-physics, multi-domain nature of SEEs and on the main underlying physical mechanisms that lead to the occurrence of single events in digital devices and circuits. This review addresses the different ways to model and simulate both in space and time this complex sequence of mechanisms from the particle-material interaction up to the electrical response of a given electronics device, circuit, or system. It highlights the specific features of each methodology, and discusses simulation requirements, code or model inputs and expected outputs.**

Index Terms— **Circuit simulation, compact models, device modeling and simulation, digital circuits, digital single-event transient, radiation effects, single-event effects, soft error rate, transport models, radiation transport codes.**

I. Introduction

SINGLE event effects (SEEs) designate a set of multi-physics and multi-scale phenomena that take place in a microelectronic device, component, subsystem, or system (digital or analog) impacted by a single energetic particle and that result in any measurable or observable change in its state, operation, or performance. SEEs were reported for the first time in the 1950s during nuclear weapon testing and observed in space electronics from the 60s [1-4]. Terrestrial cosmic-rays (atmospheric radiation) and traces of radioactive impurities (alpha-particle emitters) in circuit materials were identified later in the 70s-80s as the two major sources of SEEs at ground level [5-10]. In the 90s, the interaction of low-energy (thermal) cosmic-ray-induced neutrons with the ^{10}B isotope potentially present in device materials was also identified as another major source of SEEs [11].

In recent decades, the growing significance of SEEs in the reliability of modern electronics can be attributed to the extreme miniaturization of complementary metal-oxide-semiconductor (CMOS) devices combined with the increase of the circuit integration (i.e., the number of transistors per unit area) [12,13,14]. As feature-size scales down, the per-bit cross-sectional area exposed to an incoming ionizing particle decreases. This is accompanied by a reduction in the volume where energy is deposited by the traversing particle, and by an increase of the particle's region of influence within the affected device, cell, or circuit [12]. The ongoing reduction of the critical charge as devices shrink [12,14,15,16], has made them increasingly susceptible to natural or artificial radiation in general and down to the most tenuous levels, as encountered for example at terrestrial ground level.

Alongside the experimental aspects, modeling and simulation have long been used for better understanding the effects of radiation on the operation of devices and circuits [17-22]. Because of its increasingly predictive capacity, which goes hand in hand with the power of computational tools and advances in physical modeling, simulation offers the possibility of reducing radiation experiments and of testing hypothetical devices or conditions, which are not feasible (or not easily measurable) by experiments. For the study of SEEs in future devices for which experimental investigation is still limited, numerical simulation is an ideal investigation tool for providing physical insights and predicting the operation of future devices expected at the end of the roadmap [13,21].

As CMOS technologies move down to the nanometer scale and circuits become more complex, it becomes necessary to adopt a truly multi-physics and multi-scale simulation approach to capture the essential physics of SEEs, from the particle-matter interaction to the response of a digital circuit or system. This raises several challenges in the development of powerful simulation tools and in the management of interactions between simulation levels. In brief, multiscale simulations can be linked in two ways: i) by incorporating direct links between input/output flows of different simulation types, or ii) by transforming the results of a given simulation level into a simplified form and feeding them as input to another simulation level. A hierarchical structure of the interactions between simulation levels offers advantages in terms of efficiency, while also providing design insights [23].

This paper deals with this important issue of modeling and simulation of SEEs in digital electronics at device, circuit and system levels. The paper primarily addresses key topics related to single-event transients (SETs) and single-event upsets (SEUs) occurring in digital devices and circuits. An SET is a temporary and unintended voltage or current fluctuation that occurs when ionizing particles, such as cosmic rays or high-energy particles from nuclear reactions, interact with the

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semiconductor materials inside electronic devices [24,25]. These interactions can disrupt the normal operation of digital circuits, causing a momentary change in the logic state of a device/circuit or an operation interrupt. The other numerous effects induced by single events in electronics are only briefly mentioned at the beginning of the article to provide an overview of SEEs and to better contextualize the topics discussed here. The paper is organized as follows. Section II primarily focuses on the specific multi-scale, multi-physics, multi-domain nature of SEEs and on the main underlying physical mechanisms that lead to the occurrence of soft errors in digital circuits. In Section III, a meticulous review will address the different ways to model and simulate both in space and time this complex sequence of mechanisms from the particle-material interaction up to the electrical response of a given circuit. Section IV explores in detail the main approaches for the modeling and simulation of SEEs at device and circuit cell levels such as sensitive volume-based models, the so-called diffusion-collection method, the random-walk drift diffusion approach, and Technology Computer-Aided Design (TCAD) simulation. In section V we examine a few approaches of mixed-mode and circuit simulation used to investigate SEEs at circuit level. Section VI presents the modeling of the Soft Error Rate (SER) as well as different approaches of critical charge modeling in both memory circuits and in combinational logic. Finally, in section VII we briefly review modeling and simulation approaches of SEEs at the system-level.

II. Understanding the Nature of the SEE Problem

A. Definition and classification

We start by a general definition of a Single-Event Effect, followed by a classification of the different types of SEEs.

- A Single-Event Effect is initiated by the passage of a single energetic particle through the volume of an electronic device.
- The striking particle may be an elementary particle (proton, neutron, muon, electron, …), or an ion (alpha particle, heavy ion).
- An SEE is created if the result of the interaction of the particle with the device or circuit interferes with its electrical operation, causing or not an observable functional error.
- An SEE can result in a reversible (non-permanent) or irreversible (permanent) change in device or circuit operation. In the first case, the error is recoverable and is qualified as a "soft error"; in the second case, the error is generally the result of an unrecoverable damage and one speaks about "hard error".

The recent revision of the JEDEC standard JESD89B [24] proposes a definition and a classification of the different types of SEEs, resulting from several years of discussion and effort to try to standardize this ensemble of technical terms. These are summarized in Fig. 1 and their extensive definitions, according to the JEDEC standard, are given below (all quotes in italics correspond to definitions directly taken from [24]). Soft errors (SE) include single-event transients (SET), single-event upsets (SEU), single-bit upsets (SBU), single-cell upsets (SCU), multiple-bit upsets (MBU), multiple-cell upsets (MCU), single-event transients (SET) that, if latched, become SEU [24]:

- Single-event upset (SEU): "*A non-permanent error caused by a state change of a latch, flop, memory cell or other bistable element from the particle strike. The energetic strike can occur directly on the circuit element or propagate to that circuit (see SET).*"
- Single-bit upset (SBU): "*A SEU in which the observed error is a single logical or data bit*."
- Single-cell upset (SCU): "*A SEU where only one cell or logic element (latch, flip flop, etc.) is upset (compare to MCU).*"
- Multiple-bit upset (MBU): "*A single event that induces upset of multiple-cells where two or more of the upsets occur in the same logical word (or frame/column/sector, etc. for field-programmable gate arrays (FPGAs)). NOTE An MBU is a logical manifestation of a single event.*"
- Multiple-cell upset (MCU): "*A single event that induces several cells (e.g., memory cells or flip-flops) in an integrated circuit (IC) to flip their state at one time.*"
  Single-event functional interrupt (SEFI): "*A single event that causes the component to reset, lock-up, or otherwise malfunction in a detectable way, but does not result in permanent damage (i.e. hard error). Note that a SEFI is often associated with an SBU/MBU in a control bit or register, whereas a SEL is caused by the turn-on of a parasitic thyristor. Many SEFI events can be cleared with a component reset operation. In cases where resetting some configuration registers requires a complete power cycle of the device, it can be difficult to distinguish between a SEFI and a SEL (see below). A SEFI event does not necessarily result in an extended increase in operational current like a high current SEL.*"
- Single-event transient (SET): "*A time dependent radiation induced spurious current or voltage signal on a circuit node. A digital SET (DSET) occurs when an SET in a combinational logic gate (along data or control paths) propagates and is latched to create an error in the output of a sequential element. An analog SET (ASET) is a spurious signal in an analog circuit (e.g., a spurious signal on an input-output (IO) pin, etc.) that causes an erroneous output.*"

Single Event Hard errors (SEHE) include single event gate oxide ruptures (SEGR), single event dielectric ruptures (SEDR), single event burnouts (SEB) and destructive single event latchups (SEL) [24]:

- Single-event gate rupture (SEGR): "*An event in which a single energetic particle strike results in a breakdown and subsequent conducting path through the gate oxide of a metal-oxide-semiconductor (MOS) transistor.*"
- Single-event dielectric rupture (SEDR): "*An event in which conducting path is created in a dielectric material from a single energetic particle strike.*"
- Single-event burnout (SEB): "*An event in which a single*

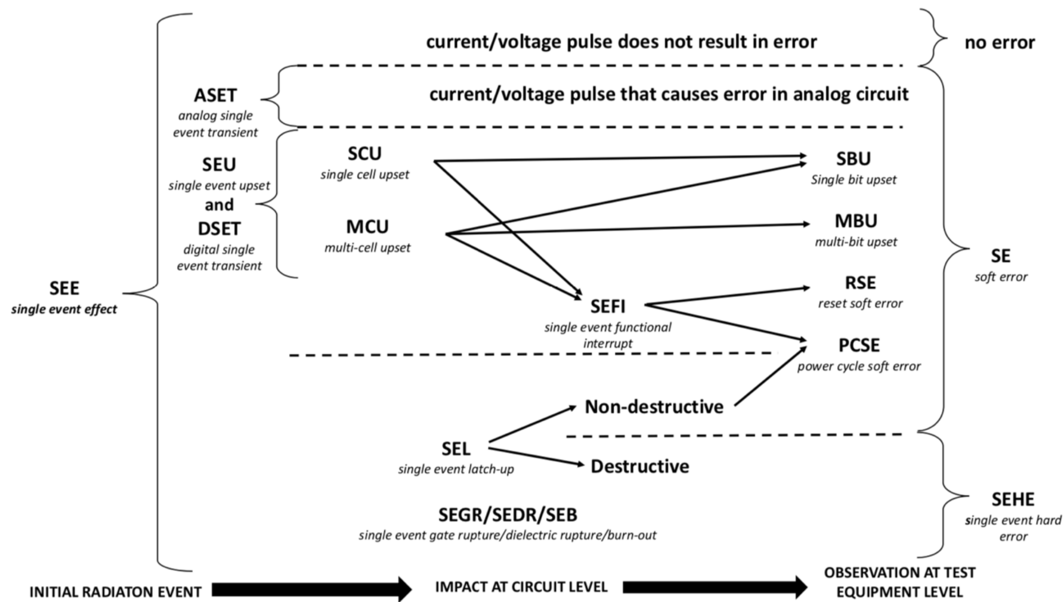


Fig. 1. Diagram of terms used to describe single event effects. (After JEDEC Standard JESD89B [24], © JEDEC 2021.)

energetic particle strike induces a localized high-current state in a device, resulting in catastrophic failure."

- Single-event latchup (SEL): "*An abnormal current state in a circuit caused by the passage of a single energetic particle inducing a parasitic thyristor to turn on and remain in a fixed state regardless of inputs, until the device is power cycled. Some SEL events result in a measurable current increase (e.g., latch-up of an IO circuit). Some SEL events may result in a difficult to detect increase in current (micro-SEL) compared to the quiescent current of the entire component (e.g., latchup of memory cells within a common well). A high current SEL may cause permanent damage to the component and result in a hard error. Micro-SEL events are typically non-destructive due to the low current draw and can be cleared by power cycling.*"

As explained in the introduction, this paper does not aim to cover the vast and exhaustive domain of all types of SEEs, but mainly focuses on the most important issues concerning the modeling and simulation of SETs and SEUs induced by single events in digital electronics. For a detailed presentation of other SEEs and radiation effects in electronics (total-ionizing dose (TID), displacement damage) we invite the reader to consult ref. [13,26,27,28] and the references cited therein.

B. Main processes that lead to the production of an SEE in a circuit/system (summary)

Before surveying the main modeling and simulation approaches of SEEs in the next sections and going into the substance of several underlying mechanisms for creating SEEs, we summarize in the text that follows and in Fig. 2 the main processes that lead to the production of an SEE in a circuit. We note that the physical processes occur on different time scales and are non-interacting.

1) Interaction of the incoming particle with the target material

An SEE is always initiated by the interaction of an incident particle with the target material. This interaction necessarily involves a transfer of energy from the particle to the medium via electromagnetic or nuclear processes. As a result of such processes, a fraction or the totality of the incoming particle energy is released inside the medium [29]. At this level, we can identify two primary interaction mechanisms for the typical particles that could potentially cause SEEs in electronics: direct ionization and indirect ionization of matter [30].

Direct ionization typically concerns electrons, muons, low energy protons ($E < 1$ MeV), alpha particles and heavy ions (with atomic number $Z > 1$). These mainly interact with the electrons and nuclei of the target material [30]. In the initial phase of the passage of such a charged particle in matter, collisions with atomic electrons are the principal mode of energy loss in a very wide range of energies of the incident particle. These interactions gradually slow down the particle. In the final phase, the particle slowing and stopping are due to collisions with nuclei. The main mechanism that leads to energy loss and slowing down of the charged particle is then the ionization phenomenon. Ionization induces the generation of a large number of excited energetic electrons (delta-rays) which generally have sufficient energy to ionize other atoms. An electronic cascade is activated in which the number of free electrons continues to increase while their average energy decreases. During the passage of the ionizing particle, a highly ionized channel of very small diameter (typically a few tens of nm) develops around the track of the particle. Very rapidly, the excited electrons in the plasma lose their kinetic energy through a series of elastic collisions with electrons of the lattice to finally reach an energy close to the binding energy of the material. Simultaneously, the ionized atoms, positively

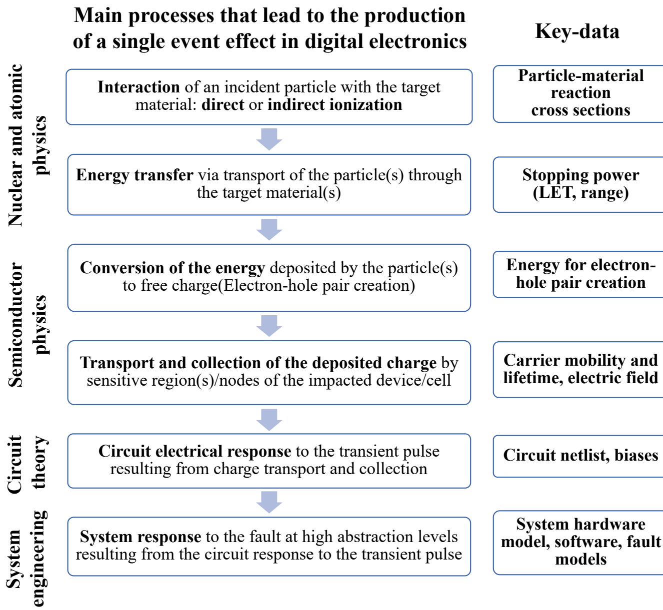


Fig. 2. Main processes that lead to the production of SEEs in digital electronics and key-data considered for their modeling and simulation, from the particle interaction to the system level.

charged, rearrange their electrons resulting in creation of holes in the valence band. A high-density column of electron-hole pairs is then formed in a narrow region around the particle track.

Indirect ionization primally concerns neutrons, but also high-energy protons and heavy ions. These particles can interact with atomic nuclei following two major mechanisms, i.e., scattering (elastic and inelastic interactions) and capture (inelastic interactions or nuclear reactions). For elastic interactions, the total kinetic energy is conserved, and the incoming particle is deflected from its path as it transfers some of its energy to the target atom. In the case of inelastic scattering, the target nucleus rearranges its internal state to one of higher energy, and the total kinetic energy is not conserved. But in both cases, the nature of the recoil nucleus is left unmodified. Instead of being scattered, an incident neutron, proton or ion may be absorbed or captured by a target material nucleus. After it has absorbed the impinging particle, the nucleus can get rid of excess protons or neutrons, it can undergo de-excitation by emitting a γ-ray, or it may even split into medium-sized fragments when the energies are high enough to trigger nuclear fission (a threshold energy exists for each such reaction). The produced fragments extend from proton or neutron to the nucleus of the target atom; they can in their turn directly ionize matter like any charged particle (previous case). It is important to note that nuclear reactions produced by high-energy ions are rare compared to ion-electron interactions, yet they hold significance in specific cases as explained in [31,32,33]. These nuclear reactions yield one or multiple secondary ionizing particles with significantly different electronic stopping power (see below) compared to the primary incident particle. The relevance of nuclear reactions in error rate estimations strongly depends on the critical charge of the circuit or device under consideration [31,32,33].

The number of nuclear interactions per type of interaction can be evaluated from cross section data of the atom nuclei present in the target material. For monoenergetic neutrons or protons arriving perpendicularly on a thin sheet of natural material, the number of nuclear interactions occurring in the target is given by

$$N_X(E) = \sum_i f_i \sigma_{X,i}(E) \times 10^{-24} \times NV \times t \times M \tag{1}$$

where X is the type of the considered interactions (elastic, inelastic, inelastic), E is the energy of the incident neutrons or protons, $\sigma_{X,i}(E)$ is the value at energy E of the type X reaction cross section for isotope i (expressed in barn), f_i is the fraction of isotope i in the target isotopic composition, t is the target thickness (expressed in cm), NV is the number of atoms per cubic centimeter and M is the number of incident monoenergetic neutrons or protons impacting the target.

2) Energy transfer from the ionizing particle(s) to the target material

For both direct or indirect ionization, two key-quantities can be introduced to characterize the energy transfer from an ionizing particle (i.e., an incident ionizing particle penetrating the target material or produced as a secondary particle in an interaction event involving a primary incoming particle and a target atom nucleus) to the target material: the stopping power and the range. We recall below the definitions of these two quantities.

Stopping power: The stopping power is the amount of energy per unit length lost by a particle in the matter. It is usually expressed in keV/µm or MeV/µm. The total stopping power is decomposed into two components: i) the electronic stopping power, corresponding to the loss of energy of the particle due to collisions with atomic electrons of the target material; ii) the nuclear stopping power, corresponding to the loss of energy of the particle due to collisions with the nuclei of atoms of the target material. The electronic stopping power is also called Linear Energy Transfer (LET). The LET thus characterizes the creation of electron-hole pairs by ionization of the target material, while nuclear stopping power describes the atomic displacement of the target material [30]. The LET is expressed as a function of the energy particle E as

$$LET = -\frac{\mathrm{d}E}{\mathrm{d}x} \tag{2}$$

For a nonrelativistic charged particle with speed v, charge z (in multiples of the electron charge) traveling into a target of electron density n and mean excitation potential I, the LET can be analytically evaluated from the reduced form of the Bethe-Bloch formula [34]

$$LET = \frac{4\pi n z^2}{m_e v^2} \cdot \left(\frac{e^2}{4\pi\epsilon_0}\right)^2 \cdot ln\left(\frac{2m_e v^2}{I}\right) \tag{3}$$

where ε_0 is the vacuum permittivity, e and m_e are the electron charge and rest mass respectively. Equation (3) shows that LET increases with decreasing particle velocity until it reaches a maximum value when the particle is close to stopping. A weighted LET is generally used, defined as the ratio between the LET and the density ρ of the target material

$$LET = -\frac{1}{\rho}\frac{\mathrm{d}E}{\mathrm{d}x} \quad (4)$$

The unit of this weighted LET is MeV/(mg/cm^2).

Range: The range R is the distance traveled by an ionizing particle of initial kinetic energy E_0 before it comes to rest in the stopping material; it is calculated from the LET of the particle as

$$R(E_0) = \int_{E_0}^{0} -\frac{1}{\frac{dE}{dx}}dE = \int_{0}^{E_0}\frac{1}{LET}dE \quad (5)$$

3) Conversion of the deposited energy to an electrical charge

The conversion of the energy deposited by an ionizing particle to free charge in a given target material can be evaluated from its mean value of energy for electron-hole pair creation $E_{e,h}$, a material-dependent constant usually experimentally measured or determined from band structure and quantum transport simulation (see for example recent work performed for bulk silicon and germanium [35]). When experimental or accurate simulated values are not available for a given semiconductor material, $E_{e,h}$ can be estimated from Klein's phenomenological model that establishes a linear relationship between the bandgap energy and $E_{e,h}$ in semiconductor materials [36]

$$E_{e,h}(eV) \simeq \frac{14}{5}E_g(eV) + 0.66 \quad (6)$$

The well-known value for bulk silicon is $E_{e,h}$ = 3.6 eV at 300 K. From (6), $E_{e,h}$ is expected to vary from ~1.1 eV for InSb (E_g = 0.17 eV at 300 K) to ~12 eV for diamond (E_g = 5.47 eV at 300 K).

For a given target semiconductor material characterized by its density ρ and its average energy for electron-hole pair creation $E_{e,h}$ and considering a particle with a given LET value, it is possible to calculate the charge Q_{dep} deposited by this particle along a path of length ℓ in the target material from the following expression

$$Q_{dep} = \frac{16.02 \times \rho}{E_{e,h}}\int_{path} LET(\ell)d\ell \quad (7)$$

In (7), Q_{dep} is given in fC if ρ is expressed in g/cm^3, $E_{e,h}$, is in eV, LET is in MeV/(mg/cm^2) and ℓ is in µm.

4) Transport and collection of the deposited charge in the region of the impacted circuit

Once a very dense column of electron-hole pairs has been created almost instantaneously (the practically instantaneous delivery of the ion energy to the electronic subsystem of a solid, lasting from 0.1 to 10^3 fs, creates a large number of electron-hole pairs per unit track length [37]) along the track of the ionizing particle, this deposited charge rapidly evolves under the action of different mechanisms that control the charge-carrier dynamics, e.g., its transport in the semiconductor material and its possible collection by a circuit node. It must be noted that these transport and collection processes of importance occur in the active semiconductor region of the device.

- Charge transport: the development of the column of electron-hole pairs starts in the femto-second range after its creation following three mechanisms that contribute to the reduction of the density of excess carriers at the heart of the track: ambipolar diffusion, carrier recombination (Shockley-Read-Hall and Auger recombination) and separation between holes and electrons under the combined effect of diffusion and drift induced by local electrical fields [37]. Charges released from this plasma column and having escaped the initial massive recombination, are quickly transported further into the semiconductor by diffusion and also by additional drift in regions where a non-zero electric field exists.
- Charge collection: released charges in the "vicinity" of a circuit node at front-end-of-line (FEOL) level, e.g., near or across a reverse-biased p-n junction or a biased diffused area contact, can be collected via drift-diffusion by such a structure and be extracted from the semiconductor material to the circuit. This charge collection process is crucial in the formation of a parasitic transient current that is injected on the impacted node. In section III we will look in detail at the physics, modeling, and simulation of this key-step in the formation of SEEs.

Fig. 3 illustrates the formation of a transient current pulse (shown in Fig 3(a)) resulting from the charge transport and collection in the case of a neutron-silicon nuclear reaction. This reaction occurs in the volume of the space charge region (SCR) of a reverse-biased nano-transistor drain junction and produces four ionizing secondaries. The figure is the result of a simplified particle Monte Carlo simulation in which the radiation-induced minority carriers (here the electrons grouped per packets of multiple charges) are represented by red points. After the production of secondaries and the energy deposition along their tracks (Fig. 3(b)), the widening of the charge clouds reflects the diffusion of the carriers, their displacement towards the top surface, and their drift in the electrical field (here vertical) of the junction (Figs. 3(c), (d), (e)). Carriers are finally extracted from the top surface (electrode) where they contribute to the formation of the transient current that is injected into the external circuit.

5) Circuit electrical response

The current transient pulse resulting from the radiation-induced charge collection and extraction at the level of a circuit node may induce disturbances in the circuit to which the impacted node is connected. The induced effects at circuit level are different according to the intensity of the current transient, as well as the number of impacted circuit nodes. If the transient peak is sufficiently important in terms of current magnitude, it can induce a hard error (permanent damage) on gate insulators (gate rupture, SEGR) or provoke a short-circuit loop between different semiconductor regions (latchup, burnout). In other cases, the transient current may generally induce a soft error which can be manifested by the change of logic state of one or

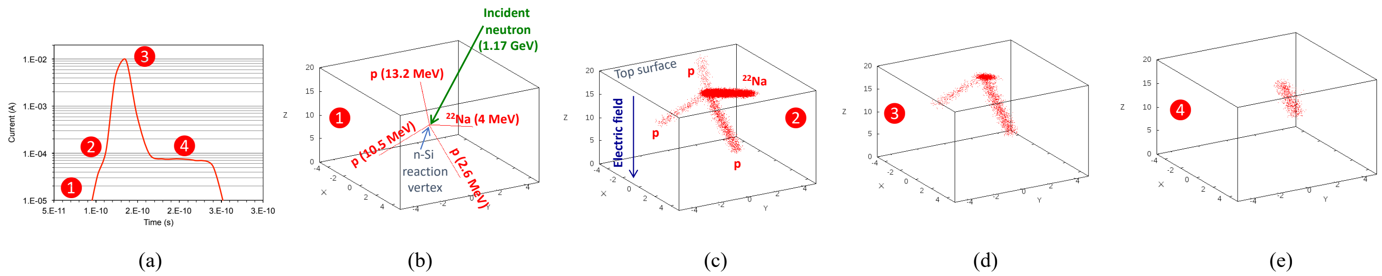


Fig. 3. Particle random-walk drift-diffusion (RWDD) numerical simulation (described in section IV.C) of the transient current (a) extracted from the junction contact (corresponding to the top surface) in a reverse-biased junction caused by the interaction of a 1.17 GeV neutron with a silicon atom (3 protons and a ^{22}Na ion produced). Illustration of the charge generation (b) and the transport and collection phases 2 (c), 3 (d) and 4 (e) indicated on the transient plot. Dimensions on the three axes are in nanometers.

more memory points (upset) or even a functional interrupt. In the following sections, we will examine in detail the circuit electrical response to such radiation-induced pulses, and we will show that the circuit is not necessary passive during this phase of charge collection. On the contrary, it can play an important role via the counter-reaction it develops on the impacted node potential following the collection of charges on it.

6) System response

When a transient event occurs at the level of a circuit, hardware component of a larger electronic system, it can trigger various consequences that reverberate at the system level. One prominent consequence is data corruption. In digital systems, the sudden change in the state of a register or memory bit due to an SEU for example can lead to errors in calculations, memory storage or communication protocols. This corruption compromises the integrity of critical information and can have cascading effects on subsequent operations. In addition to data corruption, the functionality of the affected circuit may be disrupted. This disruption may be transient, causing temporary malfunctions, or it may cause permanent changes in the logic of the circuit, resulting in unexpected behavior, system crashes or erroneous responses. In some cases, a single event can even trigger a system reset, resulting in temporary downtime, potential loss of data and disruption to overall system operation. Single events can also cause communication errors. Corruption of data as it is transmitted between different components of the system can lead to misinterpretation, protocol violations or communication failures. Such errors can undermine the synchronization of subsystems, essential for the proper functioning of complex systems. SEEs at the system level can similarly alter the control flow within software. An event-induced change in the logic of a program can lead to unintended branches or loops that were not intended by the original design. Consequently, the system might exhibit behavior that deviates from the expected and intended operational path, potentially causing software crashes or erroneous outcomes. There is also the risk of permanent damage caused by single events. In extreme cases, the circuit can be irreparably harmed, rendering the system inoperable. Finally, SEEs might not always lead to immediate visible effects. Some events could introduce latent effects that manifest themselves later, making the diagnosis of system-level issues challenging.

C. Multi-physics, multi-scale and multi-domain nature of single events

The previous subsections summarized the different processes that lead to the production of an SEE in a digital circuit or a system. It showed that single-event effects are inherently multi-physics, multi-scale and multi-domain, as indicated in the following and illustrated in Figs. 4 and 5.

- Multi-physics: SEEs are first initiated by particle-matter interactions, fields of nuclear and atomic physics. Then, they involve the creation of charges and their transport in materials, mainly semiconductors, governed by solid-state physics and quantum-mechanics. The resulting transient current or voltage pulse created in the interconnected network of elementary structures that constitute the circuit itself, in the sense of the electronics function, obeys the fundamental laws of electrokinetics and circuit theory. Finally, the potentially disturbed circuit response can affect the system of which it is a part, governed by the general theory of systems.
- Multi-scale: SEEs are initiated by a single particle interaction at atomic-level in the bulk of circuit materials and can lead to a functional error at circuit or system-level. Between these two events, there are approximately 15 orders of magnitudes on the distance scale and approximately 20 orders of magnitude on the time scale, as illustrated in Fig. 4. In addition to the multi-physics nature of SEEs, these changes of scale both in time and in distance explain why is extremely difficult to simulate SEEs with a single tool from the beginning to the end of this sequence of events.
- Multi-domain: SEE, or more accurately the precursor event to an SEE, is first an atomic event before being transformed into an electrical signal then into an analog or logical event. Depending on when it is considered, it therefore belongs to different fields or domains: the domain of materials, then of devices, then of circuits and finally of systems. To each domain corresponds a particular expression of this SEE precursor: secondary particles of a nuclear interaction, bundle of electron-hole pairs, transient current, analog signal, logic pulse, value encoded in a memory, etc. When passing from one domain to the next, as defined in the SEE chronology formulation, the physics of the previous domain appears to be lost in

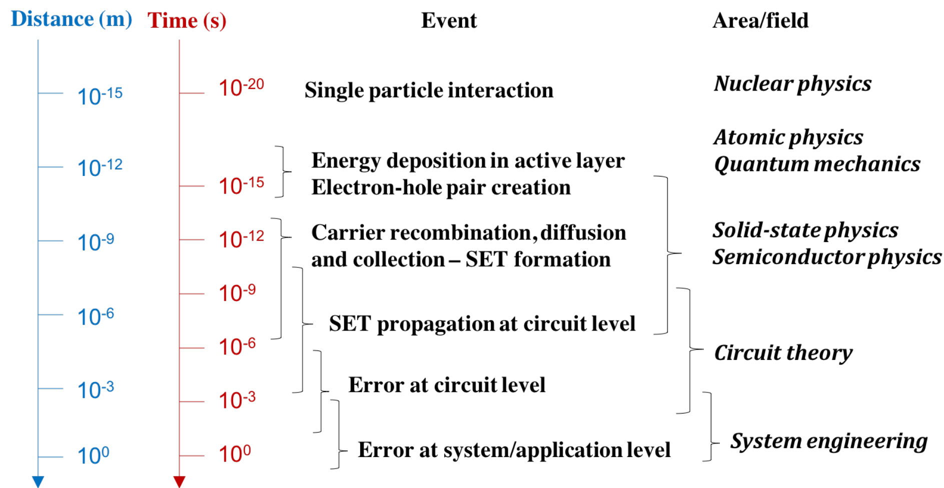


Fig. 4. Typical space and time scales for single events effects, from the single particle interaction to the detection of an error at system level.

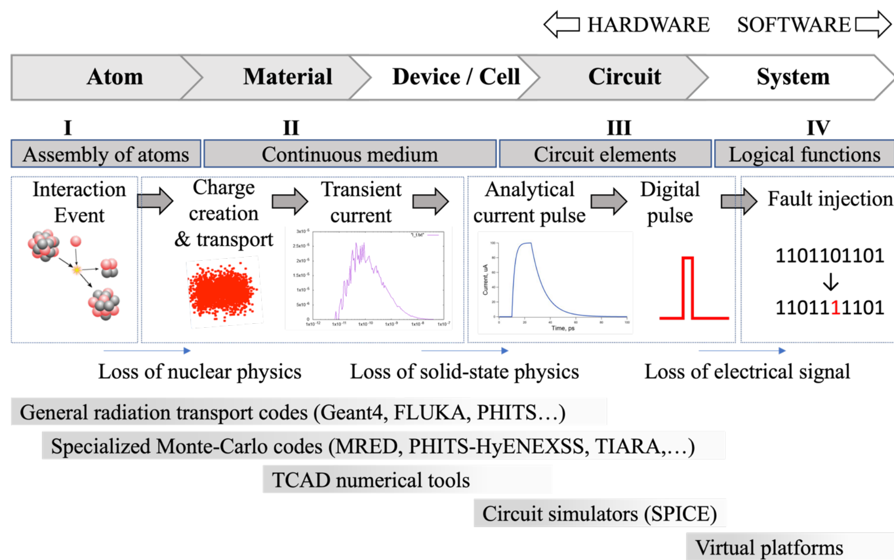


Fig. 5. The multi-physics, multi-scale, and multi-domain nature of SEE. The main simulation tools and platforms are also indicated.

the new domain; this can be overcome to a certain extent, as will be discussed in several places later in this paper. For example, when the secondary particle energy is converted into e-h pairs, the nuclear physics is no longer appropriate for describing the formation of the SEE and any information relating to the nuclear event is moreover lost. This vision is true until the final expression of the SEE at the system or application level, at the end of the chain.

Fig. 5 illustrates in a slightly different way the multi-physics and multi-scale nature of SEE, emphasizing their multi-domain character. Four domains can be defined in which an SEE precursor (or initial event) will have different expressions: at the atomic level (assembly of atoms), at the material level (continuous media), at the circuit level (circuit elements) and at the system level (logical functions). The boundary is sometimes difficult to define, hence the notion of assembly of atoms to describe the domain in which nuclear interactions and energy deposition of secondary particles by ionization take place. The same applies to the notion of continuous medium to describe semiconductor or insulating materials, whether they are considered as bulk materials or part of a component.

When considering the chronological formulation of SEEs (from atoms to systems), each change of domain is marked by a loss of information concerning the mechanism that gave rise to the precursor signal of the SEE. The precursor of an SEE is first a nuclear interaction, then a cloud of charges, then an analog electrical signal, then a digital signal and finally a binary value. Considering the electrical signature of an SEE no longer allows us to go back to the interaction that gave rise to it; likewise, considering a binary change does not make it possible to go back to the original electrical signal. This loss of information concerning the physical mechanisms from the underlying domain to the next is an important element in understanding that an SEE can be simulated at different levels and with different physical manifestations. This point will be discussed in detail in III.A. In certain cases, results from a tool that simulates a level farther along in the chronological formulation of an SEE can be used to define inputs to a tool that appears earlier in the chronological view. While at first this seems counter intuitive, the rationale is in fact simple: if the

outputs from a higher-level tool can be simplified such that they can be used to define inputs to a lower-level tool, then one gives up information from the high-level tool. This approach allows one to by-pass higher-level tools in the full analysis of an SEE, reducing simulation time significantly. This point is briefly described in Sections I.V.A and V.D.

III. TAXONOMY OF MODELING AND SIMULATION APPROACHES

In this section, we examine the different types of methodologies of modeling and simulation of SEEs, as a function of the "simulation level" envisaged to perform a given study. We propose a classification of simulation tools in five main categories. We also examine the main modeling and simulation approaches for the transport and collection of the deposited charge induced by an ionizing radiation at device or circuit levels that allow us to distinguish methods using a collection charge concept with respect to methods considering the computation of a collected current.

A. Types of methodologies: what simulation code, input, and output?

We start again from Fig. 5 which illustrates the domains covered by the main simulation tools and platforms used to simulate SEE in electronics (the list is far from exhaustive). This highlights that none of them can cover the entire chain, from particles to systems. We distinguish five categories of codes, briefly described in the following and in Table I:

(1) General radiation transport codes like Geant4 [38,39], FLUKA [40,41], MCNP [42,43] or PHITS [44,45]: these codes are general-purpose, continuous-energy, generalized-geometry, time-dependent and Monte Carlo radiation transport codes designed to track many particle types over broad ranges of energies. These codes have many applications in high energy experimental physics and engineering, shielding, detector and telescope design, cosmic ray studies, dosimetry, medical physics, and radiobiology. In the context of SEE studies, these codes can be used to develop and compile complete applications from toolkits including source files and libraries. Alternatively, they can be used to perform various calculations from precompiled versions that read data input files.

(2) Specialized Monte Carlo radiation transport codes applied to SEEs like SEMM/SEMM-2 [46,47,48], MRED [31,49,50,51], PHITS-HyENEXSS [52], TIARA [53,54,55], MUSCA-SEP3 [56,57], IRT [58], MC-ORACLE [59,60] and other codes (see references in [51]) based on nuclear and radiation transport physics : these Monte Carlo-based radiation transport tools are able to simulate a variety of effects that result from energy transferred to a semiconductor material by a single particle event. The breadth and depth of the application of each specialized code solving single event effects problems varies dramatically, from almost non-existent to a high level of detail, as illustrated in [51].

(3) TCAD numerical simulation platforms like the Synopsys® [61], Silvaco® [62] or Cogenda® [63] suites: TCAD code suites are used to model and numerically simulate semiconductor fabrication and semiconductor device operation. Included are the modeling of process steps (such as diffusion and ion implantation), and modeling of the behavior of the electrical devices based on fundamental semiconductor physics and numerical solving of electrostatics and continuity equations for different carrier transport models (drift-diffusion, hydrodynamics, quantum transport,…), also taking into consideration radiation effects and transport (see section IV.D). Coupled with a circuit simulator, TCAD tools are also able to simulate the impact of radiation at circuit-level in mixed-mode approach (see section V).

(4) Circuit simulators: they include analog simulators, digital simulators, and dedicated codes for mixed-signal analog/digital circuits. The most popular is SPICE (Simulator Program with Integrated Circuit Emphasis) which is certainly the most used electronics circuit simulator. SPICE refers to a wide variety of open-source (Ngspice [64]) and commercial circuit simulation programs (PSpice® [65], Eldo® [66]) offering extended capabilities via the integration of optional analog, radiofrequency (RF), mixed-signals or digital circuit simulation modules. Analog circuits embedding digital content can thus be simulated. More generally speaking, SPICE also refers to a class of simulation approaches based on the conversion of a text netlist of electrical elements such as resistors, capacitors, diodes, transistors and voltage/current sources and their connections to equations to be numerically solved. At this circuit level, SEEs can be modeled under the form of current or voltage pulses produced by a parametrized or arbitrary source inserted in the netlist and emulating the impact of a ionizing particle on a particular circuit node.

(5) System simulators and virtual platforms: at complex digital circuit, system-on-chip or system levels, the modeling and simulation of SEEs profoundly change in nature. SEE signals become logical (binary) information and are introduced during a simulation run via fault injection (FI) techniques. Their impact can be explored at different abstraction levels (gate-level, cycle-level, transaction-level) using a wide variety of dedicated tools [67]. Full-system simulators or virtual platforms, such as OVPsim [68] or gem5 [69], are used to explore the vulnerability of complete systems to SEEs: they must include not only the modeling of the full hardware system (i.e., processor, memory, peripherichals,…) but also the modeling of the full software system (the user application and the full operating system). The soft error vulnerability of a complete system can be analyzed from the exhaustive characterization of the execution errors monitored during a simulation.

Table I summarizes the simulation level, typical simulation inputs and outputs for the different categories of codes defined in Fig. 5 and in the text above. We will examine in the following sections some specificities of these different simulation approaches, firstly focusing on the physics of the charge transport and collection at semiconductor level, an essential step for the creation of transient signals which are at the origin of SEEs at device and circuit levels.

TABLE I
SIMULATION LEVEL, TYPICAL SIMULATION INPUTS AND OUTPUTS FOR THE FIVE CATEGORIES OF CODES INTRODUCED IN FIG. 5 AND IN THE TEXT.

Type of codes	Simulation level	Typical simulation inputs	Radiation input (or signal emulating radiation)	Typical simulation outputs
General radiation transport codes	Atom to small circuit	Simplified three-dimensional (3D) circuit architecture Sensitive volumes	Primary particles Sources of particles (or nuclear interaction databases)	Secondaries Energy deposited in sensitive volumes
Specialized Monte Carlo code as applied to SEEs				Secondaries Energy in sensitive volumes and/or collected charge Soft error rate
TCAD	Material to cell	Realistic device/circuit 3D architectures (possible link with process)	Radiation-induced generation rate	Device transient response Carrier and potential distributions
Cell circuit simulation codes	Material to cell	Transistor compact model	Numerical or analytical SETs	Cell transient response (time domain analysis)
Circuit simulators	Device to circuit	Circuit netlist Device library	Analytical SETs Logical SETs	Soft error rate
Hardware Description Language (HDL) simulators and virtual platforms	Circuit to system	Circuit design Application code	Logical faults	Soft error vulnerability Execution errors

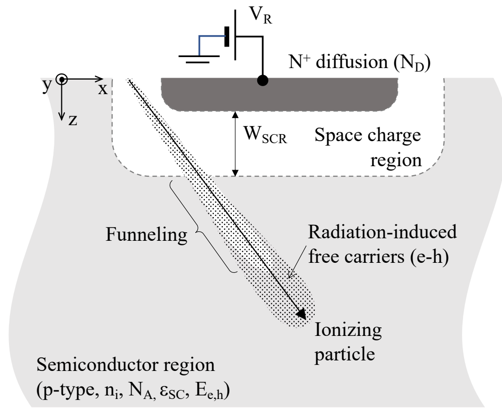


Fig. 6. Schematic illustration of the passage of an ionizing particle crossing the space charge region (SCR) of a reverse-biased p-n junction and stopping in the semiconductor region.

B. Physics of the charge transport and collection (collected charge and current)

One of the most complex and central tasks in modeling and simulation of SEE is to correctly describe the interaction of an incoming particle with the sensitive zone(s) of a circuit and to determine the resulting transient electrical response susceptible to subsequently induce an SEE at circuit level. We examine in this paragraph the underlying physics that controls the charge transport and collection at the level of an elementary device, a reverse-biased n^+-p junction integrated on bulk semiconductor material (silicon by default). We take as a starting point (t_0) the moment immediately after the passage of the particle when the radiation-induced charge is just deposited in the form of a dense track of electron-hole pairs, as schematically illustrated in Fig. 6. The device of interest is defined by its geometry, type of materials, doping concentrations, and so on. Carrier transport and potential dynamics induced by the passage of the particle in the semiconductor domain can be resolved in time from the self-consistent solving (coupling) of a set of three fundamental equations:

1) the Poisson equation that addresses the electrostatic problem. Solving this equation amounts to finding the electric potential ϕ (V) for a given charge density distribution ρ (C.m^{-3})

$$\nabla \left(\epsilon \overrightarrow{\nabla \phi}\right) = -\rho = -q\left[N_D^+ - N_A^- + p - n\right] \tag{8}$$

where ε is the material-dependent permittivity (F.m^{-1}), q is the absolute value of the electron charge, N_D^+ and N_A^- are the doping ionized atom concentrations (m^{-3}) for donor and acceptor impurities, respectively, n and p are the electron and hole densities (m^{-3}), respectively.

2) the continuity equations that guarantee the continuity of electron and hole current densities J_n and J_p (A.m^{-2}), respectively

$$\nabla \vec{J}_n = q(G-R) + q\frac{\partial n}{\partial t} \tag{9}$$

$$\nabla \vec{J}_p = -q(G-R) - q\frac{\partial p}{\partial t} \tag{10}$$

where G and R are the generation and recombination rates, respectively.

The electron and hole densities are calculated using the Fermi-Dirac statistics or using the Maxwell-Boltzmann approximation in case of non-degenerate doped semiconductors. In addition, to solve (9) and (10), a transport model must be chosen to express the current densities J_n and J_p. In the following, the classical drift-diffusion (DD) model will be used as the transport model. This assumes that the carrier energy is constantly in balance with the electric field, so that the transport only depends on the electric field. In the DD model,

the carrier transport is mainly due to electrostatic potential gradients and/or to carrier concentration gradients. The current densities of electrons and holes are then usually modeled as follows

$$\vec{J}_n = -q\mu_n n\vec{\nabla}\phi + qD_n\vec{\nabla}n \quad (11)$$

$$\vec{J}_p = q\mu_p p\vec{\nabla}\phi - qD_p\vec{\nabla}p \quad (12)$$

where μ_n (μ_p) is the electron mobility (respectively holes), D_n (D_p) is the thermal diffusion coefficient of electrons (respectively of holes), and ϕ is the electric potential, solution of (8). $D_{n,p}$ and $\mu_{n,p}$ depend on the material and electric field and are connected by the Einstein relation $D_{n,p} = (kT_L/q)\times \mu_{n,p}$ where T_L is the lattice temperature. In (11) and (12), current densities are therefore given by the sum of the conduction or drift component (the first term of the right side of equations) and the diffusion component (the second term).

In (8)-(12), the quantities n and p include not only the free carrier concentrations at equilibrium given by the band bending of the semiconductor, but also the excess carrier densities produced during the passage of the ionizing particle in the device. In other words, these radiation-induced electrons and holes are in excess with respect to the charge carriers available at thermal equilibrium. It is evident that the presence (along the particle track at t_0) and the evolution (due to diffusion, recombination, and drift in the space charge region (SCR)) of excess carriers locally modify the electrostatic potential and thus complexifies the carrier dynamics and the transient device response.

One of the most important electrostatic manifestations of excess carriers is the drastic distortion of the electric field in the border of the SCR when the particle passes through this area, known as the funnel effect. After the particle penetration, the electric field, which was originally limited to the SCR, extends far down into the bulk semiconductor along the length of the particle track and can literally "funnel" many carriers into the struck junction, further enhancing charge collection. After a few nanoseconds, the field recovers to its position in the normal depletion layer, and, if the track is long enough, a residue of carriers is left to be transported by diffusion. The extent of this funneling is a function of substrate doping concentration, bias voltage, and the particle energy. It is a clear manifestation of the self-consistent character of the problem posed by the solving of the Poisson and continuity equations in the presence of an ionizing particle penetration.

Solving self-consistently the set of equations (8)-(12) in the three spatial dimensions and in a time domain including the passage of the ionizing particle up to the return to equilibrium is thus a very complicated process that only becomes tractable when using full numerical simulation performed on a meshed structure in which each node has specific associated properties, such as type of material, doping concentration, electrostatic potential, quasi-Fermi levels, etc. This meshing is used for solving discretized forms of (8)-(12) with given boundary conditions. In practice, only TCAD tools or some dedicated codes are capable of performing such fully numerical calculations (see section IV).

To render this problem easier to solve in the context of SEE prediction at circuit level, many simplifying assumptions must be introduced. These simplifications relate to the two aspects of the problem: the electrostatics and the transport of charges.

- The first is to decouple the Poisson equation from the continuity equations. In other words, the electrostatic potential at equilibrium (before the particle struck) is conserved throughout. The continuity equations are then solved considering an electric field fixed at the equilibrium of the structure, i.e., equal to zero in the semiconductor bulk and given by the p-n junction theory inside the space charge region of the collecting junction. Consequently, electron and hole density currents are pure diffusion currents throughout the simulation domain, to which a drift component must be added only inside the SCR. Two time-dependent models can be derived from this simplified schema: the diffusion-collection model and the drift-diffusion collection model, detailed in sections IV.B and IV.C. These approaches allow a collected current to be computed, catch the dynamics of the event, and facilitate the consideration of the counter reaction of the circuit in the case of mixed-mode simulation (section V).
- In addition to the previous simplification, the way in which the sensitive node collects the minority carriers resulting from the radiation can be greatly simplified by considering that only the carriers generated in a certain so-called sensitive volume around the node will surely be collected. Here, diffusion and drift of excess carriers occur in an "invisible way", their action and efficiency are included in the geometrical parameters of the sensitive volume. The computation of the charge transport is no longer meaningful, and the time variable disappears from the calculation that reduces to a pure geometrical problem. Different models can be derived from this approach, they are described in section IV.A.

These simplifying assumptions lead to less accurate simulation results, but simplified implementation and faster simulation times. Depending on the level of simplification considered, the computation effort and accuracy will be obviously very different. From the considerations highlighted above, Fig. 7 proposes a classification of the main modeling-simulation approaches for the transport and collection of the deposited charge by an ionizing radiation at semiconductor device level, detailed in the following.

IV. Analytical, Compact, and Full Numerical Methods at Device/Cell Level

In this section, we examine in detail the main modeling and simulation approaches developed in the last decades by several research groups and authors concerning SEE at device and circuit cell levels. They include some popular sensitive volume-based models, the so-called diffusion-collection method, the random-walk drift diffusion approach and TCAD simulation.

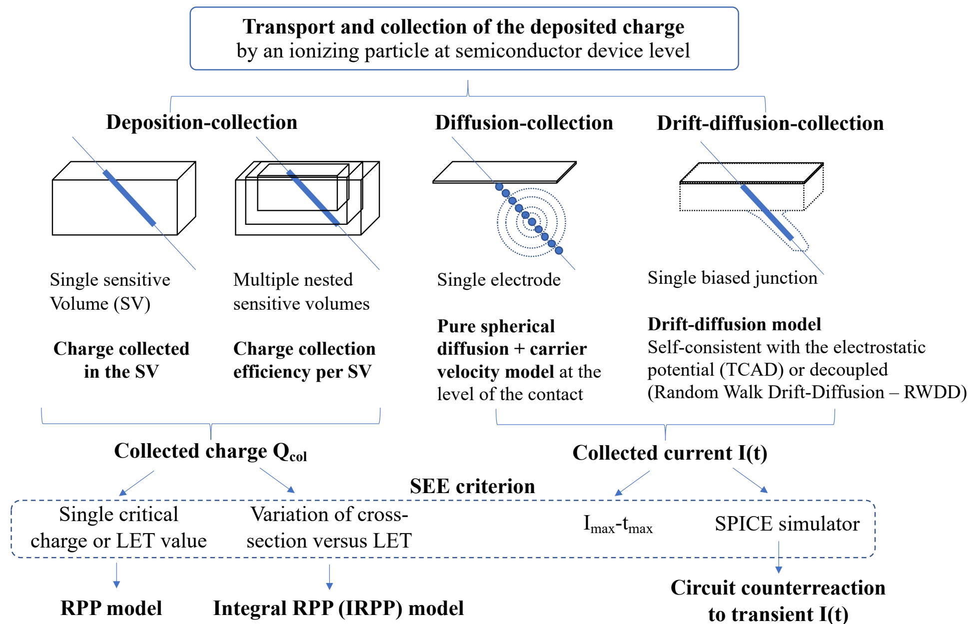


Fig. 7. Classification of the main modeling-simulation approaches for the transport and collection of the deposited charge induced by an ionizing radiation at semiconductor device level.

A. Sensitive volume-based models

RPP model: A sensitive volume (SV) is defined as "*a region in space in which energy deposition from ionizing particle can affect the operation of a device. For SEE, the volume is often associated with the depletion region of a particular circuit node*" [70]. This SV, also called "charge collection volume", is generally treated as a rectangular parallelepiped (RPP). The charge deposited by a given ionizing particle depends on its path in the SV. It can be evaluated from (7) where ℓ is the length of the particle path in the SV, as illustrated in Fig. 8(a). An RPP volume is defined by a triplet of reals (a, b, c) where a, b, and c represent the three dimensions of the parallelepiped in decreasing order. For such an RPP volume, the chord maximum length ℓ_{max} corresponds to the main diagonal, i.e., $\ell_{max}^2 = a^2 + b^2 + c^2$, and the total surface area of the volume is $S = 2(ab + ac + bc)$ (Fig. 8(a)).

Sensitive volume approaches are based on the essential notion of circuit critical charge Q_{crit}, originally defined for memory circuits as "*the minimum amount of collected charge that will cause a device node to change state and result in a single event upset*" [24]. In this definition, the critical charge is supposed to be independent of the current pulse shape, which supposes that the current pulse produced by the ionizing particle is short compared to the integration time constant of the circuit (including parasitic capacitances) [71].

The determination of the critical charge value can be evaluated from various mixed-mode, TCAD or circuit simulation approaches, described later in the paper. At this point, it is important to remember the remark that concluded section II.C. This remark emphasizes that the outputs from a higher-level of simulation (i.e., a circuit simulation) can be simplified (i.e., reduced to a single critical charge value) such that they can be used to define inputs to a lower-level approach (i.e., the RPP model), hence by-passing higher-level tools in the full analysis of the SEE problem and, in final, reducing simulation time significantly.

Supposing that the SV of Fig. 8(a) is attached to a sensitive node of a given circuit cell characterized by a critical charge value Q_{crit}, in a first approximation (discussed and completed later), if the charge generated by the incident ionizing particle in the SV is greater or equal to Q_{crit}, then the circuit will be disturbed, and an SEE will be produced. This condition can be written as follows

$$Q_{dep} = K \times LET \times \ell > Q_{crit} \quad (13)$$

where K is a material-dependent constant derived from (7) that depends on ρ, the density of the material and on $E_{e,h}$, the energy for electron-hole pair creation, and ℓ is the length of the particle path inside the SV.

The primary interest of SV-based models is that it is possible to combine certain characteristics of the particle source with the calculation of the deposited charge and therefore, by comparison with a critical charge, to calculate directly the SEE error rate for a given radiation environment. In this sense, these models are particularly well-adapted for on-orbit environments characterized by an isotropic flux of heavy-ions. To be numerically tractable, a certain number of simplifying assumptions must be considered. These assumptions have been carefully reviewed and discussed by Petersen in [71]. We recall in the following the most important (all are taken from [71]):

- *"The energy deposited in a sensitive volume is equal to the energy loss of an energetic ion passing through that volume as calculated using its LET."*
- *"Ions with the same LET have the same effect."*
- *"The change in LET along an ion track in the region of interest is negligible."*
- *"The charge generation is equal to the product of the LET of the ion and a chord of the region (as state by (13)),*

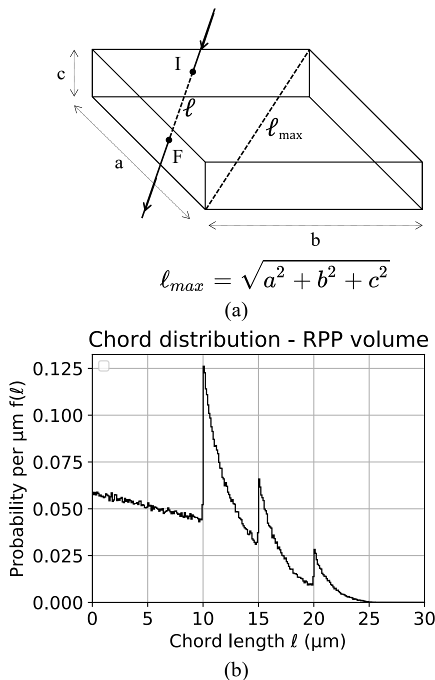


Fig. 8. (a) Definition of an RPP volume of dimensions a × b × c, and (b) chord distribution numerically calculated from Monte Carlo simulation for an RPP volume with a = 20 µm, b = 15 µm and c = 10 µm (histogram on 570,612 chords).

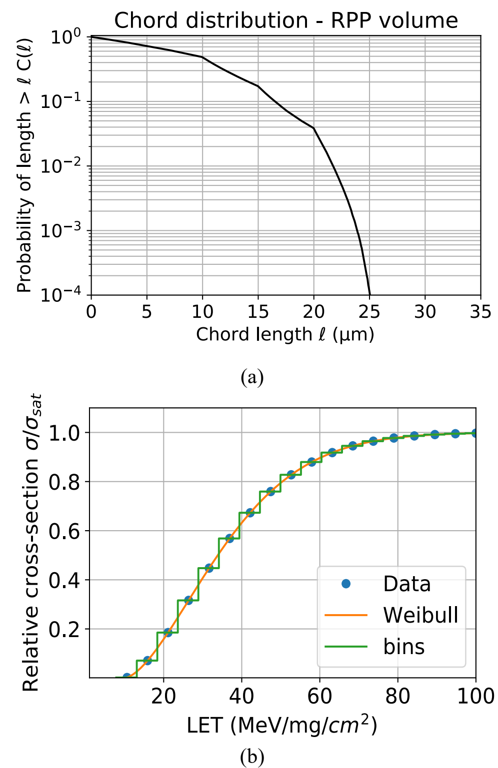


Fig. 9. (a) Integral chord length distribution corresponding to the integration of histogram of Fig. 8(b) using (15), and (b) Typical relative cross section data versus LET. The fitting of data with integral Weibull distribution is also plotted. The introduction of bins on the cross-section curve is needed for IRPP calculations.

perhaps augmented by a funnel region or a diffusion region."

- *"The charge collection path is independent of the LET."*
- *"The sensitive volume is a convex body. The charge collected from an ion track is that generated along the chord defined by the path through the sensitive volume."*
- *"The particle flux is isotropic at the device and therefore the LET spectrum is the same for all directions"*.

The charge deposited in the SV is given by the integral of the product of the chord length distribution f(ℓ) of the RPP box by the LET distribution of the incoming particles [71]. Fig. 8(b) shows such a chord length distribution for an RPP volume in the form of a probability histogram. This histogram is upper bounded by the maximum chord length value, i.e., $\ell=\ell_{max}$.

To directly derivate the SEE error rate from (13), one must evaluate for a given particle LET value Λ, the minimum chord length ℓ_{min} of the particle through the sensitive volume that will create enough electron-hole pairs to cause an upset. From (13), it is evident that $\ell_{min} = Q_{crit}/(K\times \Lambda)$; its *minimum minimorum* value is $\ell_{min} = Q_{crit}/(K\times \Lambda_{max})$ where Λ_{max} corresponds to the maximum value of the LET spectrum related to the particle source. The number of events is then directly determined by the sum of possible paths that can lead to an adequate charge deposition in the SV. Pickel's formulation [71] uses the combination of the ionizing integral particle flux in terms of its energy deposition Φ(Λ) and the path probability f(ℓ)

$$N = \frac{S}{4}\int_{\ell_{min}}^{\ell_{max}} \Phi(\Lambda_{min}) f(\ell) d\ell \tag{14}$$

where S is the total area surface of the volume, ℓ_{max} is the maximum path length in the RPP volume, Λ_{min} is the minimum LET that can deposit critical charge in path length ℓ. From (13), the quantity to be used in (14) is $\Lambda_{min} = Q_{crit}/(K\times\ell)$. Note that Φ(Λ) is derived from the distribution in energy Φ(E) using the transformation Φ(Λ) = Φ(E) × (dE/dΛ). The particle flux Φ is supposed isotropic and is integrated over 4π steradians.

For the convenience of calculation (availability of analytical approximations), the integral chord length distribution C(ℓ) may be preferred to f(ℓ). C(ℓ) corresponds to the probability of a particle traversing the sensitive volume with a chord length greater than ℓ (see Fig. 9(a)), i.e.,

$$C(\ell) = \int_{\ell}^{\ell_{max}} f(\ell')d\ell' \tag{15}$$

Equation (14) can be rewritten following the basic form of Bradford's formulation [71,72]

$$N = \frac{N}{4}\int_{\Lambda_0}^{\Lambda_{max}} \Phi(\Lambda) \times C\left(\frac{Q_{crit}}{K\Lambda}\right) d\Lambda \tag{16}$$

where Λ_0 and Λ_{max} are, respectively, the minimum minimorum and the maximum value of the LET spectrum related to the particle source, and from (13), $\Lambda_0 = Q_{crit}/(K\times \ell_{max})$.

Integral RPP (IRPP) model: In the RPP method described above (formulations of Pickel and Bradford), there is a unique critical charge that must be exceeded for the circuit cell to upset. Consequently, the curve of cross section versus LET, for a circuit modeled as a collection of identical cells with the same

SV parameters and a unique Q_{crit} value, will be necessarily a step function. Such a cross-section curve, expected if all parts of all cells had the same sensitivity, does not correspond to what is generally observed. Petersen discussed in detail in [71] (and references therein) the inadequacy of the single Q_{crit} (or LET threshold) for upset rate calculations and the necessity of integrating the LET spectrum with the cross-sections curves to properly allow for changes of sensitivity across the circuit. This more general model is called the integral RPP approach.

The IRPP model allows for the variation of the internal circuit sensitivity by integrating over a distribution of event rates corresponding to the variation of the circuit cross section versus LET $\sigma(\Lambda)$. This curve is supposed to be experimentally known. The process consists in interpreting the $\sigma(\Lambda)/\sigma_{sat}$ relative cross-section curve (σ_{sat} is the saturation cross section) in terms of a distribution of critical charges, assuming a single RPP sensitive volume with thickness c. The conversion from Λ to Q_{crit} is obtained at any part of the curve via the relationship: $c = Q_{crit}/(K\times\Lambda)$. From the experimental data (see Fig. 9(b)) and for each discrete value of Q_{crit} describing the curve, the number of events is calculated by integrating the RPP chord distribution with the LET spectrum of the environment, in the same way as in (14). The result is weighted with the quantity $(\sigma(\Lambda)/\sigma_{sat})\times$bin width for the bin corresponding to the considered discrete Q_{crit} value (Fig. 9(b)). The circuit response corresponds to the sum of these individual contributions over the entire curve [71]. In mathematical terms with continuous variables and functions, if we set $\sigma(\Lambda)/\sigma_{sat} = F(\Lambda)$, the number of events can be expressed as

$$N = \frac{N}{4}\int F(\Lambda')\int_{\Lambda_{min}}^{\Lambda_{max}} \Phi(\Lambda)\times C\left(\frac{\Lambda' c}{\Lambda}\right) d\Lambda d\Lambda' \quad (17)$$

where Λ_{min} is the minimum LET value to deposit $Q_{crit} = K\times\Lambda'\times c$ on the main diagonal of the RPP volume, ℓ_{max}, that gives $K\times\Lambda_{min}\times\ell_{max} = K\times\Lambda'\times c$, then $\Lambda_{min} = \Lambda'\times c/\ell_{max}$.

Different distribution functions can be used to model the $\sigma(\Lambda)/\sigma_{sat}$ relative cross-section curve [71]. The most popular function is the integral Weibull distribution

$$\frac{\sigma(\Lambda)}{\sigma_{sat}} = F(\Lambda) = 1 - exp\left\{-\left[\frac{(\Lambda-\Lambda_0)}{W}\right]^s\right\} \quad \Lambda \geq \Lambda_0 \\ = 0 \quad \Lambda < \Lambda_0 \quad (18)$$

where Λ is the LET, Λ_0 is the LET threshold, W is the width parameter and s is the shape parameter. Fig. 9(b) illustrates the plot of (18) with the following parameters: Λ_0 = 10 MeV/(mg/cm^2), W = 30 MeV/(mg/cm^2), s = 1.6.

<u>Introduction of funneling in RPP/IRPP models</u>: The charge-collection effect attributed to funneling, illustrated in Fig. 6, can be included in RPP/IRPP models following two different approaches summarized here.

- The first method consists in increasing the depth of the sensitive volume to include the funnel contribution. The chord lengths will be then augmented, notably in the z direction, from a funnel length ℓ_f.
- The second method is to add the funnel path to the charge-collection path, but not to change the basic RPP volume. As noted by Petersen [71], most of simulation codes allow a separation of an intrinsic sensitive volume and an additional path length ℓ_f attributed to the funnel. In this case, the charge deposited in the SV must be rewritten

$$Q_{dep} = K \times LET \times (\ell + \ell_f) \quad (19)$$

Consequently, the different expressions for ℓ_{min}, ℓ_{max}, Λ_{min} and Λ_{max} previously defined for (14), (16) and (17) must be reevaluated from (19).

A series of funneling model descriptions conducted by Messenger and Ash can be found in [72]. Different analytical expressions of the funnel lengths can be derived from the approximate solution of the continuity equations and the electroneutrality equation. The model developed by Hu [73] proposes simple expressions for the depth of collection d_f and length of collection ℓ_f related to the funneling in a n$^+$p junction subjected to an ion strike, as defined in Fig. 10(a)

$$\ell_f = \left(1+\frac{\mu_n}{\mu_p}\right)\frac{W_{SCR}}{cos(\theta)} \quad (20)$$

$$d_f = \left(1+\frac{\mu_n}{\mu_p}\right)W_{SCR} \quad (21)$$

where W_{SCR} is the width of the space charge region, θ is the incident angle of the ionizing particle, μ_n and μ_p are the electron and hole mobilities in the substrate material, respectively.

For the first method and as illustrated in Fig. 10(a), the depth of the sensitive volume has to be increased by the quantity d_f given by (21) to include the funneling. It should be noted that in this case the angular dependence of the funnel contribution is not explicit, since it is already integrated with the chord length distribution functions obtained with this RPP volume (with increased depth).

<u>Weighted sensitive volume model</u>: This method was introduced to improve the traditional RPP approach that fails to account for different charge collection mechanisms such as drift, diffusion, or bipolar amplification [74,75]. Indeed, considering the contributions of these mechanisms in the charge collection can lead to a notable difference between the amount of charge deposited in the RPP volume by the incident ion and the amount of charge effectively collected at the circuit node. A possible expansion of the single sensitive volume RPP method is to consider several distinct SVs or nested volumes, as depicted in Fig. 10(b). A weighting of the contributions of the different volumes to the collected charge is introduced to describe intracell variation in charge collection. The model quantifies the charge collection at a node by an individual particle event as a linear combination of the charge deposited in each volume SV_i scaled by the respective coefficient α_i which is related to the collection efficiency (see Fig. 10(b)) [76] by

$$Q_{col} = \sum_i \alpha_i Q_{Dep,i} = K\sum_i \alpha_i LET_i \times \ell_i \quad (22)$$

The principle of nested regions allows to model the spatial

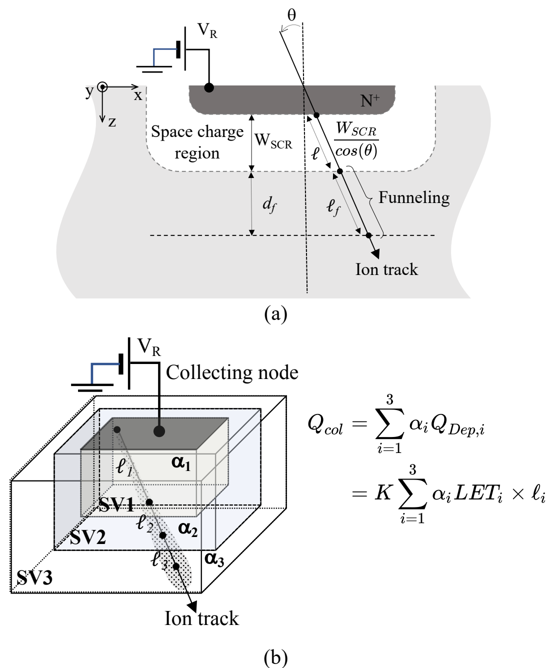


Fig. 10. (a) Definition of quantities used in Hu's funneling model [73], and (b) conceptual drawing of an ionizing particle passing through three sensitive volumes. The total collected charge for the event is the sum of the charge generated in each segment ℓ_i in volume SVi scaled by the collection efficiency for that region α_i. (Adapted after Warren et al. [74], © IEEE 2007.)

charge collection efficiency that falls off with distance from the sensitive node. For example, and as illustrated in Fig. 10(b), we could imagine an incident particle directly passing through and ionizing the innermost sensitive volume SV_1 with 100% charge collection efficiency whereas those passing through a region immediately outside this volume could have only 50% charge collection efficiency in SV_2 and 25% in SV_3.

The determination of the geometry, dimensions and collection efficiency of the different nested volumes can be typically performed using TCAD simulation (Section IV.D). Once more, the concluding remark of Section II.C takes on its full meaning: the nested volumes characterizing the collection of charge at a sensitive node can be defined only once per TCAD simulation, which then makes it possible to carry out a complete simulation of the circuit without using again TCAD simulations of higher level, which saves significant time.

To conclude, one additional remark: pushing this model to its limits with a very large number of SV (which would result in segmenting the trace of the particle into elementary sections), naturally leads to the collection-diffusion approach in which the expression of α_i coefficients are derived from the diffusion law.

B. Diffusion-collection models

In the so-called "diffusion-collection" models, the energy lost by a charged particle in the semiconductor material along its track is converted in electron-hole pairs that are rearranged in the form of a succession of point charge densities of electrons and holes, δn and δp respectively with $\delta n = \delta p = \delta n_0$ just after energy deposition and creation of the pairs (see Fig. 11(a)). The model then assumes that the transport of these discrete charge densities is governed by a pure 3D spherical diffusion law in all regions of the semiconductor domain

$$\frac{\partial n(r,t)}{\partial t} = D\nabla^2 n(r,t) \tag{23}$$

where D is the diffusion coefficient.

In the neutral semiconductor region and in the absence of an external electric field, the separation of electron-hole pairs induces an internal field drawing the electrons and holes back together (this electric field arises from the small charge imbalance that inevitably occurs as low-mobility holes try to keep up with higher mobility electrons). Consequently, when the particle track begins to expand in its radial direction, electrons and holes in the track are foremost transported together and diffuse in train. This corresponds to ambipolar diffusion and the coefficient D in (23) must be taken equal to the ambipolar coefficient D^* given by

$$D^* = \frac{(n+p)D_n D_p}{nD_n + pD_p} \tag{24}$$

where D_n and D_p are the diffusion coefficients for electrons and holes, respectively, n and p are the total electron and hole densities, respectively.

The ambipolar diffusion constant has an intermediate value between D_n and D_p but numerically closer to the diffusion constant of the less mobile species (holes in this case). For longer times after track formation when carrier densities are reduced, D reverts to its value D_n, the diffusion coefficient of electrons in the semiconductor at equilibrium. Equation (23) can be analytically solved with the limit condition $\lim_{t\to 0} \delta n(r_0,t) = \delta n_0$.

The excess carrier density at time t and distance r from the initial track element δn_0 is

$$\delta n(r,t) = \frac{\delta n_0}{(4\pi D^* t)^{\frac{3}{2}}} exp\left(-\frac{r^2}{4D^* t} - \frac{t}{\tau}\right) \tag{25}$$

where τ is the carrier lifetime.

The resulting elementary current density due to this pure diffusion process from the initial track element δn_0 is

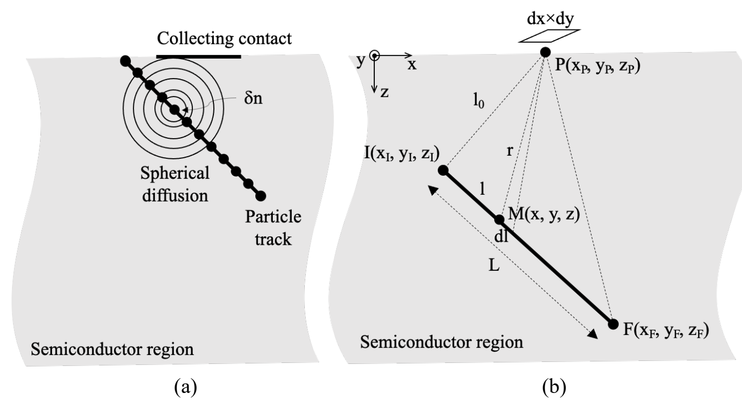
$$\delta\vec{J}(r,t) = qD\vec{\nabla}(\delta n). \tag{26}$$

The corresponding diffusion current passing through a given closed surface S is then given by

$$\delta I_{diff} = \iint_S \delta\vec{J}(r,t)\cdot\overrightarrow{dS} = qD\iint_S \vec{\nabla}\delta n\cdot\overrightarrow{dS}. \tag{27}$$

From these preliminary results established for a single point charge density δn_0, we can now generalize (25) and (27) in the case of a charge deposited along a particle track. Let consider the case illustrated in Fig. 11(b) with the following considerations:

- The ionizing particle of kinetic energy E is emitted (or arrives) at point $I(x_I,y_I,z_I)$ and stops at point $F(x_F,y_F,z_F)$.
- The total charge deposited by this particle is $Q_0 = qn_0 = qE/E_{e,h}$ where $E_{e,h}$ is the mean energy of creation for



(a) (b)

Fig. 11. (a) Schematic illustration of the diffusion-collection model principle: the ionizing particle track is divided in small elements containing $\delta n = \delta p$ electrons and holes which are able to isotropically diffuse towards the collecting electrode, and (b) definition of the main notations used in the model.

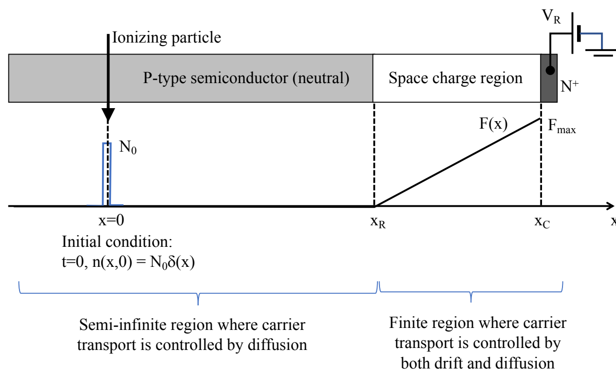


Fig. 12. The one-dimensional (1D) problem of radiation-induced carrier transport in the presence of a non-constant electric field. At t=0, the ionizing particle deposits a charge N_0 in x = 0 (Dirac distribution).

an electron-hole pair in the semiconductor bulk material. For simplicity, this charge is supposed to be linearly deposited between I and F.

The integration of (25) along the track segment IF gives

$$n(t) = \frac{n_0}{8\pi L D t} exp\left(-\frac{{l_0}^2}{4Dt} - \frac{t}{\tau}\right) exp\left(\frac{K^2}{L^2 4Dt}\right) \times \left\{ erf\left(\frac{1}{\sqrt{4Dt}}\left(L + \frac{K}{L}\right)\right) - erf\left(\frac{K}{L\sqrt{4Dt}}\right)\right\} \quad (28)$$

According to (27), the diffusion current passing through an elementary surface of dimensions $\Delta x \times \Delta y$, centered in point P and perpendicular to axis (Oz) is given by

$$\Delta I_{diff}(t) \approx qD\frac{\Delta n(t)}{\Delta z} \times \Delta x \Delta y \quad (29)$$

where $\Delta n(t)/\Delta z$ is the gradient of n in the z-direction at time t, numerically evaluated from (28) at two points, P and $P'(x_P, y_P, z_P+\Delta z)$. The discrete summation of (29) over a given surface S (divided in $\Delta x \times \Delta y$ elements) perpendicular to axis (Oz) directly gives the diffusion current $I_{diff}(t)$ that can be extracted by an electrode of surface S located at this level. Finally, the complete current pulse resulting from the passage of the ionizing particle in the semiconductor region can be computed from (28) and (29) considering a time mesh with uniform or nonuniform spacing (with a geometric progression for example).

The current pulse analytically calculated from the previous procedure is a diffusion current, without any contribution of an electric field in such a pure diffusion approach. In this sense, it ignores the contribution of the electric field of the space charge region in the transport and collection mechanism (Fig. 6). Several methods and model improvements have been published these two last decades that attempt to solve this important limitation of the diffusion-collection approach. Briefly, all these methods modify the evaluation of the current, which is no longer based on the diffusion gradient, but which relies on the introduction of a collection velocity at the level of the collecting electrode. In its simplest revised version, the charge given by (28) is converted into a current by multiplying n(t) by the elementary charge and by the average collection velocity υ_{col} evaluated over the space charge region of the reverse-biased drain. This quantity is then integrated on the surface S of the collecting electrode

$$I(t) = q \iint_S v_{col} \cdot n(t) dx dy \quad (30)$$

In (30), υ_{col} can be evaluated using different approaches, for example derived from the average value of the drift velocity induced by the junction electric field [30] or calculated using a time-dependent model including the time variations of the ambipolar diffusion coefficient [77].

Important remark: To conclude, a final remark concerning the diffusion-collection approach. Unfortunately, this model cannot analytically treat the case of two adjacent domains for which diffusion is the main mechanism on one domain and drift-diffusion controls the transport on the other domain, as illustrated in Fig. 12. This important case corresponds to the 1D modeling of a N^+/P junction with the bulk semiconductor region (neutral zone) and the space charge region.

We recall here that, in presence of an electric field F, (23) can be rewritten in 1D as

$$\frac{\partial n}{\partial t} = \frac{\partial}{\partial x}\left[D\frac{\partial n}{\partial x} + \mu_n n F\right] \quad (31)$$

Equation (31) can be fully analytically solved on a single infinite domain with constant D and μ_n in the case of F = 0 or F

$= F_0$ on the whole domain. Suppose that at t=0, $n(x,0) = N_0\delta(x)$; we then have the two following evident solutions

$$F = 0 \qquad n(x,t) = \frac{N_0}{\sqrt{4\pi Dt}} exp\left(-\frac{x^2}{4Dt}\right) \tag{32}$$

$$F = F_0 \qquad n(x,t) = \frac{N_0}{\sqrt{4\pi Dt}} exp\left(-\frac{(x-\mu_n F_0 t)^2}{4Dt}\right) \tag{33}$$

Equation (33) does not apply in the case of Fig. 12, even if a constant electric field $F_m = F_{max}/2$ is considered in the space charge region, because carriers are subjected to the action of the electric field only from $x = x_R$ and not from x = 0.

There is no analytical solution of (31) for the problem illustrated in Fig. 12. On other words, it is thus impossible to obtain an analytical expression of $n(x_C,t)$ from which a collected current could be derived. This important limitation of the methods justifies the development of the fast numerical method presented below.

C. Random-walk drift-diffusion model

The random-walk drift-diffusion (RWDD) model is a particle Monte Carlo method that simultaneously simulates drift, via a velocity term derived from the electric field, and diffusion with a random-walk algorithm simulating a Brownian motion [78,79,80]. In a similar way to what was done in the diffusion-collection method (Fig. 11(a)), an ionizing particle track crossing a circuit at silicon-level is modeled as a series of charge packets spread along a straight segment whose length equals the ionizing particle range in the target material (see Fig. 13). The linear density of the charge packet along the particle track takes into account the non-constant LET of the particle. The Stopping and Range of Ions in Matter (SRIM) code [81,82] or approximate functions [83] can be used to compute both LET and range for the incoming particle. The accuracy of this charge discretization is ensured by the degree of "granularity" that can be fine-tuned by selecting the packet size, in practice from 1 to 100 elementary charges.

The transport and recombination of the electron and hole charge packets starts immediately after the particle crosses the device. Excess carriers diffuse and drift in the "background" electric field that existed before the particle impact (at equilibrium). In this sense, the transport is decoupled from the electrostatic problem (Poisson equation) that remains unchanged. The drift-diffusion motion from instants t to t + Δt of a charge packet located at **r**(t) is calculated as follows

$$\mathbf{r}(t+\Delta t) = \mathbf{r}(t) + \mu^* t\mathbf{F}_0(\mathbf{r}(t)) + \mathbf{N}_3(0,1)\sqrt{2D^*\Delta t} \tag{34}$$

where μ^* and D^* are the carrier ambipolar mobility and ambipolar diffusion coefficient (given by (24)), respectively, $\mathbf{N}_3(0,1)$ is a 3D standard normal random vector (i.e., a triplet of reals between 0 and 1 distributed following the normal distribution [84]), and F_0 is the electric field before the particle strike.

At each time step of the simulation, the radiation-induced collected current is computed from the transport dynamics of minority charge packets governed by (34) and recombination is also considered by "killing" certain electron and hole packets, considering a fixed or a local carrier lifetime, as explained in the following.

- For the estimation of this collected current, two main procedures may be employed: the first technique is to use the semi-conductor transport equations, the second is to apply Schockley-Ramo's theorem. Simulation tools used in microelectronics generally consider the first option; the transport equations are implemented in a TCAD simulator that numerically solves them self-consistently with Poisson's equation. This approach considers the free-charge carrier distributions as continuous functions in time and space coordinates. The second option is generally used in instrumentation or high-energy physics for the calculation of detector responses to transient radiation events. In this second approach, Ramo's theorem is used to treat each carrier considered individually and all the effects due to a given population of carriers are summed [85]. In our work, we implemented the first formalism (transport equations) by applying the continuity equation at the collecting (drain) contact. The transient current at the collecting node is directly computed from the number of carriers Δn that reach this contact during the time step Δt, i.e.

$$I(t) \approx q \times \frac{\Delta n}{\Delta t} \tag{35}$$

  In this expression, the displacement current is neglected, a reasonable approximation in this case [86]. This collection current is then injected in the electrical simulation to model the circuit response.
- For modeling carrier recombination, a simple implementation consists in considering an exponential law that decreases the number of charge packets as a function of time: $N(t) = N_0 \exp(-t/\tau)$. In this exponential law, N_0 is the initial number of charge packets deposited by the particle at $t = t_0$ and the time constant τ is equal to the average carrier lifetime. At each time step, the number of surviving packets is then fitted to N(t) via a random killing of excess packets. A more sophisticated implementation has been proposed by Malherbe et al. [87]. It considers a local evaluation of the lifetime of excess carriers, which is given by $\tau = \delta c/R$ where δc is the local excess density of carriers with respect to the equilibrium before particle strike and R is the total recombination rate (including Shockley-Read-Hall and Auger recombination). Certain packets are "killed" with a local probability of $\Delta t/\tau = \Delta t \times R/\delta c$ (note that this only simulates geminate recombination, for simplicity).

The practical implementation of the RWDD model is greatly facilitated by using an object-oriented programming language, that offers considerable advantages in terms of advanced structures, such as classes, objects, and containers [80]. For example, the particle track can be then defined as a container including all the charge packets described as independent objects. The members of the charge packet class include the geometrical coordinates of a given packet and its electrical charge. The container content may change during the simulation due to two different mechanisms cited previously:

(1) carrier recombination or (2) carrier extraction that corresponds to particles that escape the simulation domain. This object-oriented programming of RWDD should facilitate the simulation of complex circuits with an arbitrary number of sensitive areas and collecting nodes, intrinsically considering, in this case, multiple node charge collection in the simulation process. As also explained in [80], in the RWDD approach, the behavior of each packet of charge is computed independently of the other charges. These processes being independent, the task of calculating the charge transport can be easily parallelized on a graphic processing unit (GPU) whose internal architecture is perfectly adapted to such a massive parallelism. Moreover, the RWDD model needs to implement a random number generation procedure that is usually time-consuming; if the random numbers are independent, this task can also be easily parallelized on GPU.

These two characteristics of the RWDD model are expected to result in a considerable improvement in computation speed, since the number of parallelizable tasks in RWDD is relatively high. In [79], an acceleration factor ×140 was reported using a single GPU unit with respect to the classical CPU implementation for the simulation of 100,000 charge packets with 1,000-time steps.

Fig. 13 illustrates a typical RWDD simulation. At t_0, a 5 MeV alpha particle is emitted in a reverse-biased N+/P junction; its track partially overlaps the space charge region. At t_0 + 10 ps, the particle track has considerably radially extended and minority charge carriers (here electron packets in red) in the SCR are drawn into the electric field and begin to approach the collecting N^+ region. At t_0 + 40 ps, the drift regime in the SCR and the isotropic diffusion in the neutral substrate region are clearly visible, the track segment in the substrate tends to become a spherical cloud of charge packets that continues to extend with time. At t_0 + 0.1 ns, minority carriers in the SCR are less numerous, they have been massively collected at the N+ electrode. The SCR remains supplied with carriers which are transported by diffusion in the substrate, and which are entrained by the electric field as soon as they enter the SCR.

Fig. 14 shows a direct comparison of the transient currents and the corresponding charges collected by the drain of the NMOS transistor subjected to a 5 MeV alpha particle striking the center of the drain perpendicularly to the device, obtained from RWDD and TCAD simulations. One can observe a few differences between the two curves, especially in the early stages of the transient, mainly due to: i) the arrival of discrete charge packets at the level of the collecting drain contact in RWDD which induces inherent granularities; ii) the slightly delayed charge generation considered in the TCAD simulation due to the introduction of a temporal distribution in the generation rate (see section IV.D), and iii) because in RWDD the transport is decoupled from the electrostatic problem (Poisson equation), contrary to TCAD. Values of the collected charges obtained from TCAD and RWDD are very close at the end of the transient event, with a difference limited to a maximum of 15%, indicating that both modeling approaches have, in this case, very similar charge collection efficiencies.

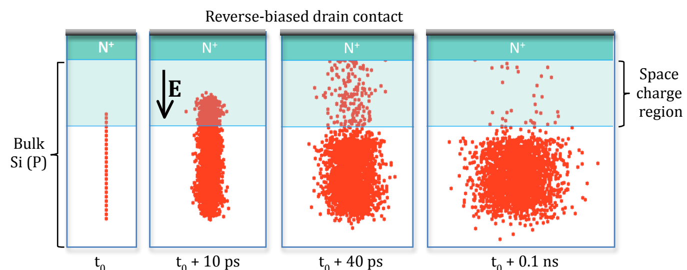


Fig. 13. Schematic illustrating the charge transport and collection processes after a 5 MeV alpha-particle strike in a reverse-biased junction (its geometrical and electrical parameters correspond to the 65 nm node). The biased contact collects charges that diffuse in silicon and are accelerated by the electric field developed in the space charge region. (After Glorieux et al. [79], © IEEE 2014.)

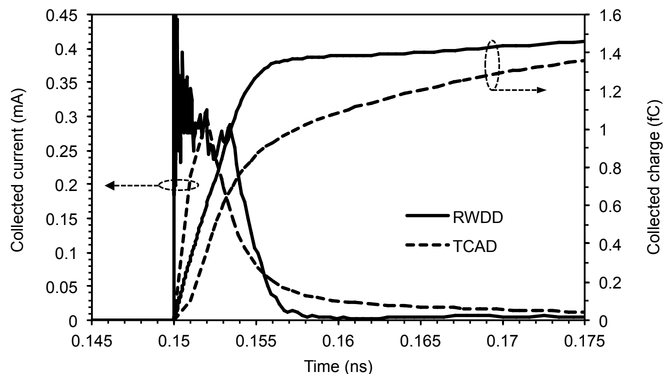


Fig. 14. Current and charge collected by an isolated OFF-state NMOS transistor (designed in 65 nm CMOS technology) after a 5 MeV alpha particle strike computed by TCAD and by the RWDD model. (After Autran et al. [78], © Elsevier 2014.)

D. *TCAD simulation*

TCAD simulation, also known as numerical modeling (i.e., based on the numerical resolution of a set of physics equations) aims to quantify the understanding of the underlying technology and abstract this knowledge for use in circuit design. It consists of two distinct parts: the simulation of the manufacturing process (not described in this short course) and the simulation of the device electrical operation (device electrical simulator). This type of simulation does not generally correspond to a large circuit approach; it is restricted in practice to a single device, a circuit cell or a portion of a given circuit limited to a few units/tens of transistors. TCAD simulation is nonetheless an essential step in the development of integrated circuits and microelectronics.

TCAD electrical simulation models the electrical behavior of a device/circuit cell of interest, considering its 3D geometry, materials, and doping profiles. The effects of radiation on the device operation can be also simulated at this electrical simulation-level. The starting point of the electrical simulation is the device/circuit cell of interest. It is represented as a meshed structure where each node has specific associated properties such as the type of material, the dopant concentration, etc. This mesh is used for solving the main differential equation such as the Poisson equation and the transport and continuity equations, as described in section III.B. As previously mentioned, solving self-consistently the set of equations (8)-(12) in the three spatial dimensions and in a time domain including the passage of the ionizing particle up to the return to equilibrium is a very

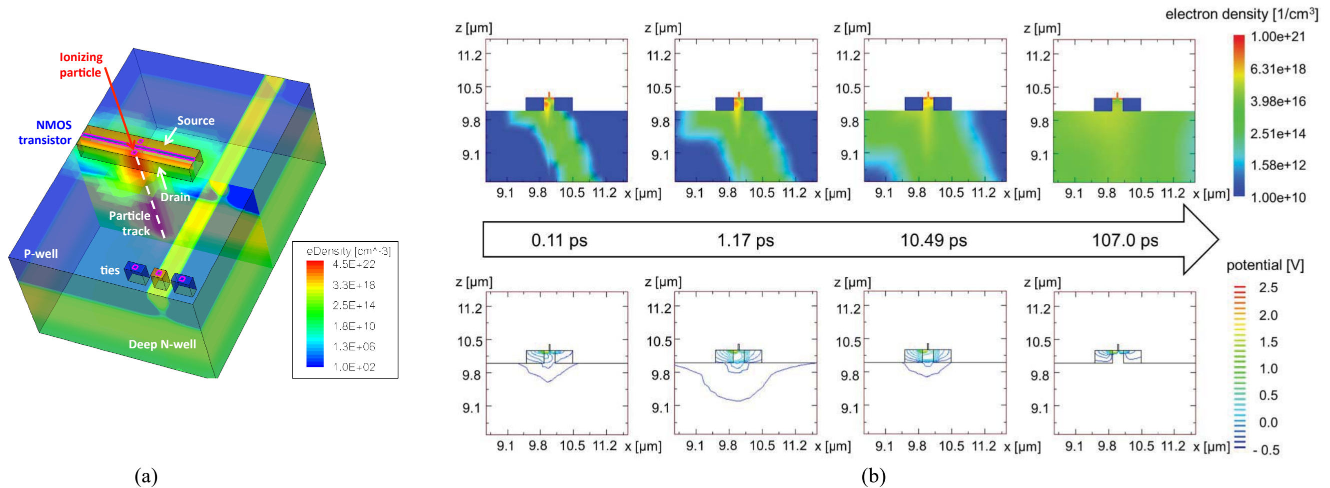


Fig. 15. (a) 3D electron density distribution obtained by TCAD simulation at 2 ps after an alpha particle strikes the drain of an OFF-state isolated NMOS transistor (designed in 65 nm CMOS technology). To facilitate the picture analysis, spacers, gate material, and isolation oxide are not shown here. The long arrow indicates the location and direction of the ionizing particle strike (Reprinted from Autran et al. [78], © Elsevier 2014), and (b) time evolution of the electron density and of the electrostatic potential in a 32 nm NMOSFET after the simultaneous generation of five ion tracks, created to simulate the nuclear reaction n + ^{28}Si → 3n + 2p + 2α + ^{16}O initiated by a 233 MeV neutron in the device. (After Abe et al. [88], © IEEE 2011.)

complicated process. The simulation starts with different initialization steps that concern device geometry, mesh properties, charge density and biases applied to the different device electrodes. After this initialization, the discretized Poisson equation is solved and the electrostatic potential in the device is calculated. The potential is afterward injected directly into the resolution of the continuity equation. The output of this module is used to calculate a new carrier density to be used in the Poisson equation. In this way, a new potential is found and is injected into the continuity equation and so on. The loop stops when the convergence criterion is reached.

In such a simulation scheme, the effect of a particle strike in the device is included in (9)-(10) in the form of a generation rate, depending on several radiation characteristics and representing an external generation source of carriers. This radiation-induced generation rate G is added to the other conventional generation rates that account for various direct generation-recombination mechanisms occurring in the device. A general expression for G is the following

$$G(w,l,t) = F(l) \times R(w) \times T(t) \tag{36}$$

where F(l) gives the number of electron-hole pairs (per unit of length) created by the ionizing particle along its path, R(w) is a radial distribution function and T(t) is a temporal distribution function. With respect to quantities introduced in (36), the particle track is described in a cylindrical coordinate system (w, θ, l) that specifies point positions by the radial distance *w* from the track axis, the azimuth angle θ (the axis rotation corresponds to the particle axis) and the axial coordinate *l* with respect to the origin O of the particle track.

F(l) has the following expression

$$F(l) = \frac{dN_{ehp}}{dl} = \frac{1}{E_{e,h}}\frac{dE}{dl} \tag{37}$$

where N_{ehp} is the number of electron-hole pairs created by the particle strike, E is the energy of the particle and $E_{e,h}$ is the mean value of energy for electron-hole pair creation in the considered material (given by (6)). F(l) varies as a function of the particle penetration in the material, expressed as the distance *l* traversed by the particle in the matter along its path. The quantity dE/dl is related to the LET of the particle.

For conservative reasons, the radiation-induced generation rate given in (36) must fill the condition

$$\int_0^\infty \int_0^{2\pi} \int_0^\infty G(w) dw d\theta dt = \frac{dN_{ehp}}{dl} \tag{38}$$

Consequently, functions R(w) and T(t) are subjected to the following normalization conditions

$$2\pi \int_0^\infty R(w) w dw = 1 \qquad \int_{-\infty}^\infty T(t) dt = 1 \tag{39}$$

Ion track models implemented in commercial TCAD simulators usually propose an exponential function or a Gaussian function for the spatial distribution function

$$R(w) = \frac{1}{\pi r_C^2} exp\left[-\left(\frac{w}{r_C}\right)^2\right] \tag{40}$$

where r_C is the characteristic radius of the Gaussian function. The temporal distribution function is usually modeled by a Gaussian function

$$T(t) = \frac{1}{t_C\sqrt{\pi}} exp\left[-\left(\frac{t}{t_C}\right)^2\right] \tag{41}$$

where t_C is the characteristic time of the Gaussian function. The characteristic time and the characteristic radius are two key-parameters for tuning the radiation-induced pulse duration and the ion track width, respectively, during a simulation run.

Figs. 15(a) and 15(b) provide two examples of TCAD simulations. In Fig. 15(a), a 65 nm NMOS transistor was impacted by a 5 MeV alpha particle striking the center of the drain perpendicularly to the device. The radiation-induced charge was generated along the particle track using (36) with a characteristic radius of 20 nm and a characteristic time of 2 ps.

In Fig. 15(b), a more complex event, requiring the simultaneous generation of five ion tracks in a 32 nm NMOS transistor was performed [88]. This simulation aimed at reproducing the impact of a high energetic neutron (233 MeV) in the device, initiating a nuclear reaction with a silicon nucleus of the target material (n + ^{28}Si → 3n + 2p + 2α + ^{16}O). The linear density of charge deposited by the secondary ions and the ion track were assumed to have a Gaussian radial distribution with a characteristic radius of 30 nm. The device simulation was performed using the drift-diffusion method in the 3D TCAD simulator HyENEXSS (Hyper Environment for Exploration of Semiconductor Simulation). In Fig. 15(b), the time evolution of the electron density and of the potential is shown after the five ion tracks were simultaneously created. Within tens of ps, the distortion of potential is formed and the charge collection by drift is enhanced. The potential variation becomes relaxed with time. The variations of the transient current response and the collected charge as a function of time (not shown here, see [88]) show that an initial high drain current is induced due to drift. After about 100 ps, the potential distortion disappears, and diffusion dominates the charge collection process.

V. Mixed-mode and circuit simulation

Simulation at circuit-level is essential for studying, understanding, and anticipating the impact of radiation on the real circuit operation and architecture, not reducible to a single device isolated from the rest of the circuit. A wide variety of techniques can be envisaged. First, we can distinguish two main approaches:

1) The methods based on sensitive volume(s) at device or circuit level that considers scoring quantities (deposited energy, LET, …) and related criteria (critical charge, threshold LET, I_{max}-t_{max}, …) to evaluate the SEE event rate of a given device/circuit architecture. In these methods, the electrical operation of the device/circuit of interest is implicitly considered in the criterion used to determine if a given event is able or not to induce an error.

2) The methods based on a device/circuit electrical simulation to determine the impact of a given radiation on the circuit operation. In this case, the electrical operation is performed explicitly using various techniques. These include pure circuit simulation (SPICE), mixed-mode approaches and full numerical methods (TCAD). The "stimulus signal" (current or voltage transient) resulting from the passage of a particle in the sensitive region of the device/circuit can be obtained from different models able to catch, more or less accurately, the complex physics of the transport and collection of the radiation-induced charge. These models include the diffusion-collection models (see section IV.B), the RWDD approach (see section IV.C), and other full numerical methods, such as TCAD, or more sophisticated solutions of the transport problem treated using the Green's function formalism [21].

In the following, without wishing to be exhaustive, we examine a few approaches to illustrate this variety of methods that exist to investigate SEEs at circuit level.

A. *Circuit simulation with analytical SET current pulses*

Circuit simulators solve systems of equations that describe the electrical operation of circuits, such as Kirchhoff's current and voltage laws. The basic components of these codes are compact models describing the operation of all elementary devices (transistors, diodes, resistors, etc..) constituting the circuit. For simulating single-event effects at circuit level, a single-event induced transient is usually modeled as a current source connected at the struck node of the circuit. Different models exist for reproducing the shape of the SET that is experimentally measured or obtained via full numerical simulation. One of the most popular solutions is the use of a double exponential current transient pulse, originally proposed by Messenger [89]

$$i_{inj}(t) = \frac{Q}{t_f - t_r}[exp(-t/t_f) - exp(-t/t_r)] \quad (42)$$

where Q is the collected charge (i.e., the integral of the pulse), t_r is the rising time constant, and t_f is the falling time constant. In principle, the same current model may be used for simulating the particle hits in both P-type channel (PMOS) and N-type channel (NMOS) MOS transistors, and the only difference will be in the direction of the current flow at the level of the current source implemented in the circuit netlist [90].

Numerous other models for the SET induced current have been proposed. Andjelkovic et al. have proposed a classification in [90]. The authors distinguished six major groups of models, respectively based on: single voltage-independent current sources, voltage-dependent current sources, two voltage-independent current sources, piecewise interpolation, lookup table, as well as an alternative approach to the current injection models employing a switch and a series resistor to reproduce the SET response. These different approaches have both advantages and drawbacks in terms of accuracy, implementation, and calibration, which should be considered in practical applications. For example, in (42), the time constants t_r and t_f are technology related. According to [89], the time constant t_f can be expressed by

$$t_f = \frac{k\epsilon_0\epsilon_{Si}}{q\mu N} \quad (43)$$

where ε_0 is the permittivity of vacuum, ε_{Si} is relative permittivity of silicon, q is the electron charge, μ is the minority carrier mobility, and N is the substrate doping density of the collecting junction. There is no straightforward equation to determine the value of t_r, but it is generally given in terms of t_f, as reported in [90]: for example, $t_f = 3.28 \times t_r$ in [91], and $t_f = 4.6 \times t_r$ in [92]. In general, the value of t_r is in the range from several ps to tens of ps, while the value of t_f is in the range from tens of ps to hundreds of ps.

Another SET model has been proposed by Kauppila et al. [93]. This model is a compact voltage dependent SET current model that associates in parallel an independent current source I_{SRC}, a capacitor C_S and two voltage-dependent current sources G_{REC} and G_{SEE}. The capacitor C_S stores the charge which is

equivalent to the SET and its value can be chosen arbitrarily. The independent current source I_{SRC} is basically the standard double-exponential current source and the two sources G_{REC} and G_{SEE} account for the recombination process and the variation of the node voltage due to the induced charge, respectively. As noted by Andjelkovic et al. in their review, the current model proposed by Kauppila et al. allows the SET-induced current to be accurately characterized, particularly the plateau observed for high LET values when the impacted junction is embedded in a CMOS inverter [90,93] (see also section V.B).

Fig. 16 shows the circuit schematic of a generic four-transistor static random-access memory (SRAM) cell. The passage of an ionizing particle in the $NMOS_2$ drain is electrically simulated with an external SET current source connected to the struck node. At this level, the aforementioned SET models can be used to provide a given SET transient pulse that is injected during the transient simulation. The selection of the SET current source is the user's choice.

To solve the transient simulation problem defined in Fig. 16, when the circuit architecture is composed of only a few connected devices, the steady-state circuit electrical solution can be simply solved considering Kirchoff's circuit laws and compact models for transistors. In the following, the method is illustrated for the case of the SRAM cell. Considering that the particle strikes the OFF-state NMOS transistor termed $NMOS_2$ (initial conditions $V_1 = 0$, $V_2 = V_{DD}$) the time variations of potential V_2 for the sole and isolated inverter #2 can be written as

$$\frac{dV_2}{dt} = \frac{-i_{inj}(t) + I_{DP2}(V_1 - V_{DD}, V_2 - V_{DD}) - I_{DN2}(V_1, V_2)}{C_N} \quad (44)$$

where $i_{inj}(t)$ is the current pulse given by (42) due to the particle strike and collected on the node 2, I_{DN2} and I_{DP2} are the currents of the $NMOS_2$ and $PMOS_2$ transistors, respectively and C_N is the node capacitance. $I_{DN2}(V_{GS},V_{DS})$ and $I_{DP2}(V_{GS},V_{DS})$ depend on two input parameters: the gate-to-source bias (V_{GS}) and the drain-to-source bias (V_{DS}). For example, in (44) for the PMOS transistor $V_{GS}=V_1-V_{DD}$ and $V_{DS}=V_2-V_{DD}$.

Considering now the full SRAM cell composed of the two cross-coupled inverters, we obtain the following system of two coupled differential equations

$$\begin{cases} C_N \frac{dV_1}{dt} = I_{DP1}(V_2 - V_{DD}, V_1 - V_{DD}) - I_{DN1}(V_2, V_1) \\ C_N \frac{dV_2}{dt} = -i_{inj}(t) + I_{DP2}(V_1 - V_{DD}, V_2 - V_{DD}) - I_{DN2}(V_1, V_2) \end{cases} . \quad (45)$$

Equation (44) for the sole and isolated inverter #2 or (45) for the SRAM cell can be easily solved in the time domain, using a 4th order Runge-Kutta method [94] with a time step Δt.

In (45), NMOS and PMOS source-to-drain currents are modeled using a compact or analytical model, which is the user's choice. One possible choice between all the transistor models available is the EKV 2.6 MOSFET model [95,96] since it represents a very good compromise between accuracy and complexity. This is a predictive (scalable) compact model for the simulation of submicron CMOS technologies, considering fundamental physical characteristics of the MOS structure. The

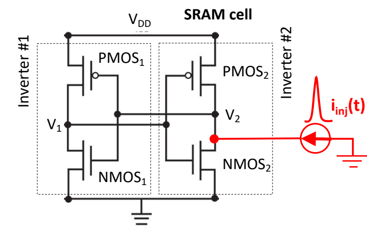


Fig. 16. Circuit schematic of an SRAM cell formed by two cross-coupled CMOS inverters. The passage of a particle in the $NMOS_2$ drain is electrically simulated with an external SET current source connected to the struck node.

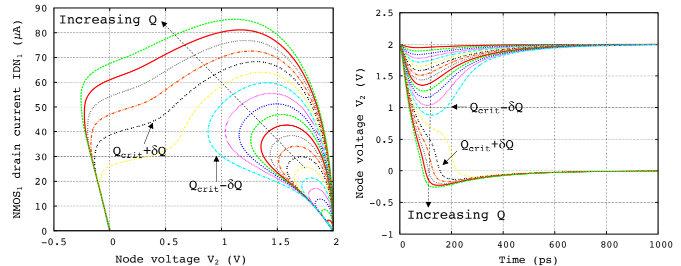


Fig. 17. Example of SRAM transient simulations based on (45) for different current pulses with increasing Q in (42). The cell upsets when Q becomes larger than Q_{crit}, the critical charge of the SRAM. Simulations performed for a generic 0.35 µm CMOS technology using the C++ implementation of the EKV 2.6 MOSFET model [95,96].

drain current formulation can be coded in around 100 lines of C++. Fig. 17 illustrates the numerical solutions of (45) for an SRAM cell subjected to current pulses on node #2 (see Fig. 16) with increasing charge values Q in (42). The cell upsets when Q becomes larger than Q_{crit}, the critical charge of the SRAM.

For more complex circuit architectures than a single inverter or an SRAM cell, a circuit simulator must be used in the place of small and dedicated programs for circuit solving. An abundance of literature exists on the soft error characterization methods of advanced CMOS technologies based on circuit simulation. A nice example is given by work conducted by Li and Draper on both combinational circuits and sequential elements [97]. They carried out a detailed analysis to characterize, using HSPICE®, the impact of single transients induced by one particle hit in various circuits, including redundant flip-flop (FF) structures. They adopted the double exponential current pulse model (42) to describe the shape of the radiation-induced current pulse. Fig. 18(a) illustrates the characterization of a feedback redundant SEU-tolerant (FERST) FF, where circuit nodes N_1 and N_3 are coupled with N_2 and N_4, respectively. To flip the stored value, two independent current sources $Igen_1$ and $Igen_2$ are attached to the cross-coupled nodes N_1 and N_2 with deposited charge Q_1 and Q_2, respectively. The use of two current sources allows the effect of charge sharing [13,98,99] on the two circuit nodes N_1 and N_2 to be emulated. As a result of the particle strike, the stored value is changed when Q_1 and Q_2 are large enough, as depicted in the error map of Fig. 18(b). This table is built for each cross- coupled pair of nodes, which records the mappings from deposited charge values at the cross-coupled nodes to the result whether an error is induced, given a certain FF logic state and clock signal value. Similar steps are repeated for other

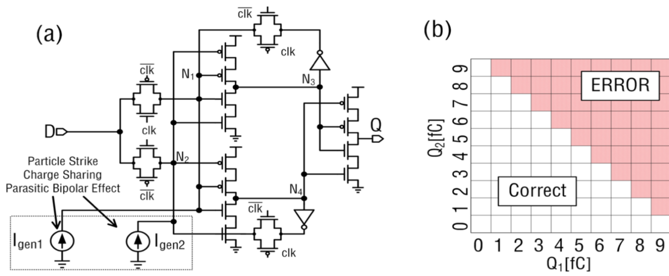


Fig. 18. Example of hardened flip-flop circuit characterization using two independent current sources that emulate charge sharing effects induced by the particle strike on circuit nodes N_1 and N_2. (After Li and Draper [97], © ACM 2017.)

cross-coupled nodes, e.g., N_3 and N_4, to characterize the circuit.

B. Radiation transport coupled with circuit simulation

The injection on a circuit node of a given "stimulus" signal, electrically emulating the impact of an ionizing radiation, does not necessarily correspond to reality, both regarding the real behavior of the circuit and its influence on the signal itself. Indeed, the process of collecting charges induced by radiation is a dynamic process: the charge (or the current) collected modifies the potential of the collector node and induces a counter-reaction of the circuit to this change which will modify the collection process, and so on. To illustrate this effect, we explore the same case as in Fig. 14, but this time with the NMOS transistor embedded in a CMOS inverter. Because the device is now not isolated (standalone), the drain voltage is no longer fixed at the constant voltage V_{DD}. The drain voltage corresponds to the voltage of node V_2 that depends on the operation of the second transistor of the CMOS inverter. This leads to the variation of the voltage V_2 during the transient process. These node bias changes may modify the charge collection efficiency at the drain of the NMOS transistor, through the variation of both the electric field F and the width of the space charge region W_{SCR} via a feedback process. To consider such a feedback effect, using the RWDD model, the magnitude of the current (given by (35)) varies at each time step due to the variations of W_{SCR} and F that depend on the voltage node V_2, which is also updated at each time step by the circuit simulator.

Simulated transients of the CMOS inverter (under the initial conditions $V_1 = 0$ and $V_2 = V_{DD}$) obtained with the RWDD model when a 5 MeV alpha particle passes across the NMOS drain are shown in Figs. 19(a) and 19(b). These results reveal the influence of the circuit feedback on the SCR characteristics, through the time changes of V_2. Without the circuit feedback on the SCR, the radiation effect turns V_2 to negative values for a period equal to about 30 ps. This obviously reveals a dummy condition for a cross-coupled inverter in the case of an SRAM cell (somewhat reduced by the gate capacitance in the case where the second inverter is coupled). Fig. 19(b) illustrates an important issue concerning the inverter operation: the dummy condition described above persists 2× as long when SCR feedback is activated.

In the most general case, where the radiation transport code is coupled with an external circuit simulator, a watchdog process is inserted between the radiation transport code and the circuit simulator to ensure that the two codes are working in interactive mode. The coupling between the two solvers requires an efficient exchange of numerical information at each iteration (time step), generally in the form of current and voltage data. A simulation run consists of a certain number of simulation loops, each loop corresponding to a time incrementation (constant or variable time step) in the time domain analysis. At each step, the radiation code transports the radiation-induced charge in the structure and the circuit simulator solves the circuit equations and updates the node potentials that are used in the next step for the radiation transport, and so on, until the entire time domain is covered.

Fig. 20 illustrates this mixed-mode methodology for an

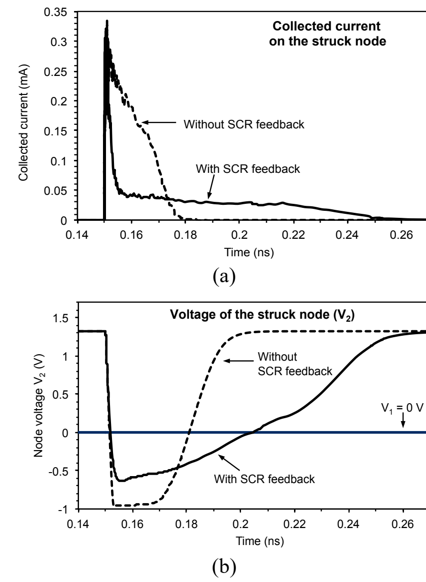


Fig. 19. (a) RWDD simulation of the impact of an ionizing particle on an off-state NMOS transistor embedded in a CMOS inverter with and without the feedback effect of the space charge region (width and electric field dependence on V_2) on the collected current, and (b) on the voltage on the struck node. (After Autran et al. [78], © Elsevier 2014.)

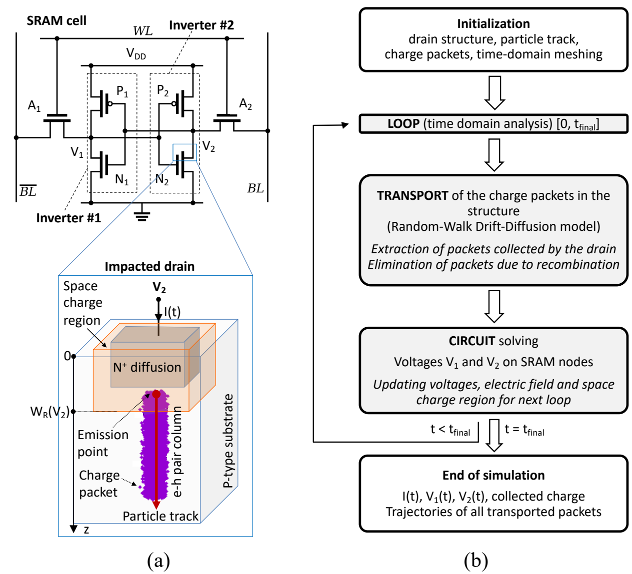


Fig. 20. (a) Mixed-mode methodology for an SRAM cell combining the RWDD transport model (impacted drain) and SPICE simulation, and (b) simplified flowchart of the simulation. (Adapted after Moindjie et al. [100], © Elsevier 2019.)

SRAM cell combining the RWDD transport model at the level of the spatial region limited to the impacted drain and SPICE simulation at the level of the four-transistor SRAM cell.

C. Mixed-mode TCAD applied to SEEs

Mixed-mode TCAD tools [21,30,101] constitute a particular case of the previous solutions in so far as the coupling between the full numerical electrical simulation, including the radiation transport, and circuit simulation is directly included as "mixed-mode" or "mixed-level" simulation in all major commercial simulation suites, such as Synopsys® [61], Silvaco® [62] or Cogenda® [63]. Often available in TCAD tools, this mixed-mode approach can be used in two different ways [101], as illustrated in Fig. 21 and discussed below:

- The first possibility is to numerically simulate only a single transistor of the circuit, with all others simulated using compact models. This approach is the most used in circuit simulation, for applications needing to reproduce the operation of a particular device very accurately. An example of this approach is the simulation of radiation effects in memory cells. In this case, the device that needs to be numerically simulated is the device struck by the ionizing particle. Only the struck transistor is modeled in the 3D device domain, the other transistors of the memory cell are simulated using compact models. The current transient resulting from the ion strike on the struck device is directly computed by device domain simulation. Thus, the inaccuracy of the circuit simulation due to the current transient used as a stimulus can be eliminated.
- A second possibility is to numerically simulate all individual transistors of the integrated circuit and to connect them through the mixed-mode interface, which describes the operation of the total system. Computational resources and software constraints limit this type of simulation to circuits containing a maximum of a few tens of transistors (such as inverters, ring oscillators with few stages, individual memory cells or FF latches).

In the mixed-mode approach, the two simulation domains (device and circuit) are closely connected by boundary conditions at contacts, and the two solvers exchange numerical information at specific intervals (iterations, time steps) and at specific locations (boundaries of the TCAD 3D model and the corresponding node/branch of the circuit schematic) [101]. For instance, the circuit simulator may calculate appropriate voltages and apply them at the TCAD 3D model boundaries (contacts), and in response to the applied voltages, the TCAD solver calculates contact currents and feeds them back into Spice [101].

This approach provides several interesting advantages. First, mixed-mode TCAD can capture the dynamic interaction of the physical charge collection process with the surrounding circuit [101]. Errors inherent to compact models or inaccuracies of input stimulus can be avoided by full device numerical simulation. It is also possible to access internal physical quantities of the numerically simulated device (such as potential, electric field, densities of carriers) at any time during

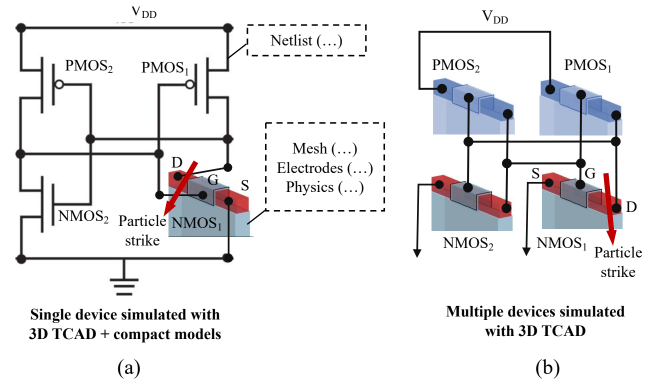


Fig. 21. Illustration of two mixed-mode approaches for the simulation of an SRAM cell with a single transistor (a) or the totality of the devices (b) numerically simulated in the 3D device domain and connected via a circuit netlist (the remaining transistors, in the first case, being simulated using compact models). (Adapted after Munteanu et al. [102,103]).

the mixed-mode simulation. Furthermore, mixed-mode approaches may be used to simulate the operation of small circuits made on emerging devices (such as ultra-scaled multiple-gate or silicon nanowire-based architectures [102,103,104]) and/or to take into account new physical phenomena (e.g., quantum confinement [104] or quasi-ballistic transport) for which compact models do not exist or are still not satisfactory in terms of accuracy. In this case, all transistors contained in the small circuit can be simulated in the 3D device domain. More particularly, the mixed-mode approach has been successfully used to simulate ionizing radiation impact on these new devices and associated small circuits. The main drawback of the mixed-mode approach is the increased computational time compared to a pure circuit simulation. In addition, mixed-mode simulation is not feasible for complex circuits and in the case where there is a coupling effect (charge sharing) among adjacent devices. Given that the spacing between devices decreases when reducing the device dimensions, it is expected that coupling effects become increasingly important; in this case the numerical simulation of the full circuit in the 3D domain may become mandatory.

D. Monte Carlo circuit simulation using specialized codes

Monte Carlo (MC) methods are computational methods that use random numbers to model stochastic processes, or to model deterministic processes that can be approximated by stochastic ones. The Monte Carlo approach is the numerical method of choice for problems that model objects interacting with other objects or their environment based upon simple object-object or object-environment relationships [105]. Monte Carlo-based physical simulations of SEEs in electronics solve the radiation problem in two main steps: 1) the interaction of radiation with the device and the subsequent motion of charges, and 2) the resulting changes in nodal currents and/or voltages, within the device/circuit [31,49,50]. Since this simulation chain is complex due to its multi-scale and multi-physics character, the same simulation engine cannot generally cover these two steps. For example, the interaction of radiation with the device and the subsequent motion of charges can be fully simulated using a general-purpose code as previously cited (section III.A) but the resulting changes at device or circuit level require an electrical

simulator or dedicated code. Due to the computational cost (central processing unit (CPU)-time), the transport of the radiation-induced charges in step #1 is also often processed by another program or a specially designed code based on a simplified transport model and optimized algorithm.

Dozens of code developments in this domain have been reported in the literature. In 2013, an extended review paper by Reed et al. ([51], completed with [54]), presented the contributions from different groups, each developing and/or applying Monte Carlo-based radiation transport tools to simulate a variety of effects that result from energy transferred to a semiconductor material by a single particle event. The topics span from basic mechanisms for single-particle induced failures to applied tasks such as developing websites to predict on-orbit single-event failure rates using Monte Carlo radiation transport tools [51,54]. Following on from [51,54], Table II proposes an updated list of the most recent codes, including several references published since 2013. To illustrate some basic principles and general properties of these specialized codes in the computation of SEEs, we now examine several examples from recent literature.

Particle-matter interactions and radiation transport: The first main difference between all these codes is the way in which the particle-matter interactions are generated, and the radiation transported. We can distinguish three main cases:

- The code is built from the "ground up", using nuclear and radiation transport physics or uses radiation transport libraries designed by the high-energy physics community (e.g., Geant4). Intrinsically, the code can directly compute, during a simulation run, all the steps related to incoming particle generation and source emulation, interaction event generation, ion transport through the device/circuit geometry and finally scoring calculations with respect to sensitive volume(s). Additional routines can also be added to handle the transport of electric charges using various models. This approach is used in MRED or TIARA-G4.
- The code uses a precompiled Monte Carlo tool (e.g., FLUKA, PHITS or MCNP) to perform similar calculations to the previous case, but in a more constrained framework because the exchange of information with the precompiled tool can only be done through input and output files which have a strict format. It is always possible to extend the code capabilities by external routines or to encapsulate the precompiled code in proprietary software by making a dynamic link and by managing the inputs and outputs from the developed code in a transparent way for the user. It is also possible to transfer output data to another code to continue the SEE simulation at the electrical level. This approach is used in PHITS-HyENEXSS or G4SEE.
- The code does not directly use Monte Carlo radiation transport codes, libraries or precompiled codes but directly computes and manages incident particle generation, particle-matter interactions and charged particle transport itself, using precompiled event databases for nuclear interactions and additional data (SRIM tables [81,82] or behavioral modeling [83]) to describe the transport of ions. This approach is preferentially used in MC-ORACLE, MUSCA-SEP3 or TIARA for example. The use of nuclear interaction event databases considerably reduces the computational time but requires a delicate treatment of the management of events in the case of complex architectures using several or many different materials.

Energy deposition, charge transport and collection: The second differentiation criterion between these specialized codes is the way in which the particle energy is deposited, and the electrical charge is transported in the simulation domain and collected on the sensitive circuit node(s). Very schematically, two main approaches can be distinguished:

- For the codes which consider a circuit as a set of sensitive volumes, the electrical charge deposited is directly deduced from the energy deposited by the particles at the level of these sensitive volumes. The code therefore performs particle calorimetry by considering the sensitive volumes as detectors. A deposited energy spectrum is then obtained. The scoring of the particles is carried out for each sensitive volume, which makes it possible to estimate the deposited charge by considering the average creation energy of the electron-hole pairs in the target material. More refined models, like nested sensitive volumes, deduced from separate TCAD simulation (as explained in section IV.A), and implemented in MRED for example, can be used.
- For codes that have a specific module to transport the electrical charge, energy is first deposited along the path(s) of the ionizing particle(s) traversing the simulation domain and converted to electron-hole pairs. The ambipolar transport of this charge in-excess starts and minority carriers are transported then collected by the sensitive nodes that are, in this case, biased electrodes. Diffusion-collection models presented in section IV.B can be used at this level, as performed in several codes, for instance MC-ORACLE, MUSCA SEP3 or TIARA. Otherwise, a full numerical resolution of the Poisson and continuity equations can be performed, using internal solvers, as in MRED, or by outsourcing the task to an external program called via a dedicated input-output interface, as performed for example in PHITS-HyENEXSS.

Device/circuit response: The electrical response of the impacted device, cell or circuit can be deduced from a simple criterion, for example a critical charge criterion or from the I_{max}-t_{max} criterion as in MC-ORACLE or TIARA. Alternatively, a more complex criterion can be envisaged, considering a part or the totality of the circuit response simulated with a circuit simulator. The call to the circuit simulator can be invoked at the end of the charge transport and collection process or during the collection process itself, to take into account the circuit counterreaction, as illustrated and discussed in section V.B.

3D circuit construction and link with the electrical circuit: In addition to all the differences highlighted between these specialized Monte Carlo codes, perhaps one of the most important is the ability of a given code to consider any complex circuit and to apprehend its complexity at different

TABLE II
SPECIALIZED MONTE CARLO SIMULATION CODES APPLIED TO SEES IN ELECTRONICS CIRCUITS. THE ASTERISK INDICATES CODES PARTIALLY BASED ON GEANT4 SIMULATION TOOLKIT [38,39].

Program name	Main ref.	Lab. Affiliation	Acronym definition / Short description
ACCURO	[122,123]	Robust Chip	Device and circuit simulation with fast single event analysis (commercial tool).
MCEA*	[125,126]	CEA-DIF	Monte Carlo code for estimating the SEU sensitivity of a memory array
CLUST-EVAP, PROPSET, PROTEST	[51]	NASA/Johnson Space Center	Monte Carlo proton reaction and transport codes
CUPID	[51]	Clemson University	Clemson University Particle Interactions in Devices
FLUKA	[40,41,51]	Fluka collaboration	General-purpose Monte Carlo energetic particle reaction and transport code
GRAS*	[51]	ESA	Geant4 for Radiation Analysis for Space
G4SEE*	[106,107,108]	CERN	Geant4 for SEE Monte Carlo simulation tool
IRT*	[58]	Intel	Intel Radiation Tool
MCNP / MCNPX	[42,43,51]	Los Alamos National Laboratory	Monte Carlo N-Particle eXtended / a software package for simulating nuclear processes
MC-ORACLE	[51,58,60]	University of Montpellier-2	Monte Carlo predictive code for SET and SEUs
MRED*	[31,49,50,51,127]	Vanderbilt University	Monte Carlo Radiative Energy Deposition
MUSCA SEP3*	[51,56, 57]	ONERA	MULti-SCAles Single Event Phenomena Predictive Platform / Monte Carlo SEE predictive tool
NOVICE	[51]	EMPC	Radiation transport/shielding code
PHITS	[44,45,51]	JAEA, RIST, KEK and other institutes	Particle and Heavy Ion Transport code System / a general purpose Monte Carlo particle transport code
PHITS-HyENEXSS	[52,124]	Kyushu University	Monte Carlo simulation code linking PHITS and HyENEXSS simulators
SEMM / SEMM-2	[46,47,48,51]	IBM	Soft Error Monte Carlo Model
TFIT	[109,110]	iRoC Technologies	Cell Level Soft Error Analysis (commercial tool)
TIARA*	[53,54,55,87], [111-121]	STMicroelectronics Aix-Marseille University	Tool suIte for rAdiation Reliability Assessment

levels: at the material and device levels, at the circuit architecture level and at the electrical level. In other words, a complete simulation platform should ideally be able to perform an SEE simulation with a maximum of details concerning the circuit architecture given from standard circuit definition files used in microelectronics: a schematic, a physical layout in GDS format and a transistor-level netlist. To perform this task, the code must create, at the beginning of the simulation sequence, a structure that represents the circuit both in the physical and electrical domains.

To illustrate this point, we take the example of the last version of the TIARA code, named TIARA Industrial Platform [55] that has extended capabilities in this domain. Malherbe has described in [121] in details the circuit building processes implemented in TIARA: given a layout file of the circuit, a so-called Builder3D module constructs a three-dimensional structure of the circuit in the physical domain (Fig. 22). The module also takes as input a geometrical description of the technology process stack: roughly speaking, the layout provides us with the top-view data (“X” and “Y” coordinates), and the process stack is the side-view information needed to extrude the patterns into layers of a certain thickness along the “Z” axis. TIARA’s 3D structures are collections of axis-aligned boxes, which seems a reasonable choice for the layouts in modern technologies, down to the device level. Note that layout files encode arbitrary polygons (closed chains of vertices), and thus TIARA must first perform a meshing operation to convert the paths into non-overlapping rectangles. After the geometrical structure of the circuit is built, the LVSmatcher module is used to map physical locations to electrical nodes in the netlist. Such a physical-to-electrical mapping is needed for TIARA to identify the sensitive circuit nodes at which to inject the radiation-induced currents, when provided only with the geometrical location of the event [121]. This is performed by the LVSmatcher module, which runs a custom Layout Versus Schematic (LVS) comparison to match the layout and netlist

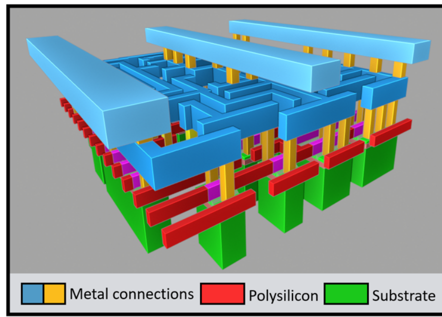


Fig. 22. Example of a generated 3D structure by TIARA Industrial Platform (2021) corresponding to a 28 nm fully depleted (FD) silicon-on-insulator (SOI) flip-flop circuit with two metal layers. (After Thery et al. [55], © IEEE 2021.)

connectivity graphs. The complete description of this method can be found in [121].

Data post-processing, event visualization and metrics estimation: All specialized Monte Carlo codes have at least one or several dedicated modules to aggregate simulation results, prepare output files for event visualization and mappings using two- or three-dimensional (2D/3D) viewers, calculate histograms and estimate various statistical metrics, such as the device/circuit cross section or the soft error rate. The management of intermediate calculation files and log files are also important, to keep track of as many parameters as possible and to save them in correct final formats. Some aspects of data visualization and scoring that may have an important role in the verification of the convergence of an SER for a large-scale simulation, event visualization in the case of remarkable events, detailed scoring to better understand SEE mechanisms on a nuclear physics level or event mapping to identify sensitive area at layout level, can be found for example in [23,127,128].

VI. Circuit-Level Soft Error Analysis

Soft Error Rate (SER) estimation and analysis is an important challenge for Very-Large-Scale Integration (VLSI) circuits that cannot be simulated, due to their complexity, using a simulator or a specialized code. Historically, soft errors have first affected memory circuits because of the large area of the chips devoted to caches and the higher vulnerability of SRAM cells in comparison to combinational logic [16]. However, technology scaling, especially in the past decade, has increased the SER in logic circuits by several orders of magnitude, making it comparable to the SER of unprotected memory for modern technologies [129]. In what follows we briefly examine the modeling of the SER in both memory circuits and in combinational logic.

A. Soft error rate in memory circuits

In an SRAM memory circuit, for a given supply voltage and for a given drain architecture, the SER can be directly linked with the critical charge via an exponential relationship (suggested by the experiment), as originally established by Hazucha and Svensson in [130,131] in the case of soft errors induced by high energy atmospheric neutrons

$$SER = \kappa \times F \times A \times exp\left(-\frac{Q_{crit}}{\eta_S}\right) \tag{46}$$

where K is a scaling factor (assumed to have the same value for all technologies), F is the neutron flux with energy above 1 MeV (cm^2s^{-1}), A is the area of the circuit sensitive to particle strikes, in cm^2, Q_{crit} is the critical charge and η_S is the charge collection efficiency of the device for a given type of radiation, both expressed in the same unit (fC).

Two key parameters for SER are Q_{crit} and η_S. These model parameters are determined by fitting (46) to a set of experimental SER data and simulated critical charge data. A lower Q_{crit} means a priori more soft errors. η_S and Q_{crit} are determined by the process technology [131], whereas Q_{crit} also depends on characteristics of the circuit, particularly the supply voltage and the effective capacitance of the drain nodes, as we will analyze later in section VI.C. Q_{crit} and η_S are essentially independent, but both decrease with decreasing feature size. Equation (46) shows that changes in the ratio $-Q_{crit}/\eta_S$ will have a very large impact on the resulting SER. The SER is also proportional to the area of the sensitive region of the device, and therefore it decreases proportionally to the square of the device size. Changing the supply voltage requires finding a new value for the collection efficiency η_S following a method proposed by Hazucha and Svensson in [131].

In [132], Torrens et al. analyzed the dependence of the SER on the design parameters of pull-down NMOS and pull-up PMOS transistors in regular parameter-variation tolerant 6T-SRAM cells. They used the expression proposed by Heijmen et al. [133] in which the SER is expressed for both the sensitive NMOS and PMOS of the SRAM cell as

$$SER = \kappa\left(A_{diff,e} \times e^{-\frac{Q_{crit,e}}{\eta_e}} + A_{diff,h} \times e^{-\frac{Q_{crit,h}}{\eta_h}}\right) \tag{47}$$

where $A_{diff,e}$ and $A_{diff,n}$ are the NMOS and PMOS sensitive drain area, respectively, $Q_{crit,e}$ and $Q_{crit,h}$ denote the critical charge for upsets due to the collection of electrons and holes at the sensitive drains of the NMOS and PMOS transistors, respectively, and κ is a parameter that depends on the radiation flux (κ = A×F defined in (46)). Parameters η_e and η_h are the charge collection efficiency for electrons and holes, respectively. To compute SER, parameters κ, η_e and η_h must be obtained experimentally (as they are device- and environment-dependent) [132]. In practice and as discussed in [132], (47) can be simplified to (46) and the SER can be computed from $Q_{crit,e}$, because $Q_{crit,e}$ is always inferior to $Q_{crit,h}$. However, the model precision increases when both electron and hole collection are considered. To link the SER expression in (47) with electrical and geometrical parameters of the SRAM cell, Torrens et al. proposed an analytical model of Q_{crit} that will be discussed in subsection VI.C. The analytical developments described in [132] allows calculating the critical charge and the SER from technological parameters giving insight on the relative contribution of each design parameter, notably the transistor geometry and the supply voltage.

B. SER of combinational logic

Modelling and analyzing the SER in logic is more complex than in memory elements, since there is an exponential number of input vectors, signal correlations and combinations with pulse widths [134]. However, in combinational logic gates, the same considerations of Q_{crit}/η_S can apply for single event transient (SET) pulse generation. For a complete analysis, however, one must also consider how SET masking factors scale across process nodes. Indeed, there exist some masking effects that reduce the likelihood that a particular SET within a circuit will be latched and cause an error. These masking effects are commonly classified as [16,30,134]:

- Logical masking: this occurs when a particle strikes a portion of the combinational logic that cannot affect the output due to a subsequent gate whose result is completely determined by its other input values. For example, as illustrated in Fig. 23(a), if the strike happens on an input to a NAND (NOR) gate but one of the other inputs is in the controlling state (e.g., 0(1) for a NAND (NOR) gate), the strike will be completely masked and the output will be unchanged (i.e., the particle strike will not cause a soft error).
- Electrical masking: this occurs for transients with bandwidths higher than the cutoff frequency of the CMOS circuit. These transients will then be attenuated [135]. The pulse amplitude may reduce, the rise and fall times increase, and, eventually, the pulse may disappear (as shown in Fig. 23(b)). On the other hand, since most logic gates are nonlinear circuits with substantial voltage gain, low-frequency pulses with sufficient initial amplitude will be amplified [134].
- Temporal masking (or latching-window masking): this occurs when the pulse resulting from a particle strike reaches a latch, but not at the clock transition where the latch captures its input value. This is explained in Fig. 23(c): when the transient propagates towards a sequential element (a latch in the present case), the disturbance on node DIN may be outside the latching window. Hence, the error will not be latched, and there will be no soft error.

Due to these masking effects the soft error rate in combinational logic has been found to be significantly lower than expected. Additional to these masking mechanisms, two key-factors impact the soft error rate in combinational logic: the clock frequency and the SET pulse width [30]. With increasing clock frequency there are more latching clock edges to capture a pulse which causes the error rate to increase. The pulse width is a key parameter which determines both the distance the SET will travel through the combinational chain and the probability that the SET be latched in a memory element as wrong data. The wider the SET pulse width, the greater probability it has of arriving on the latching edge of the clock. If the transient becomes longer than the period of the clock, then every induced transient will be latched. The SET pulse width and amplitude depend on both process and circuit parameters (substrate and/or epitaxial layer doping, circuit capacitance, etc.).

A wide variety of SER estimation methods and formulations

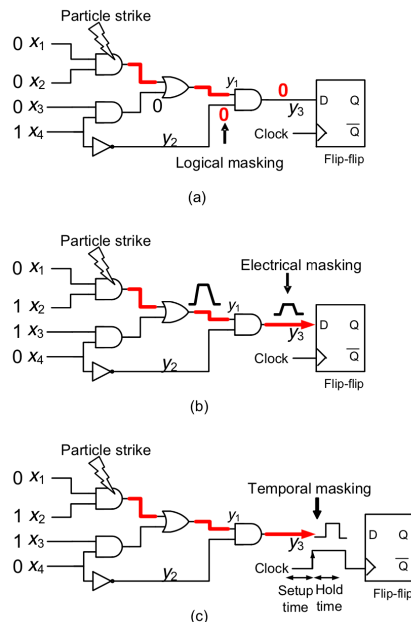


Fig. 23. Illustration of three masking effects: (a) logical, (b) electrical, and (c) temporal. (After Yu [136].)

exist in the literature with important differences that are not always clearly distinguished. Certain approaches assume particle hits at individual circuit nodes [136,137,138], other models consider them on the gate as a whole [129]. Conditional and unconditional error models must be also distinguished. A conditional error model allows the error probability to vary with respect to different input vectors, while an unconditional error model requires the error probability to be constant, and therefore independent of the input vectors [136]. As an illustration of the SER estimation methods developed, we briefly discuss in the following the approach developed by Anglada et al. [129]. In their recent work, the overall SER of a given combinational circuit can be computed as the accumulation of the individual SER of all the logic gates in the circuit [129]

$$SER_{circuit} = \sum_{i=1}^{N_{gates}} SER_{gate_i} \quad (48)$$

where SER_{gate_i} is defined as the probability that a particle with a particular charge q strikes at gate #i and the SET originated is not masked. SER_{gate_i} is computed by integrating the product of the probability that a particle striking the gate causes an SET and the non-masking probability over the range of charges able to induce a soft error

$$SER_{gate_i} = K \times A_{gate_i} \times F \times \int_{Q_{crit_i}}^{\infty} f_Q(q) \times V(gate_i, q) dq \quad (49)$$

where K is an overall scaling factor, A_{gate_i} and Q_{crit_i} are the area and the critical charge for the gate #i, respectively, F is the particle flux, V is the vulnerability of gate #i for the collected charge q (defined below) and f_Q is the probability density function of collected charge, defined in [138,139] as a function of the charge collection efficiency η_S

$$f_Q(q) = \frac{1}{\eta_S} \times exp(-q/\eta_S) \quad (50)$$

In practice, the integral in (49) is often approximated as a discrete sum (N_C terms)

$$SER_{gate_i} = \sum_{c=1}^{N_C} R_{PH}(gate_i, q_c) \times V(gate_i, q_c) \quad (51)$$

$$R_{PH}(gate_i, q_c) = K \times F \times A_{gate_i} \times exp(-q_c/\eta_S) \quad (52)$$

where q_c corresponds to a discrete charge selected from the continuous range: $q_c = c \times (q_{max} - Q_{crit_i})/N_C$. In [129], it is reported that a discretization of the integral in five intervals yields an accurate enough SER estimation in comparison to SPICE models. The vulnerability of a gate is defined as the probability that a soft error propagates up to a latch. It can be formulated as

$$V(gate_i, q_c) = LM(i,c) \times EM(i,c) \times TM(i,c) \quad (53)$$

which corresponds to the probability that the SET with charge q_c at gate #i is neither affected by the logical masking factor (LM) nor the electrical masking factor (EM) nor the timing masking factor (TM). The computation of the different non-masking probability factors in (53) is a complex task that requires a specific calculation strategy for each type of masking. It must also include the reconvergent fanouts (when a logic signal splits into multiple branches and later reconverges in two or more inputs of a gate) that break the assumption that signal paths are independent [129], even if most of the gates are not sources of reconvergence. The complete algorithm to estimate the SER in a circuit from (48), (51), (52) and (53) is given and discussed in [129].

C. Critical charge modeling in SRAM

As mentioned in section IV.A, the critical charge (Q_{crit}) is a first-order metric that has been introduced to characterize the circuit sensitivity to SEEs [18]. It corresponds to the minimum amount of charge induced during a particle strike that, after being transformed into current, will result in a change of logic level across the target node. Q_{crit} can be used as a parameter for assessing the circuit sensitivity to single event transients (SETs) induced in combinational logic and single event upsets (SEUs) induced in sequential elements [18]. Since the value of the critical charge is used as input for the evaluation of the soft-error rate at a high-description level, accurate determination of the critical charge is of great importance for the design of radiation tolerant circuits and systems.

In the case of an SRAM cell (Fig. 16), Q_{crit} can be simply modeled as a sum of capacitance and conduction components of the impacted node [30]

$$Q_{crit} = C_N V_{DD} + I_{DP} t_F \quad (54)$$

where C_N is the equivalent capacitance of the struck node, V_{DD} is the supply voltage, I_{DP} is the maximum current of the on-state PMOS transistor ($PMOS_1$ in Fig. 16) and t_F is the cell flipping time. While both capacitance and conductance components indeed contribute to this critical charge, the first term is generally overestimated because the flipping threshold of an inverter is less than V_{DD} ($V_{DD}/2$ for perfectly matched NMOS and PMOS). In addition, the conductance term only considers the peak value of the current, which is not realistic. A more correct way for estimating the critical charge has been proposed by Xu et al. [140]

$$Q_{crit} = \int_0^{V_{trip}} C_N dV + \eta I_P T_{pulse} \quad (55)$$

where V_{trip} is the static tripping point of the SRAM cell defined as the threshold voltage at the struck node required to flip the cell content, η is a correction factor, I_P is the driven current of the on-state PMOS transistor and T_{pulse} is the duration of the particle-induced current pulse I_{pulse}. Equation (55) provides a better estimation of the capacitance component of Q_{crit}, particularly the effect of junction capacitance and the addition of the backend metal-insulator-metal (MIM) capacitor. However, this model fails to incorporate the dynamics of the voltage transient at the struck node, the quantitative description of I_{pulse}, and the contributions of the different transistors that constitute the cell. As a result, the accuracy of (55) in estimating Q_{crit} is also limited.

Improved analytical techniques for solving Q_{crit} in SRAM cells with reduced discrepancies (≤ 10% and below with respect to full SPICE simulations) have been proposed in recent years by Zhang et al. [141], Jahinuzzaman et al. [142], Mostafa et al. [143,144] and Torrens [132]. These different models consider the dynamic behavior of the cell and decouple the nonlinearly coupled storage nodes with different approaches. Decoupling of storage nodes enables solving associated current equations to determine the critical charge, usually for a simple or double exponential pulse current.

In [144], Mostafa, Anis, and Elmasry developed a full Q_{crit} analytical model, considering a decoupling solution for the system of differential nodal current equations at node #1 and #2 of the SRAM cell (Fig. 16)

$$\begin{cases} C_1 \frac{dV_1}{dt} = [i_{p1} - i_{n1}] - i_{inj}(t) \\ C_2 \frac{dV_2}{dt} = [i_{p2} - i_{n2}] \end{cases} \quad (56)$$

where C_1 and C_2 are the capacitances of the nodes #1 and #2, respectively, i_{p1} and i_{n1} (respectively i_{p2} and i_{n2}) are the currents of transistors $PMOS_1$ and $NMOS_1$ (respectively $PMOS_2$ and $NMOS_2$), respectively, and i_{nj} is the transient current pulse connected here to node #1 and modeled by a simple exponential current pulse given by

$$i_{inj}(t) = \frac{Q}{\tau} exp(-t/\tau) \quad (57)$$

where Q is the total charge deposited by this current pulse at the struck node, and τ is the falling time.

After a long analytical development, the authors show that the critical charge can be expressed as follows

$$Q_{crit} = Q\,[1 - exp(-t_f/\tau)] \quad (58)$$

where Q is the total charge for a current pulse to be able to upset the cell, and t_f is the cell flipping time that has for final expression (using the branch W_{-1} of the Lambert function)

$$t_f = -\tau\left[1+\frac{C_1V_{DD}/2}{\tau[i_{p1}-i_{n1}]}+W_{-1}\left(-exp\left(-1-\frac{C_1V_{DD}/2}{\tau[i_{p1}-i_{n1}]}\right)\right)\right] + \frac{C_2V_{DD}/2}{[i_{p2}-i_{n2}]} \quad (59)$$

In the above derivation, the different currents i_{p1}, i_{n1}, i_{p2} and i_{n2} must be evaluated for the following and respective gate-to-source $|V_{GS}|$ voltage values: V_{DD}, 0, $V_{DD}/2$ and $V_{DD}/2$. At this level, the use of a transistor analytical model can be envisaged. In [144], the authors suggest considering a unified physical current formula, that is used for all the transistor operating regions, as introduced in [145]. Another solution should be to use the EKV model [95,96] introduced in section V.A or another compact model. Fig. 24 illustrates the verification of the analytical Q_{crit} model ((58)-(59)) with results obtained using SPICE transient simulations. The test circuit considered is a 65 nm CMOS bulk SRAM. The simulations have been repeated for different V_{DD} values (from 0.1 to 1.2 V), to find the effect of reducing V_{DD} on the critical charge. The maximum error reported is 7.2% on Q_{crit} values and the average error is 3.8% with respect to SPICE results.

Another critical charge calculation model has been proposed by Torrens et al. [132] in the framework of a detailed analysis of the SER dependence on transistor design parameters for six-transistor SRAM cells (Fig. 25). In Fig. 25(a), the four transistors, M_{nL}, M_{pL}, M_{nR}, and M_{pR} correspond to the two identical cross-coupled inverters of the latch, while the other two, M_{xL} and M_{xR}, control the latch access during write and read operations. As explained by the authors [132], transistor widths W_n, W_p, and W_x are usually selected to ensure cell stability during write and read operations. These constraints require that the cell ratio defined as $CR = W_{nL,R}/W_{xL,R}$ must be greater than one (usually CR = 1.5 to 2.5) and the pull-up ratio defined as $PR = W_{pL,R}/W_{xL,R}$, must be less than 3. Typically, to minimize cell area, the size of the pull-up transistors and pass transistors are chosen to be minimal (*PR = 1*) [132]. In their study, the authors have explored the modification of transistor widths as a memory cell hardening technique by increasing the minimum allowed widths by a given factor. To maintain a regular layout structure, the widths of all PMOS transistors are incremented by a factor r_p with respect to the minimum allowed width W_{min}, while the widths of all NMOS are incremented by a factor r_n. Such layout modifications prevent the formation of bends in the diffusion regions and maintain the layout structure: $W_p \equiv W_{pL} = W_{pR} = r_p \times W_{min}$ and $W_n \equiv W_{nL} = W_{nR} = W_{xL} = W_{xR} = r_n \times W_{min}$. To evaluate the SER from (46), the authors developed a critical charge model embedding in the equations the transistor and cell geometry. Starting from (55), they first expressed the critical charge $Q_{crit,h}$ related to the collection of holes at the drain of M_{pR} required to flip node R from 0 to 1 and $Q_{crit,e}$ related to electron collection at the drain of MnL required to flip node L from 1to 0. They obtained

$$Q_{crit,h} = C_R V_{trip} + \eta\,|I_{DN}|\,T_{pulse} \quad (60)$$

$$Q_{crit,e} = C_L (V_{DD} - V_{trip}) + \eta\,|I_{DP}|\,T_{pulse} \quad (61)$$

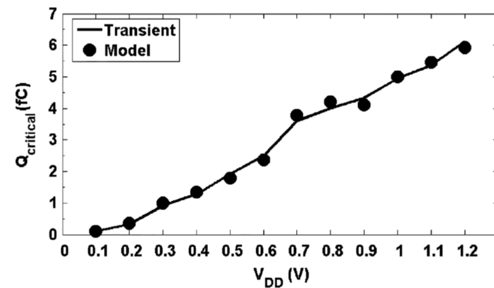


Fig. 24. Comparison of the critical charge versus V_{DD} as estimated using the analytical model ((58)-(59)) and as deduced from transient SPICE numerical simulations considering technological and electrical parameters for a 65 nm CMOS bulk technology. (After Mostafa et al. [144], © IEEE 2011.)

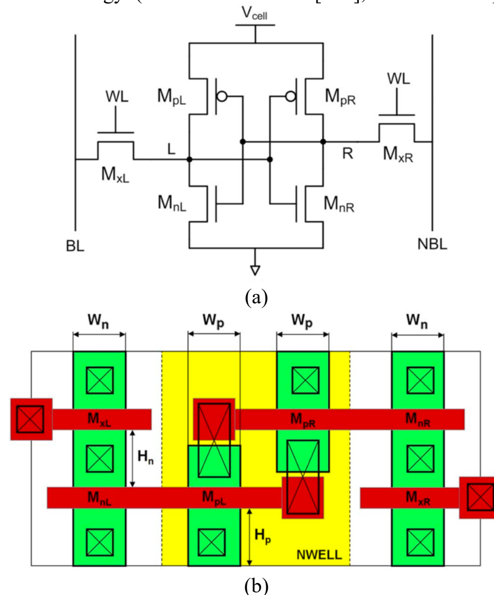


Fig. 25. Schematic (a) and layout (b) of a six transistors SRAM cell with definition of transistor names and key-geometrical dimensions. (After Torrens et al. [132], © IEEE 2014.)

where C_R (respectively C_L) is the equivalent capacitance of the R node (respectively L node), I_{DN} (respectively I_{DP}) is the maximum driving current of the on-state MnR (respectively MpL) device, T_{pulse} is the duration of the particle-induced current pulse, and η is a correction factor to account for the time varying behavior of the restoring current. Here, because of the symmetry of the six-transistor SRAM cell, $C_R = C_L = C$ with C given by

$$C = C_{gn}A_n + C_{gp}A_p + C_{gon}W_n + C_{gop}W_p + C_{jan}A_{diff,n} + C_{jswn}(2H_n) + C_{jap}A_{diff,p} + C_{jswp}(W_p + 2H_p) \quad (62)$$

where $C_{gn,p}$ is the n and PMOS intrinsic gate capacitance, $A_{n,p} = W_{n,p} \times L$ is the gate area, $C_{gon,p}$ is the overlap capacitance, $C_{jan,p}$ and $C_{jswn,p}$ are the source/drain junction area capacitance and the sidewall capacitance, respectively, $A_{diff,n} = W_n \times H_n$ and $A_{diff,p} = W_p \times H_p$, are the NMOS and PMOS diffusion areas (Fig. 25(b)), H_n and H_p being the respective drain diffusion lengths.

Describing the transistor current in the saturation region using the alpha-power law model, and after several substantial analytical developments not detailed here, the authors showed, from calculated data using their model, that the critical charges

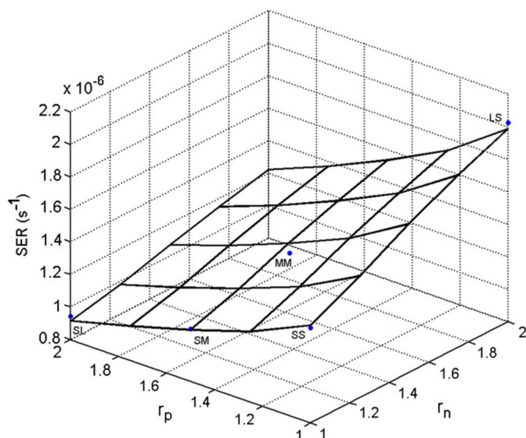


Fig. 26. Surface representing the calculated SER (from (46) using the modeled critical charges) as a function of r_n and r_p along with experimental data points. The parameters used in the model are related to a 65 nm CMOS process (see [145] for their numerical values). (After Torrens et al. [132], © IEEE 2014).

$Q_{crit,e}$ and $Q_{crit,h}$ are quasi-linear functions of W_n and W_p. Setting $W_p = r_p \times W_{min}$ and $W_n = r_n \times W_{min}$, the two critical charges can be approximated by linear relationships with coefficients r_n and r_p in the form

$$\begin{cases} Q_{crit,e} = Q_{0,e} + \chi_{n,e} \times r_n + \chi_{p,e} \times r_p \\ Q_{crit,h} = Q_{0,h} + \chi_{n,h} \times r_n + \chi_{p,h} \times r_p \end{cases} \tag{63}$$

where the six parameters are fitted from calculated data using the complete analytical model for $Q_{crit,e}$ and $Q_{crit,h}$ described in [132]. The maximum discrepancy between the complete analytical model and the linearized equation (63) is below 0.5%. Fig. 26 shows a surface representing the calculated SER from (46) using the modeled critical charges as a function of r_n and r_p. The five points labeled SS, SM, SL, MM, and LS correspond to experimental data measured on 65nm SRAM circuits during alpha particle accelerated SER tests. The five memory blocks correspond to different couples of values for r_n and r_p [132]. Both experimental and simulated SER values show that increasing r_p leads to a desired SER reduction, whereas increasing r_n produces an undesired SER increment. SL cell ($r_n = 1$, $r_p = 2$) is the best cell in terms of SER. Results show that a direct correlation between SER and critical charge is found for all cells having small NMOS ($r_n = 1$ for SS, SM, and SL), and a higher critical charge corresponds to a better SER.

However, not all transistor width enlargements result in a SER improvement. Only PMOS width increase provides a SER improvement, whereas NMOS width increase worsens the cell behavior in terms of SER. While cells SL and LS have the same cell area, the LS-cell SER is twice the SER of the SL one. These very interesting results reveal that SER is reduced by increasing the PMOS transistors channel width when simultaneously maintaining the minimum width for NMOS. As an increase in W_p also reduces cell writability, a tradeoff must be therefore established.

Previous models, TCAD, mixed-mode or full SPICE simulations can be used to study the scaling of Q_{crit} as a function of transistor/circuit feature sizes and geometries. To conclude, Fig. 27 shows that, for recent technologies, Q_{crit} values are now well below the femtocoulomb, an extremely low value of a few thousands of electrons, typically in the same order of magnitude as the charge deposited by very low LET particles, for example a muon or an energetic electron, in a few nanometers of silicon.

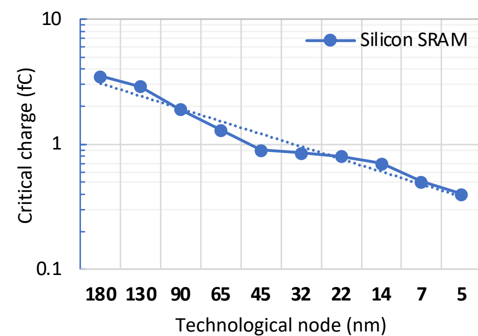


Fig. 27. Typical values of critical charges reported in literature for silicon SRAM memories as a function of the technological node of the International Technology Roadmap for Semiconductors (ITRS). (Data after [146,147,148].)

D. *Critical charge modeling in sequential circuits*

SEEs are also serious design issues in sequential circuits because if a transient fault or glitch occurs at the output of a latch/flip-flop for example, it may lead to a noncritical path turning into a critical path. A conventional D-latch or flip-flop is thus very sensitive to SEU due to high-energy particle strikes. During the low phase of the clock signal, an SEU may upset the logic level of the positive edge-triggered flip-flop, and the corrupted values are not corrected until a new value is stored in the flip-flop. In [149], Kumar et al. developed an accurate semi-analytical model to estimate the critical charge for a static D-latch operating in the sub/near-threshold regime. The proposed model is a function of design parameters such as transistor sizes, supply voltage, and fan-out load.

Fig. 28 depicts the conventional static D-latch circuit studied [149]. It has two paths: the first is the main path which consists of an inverter and the second is the feedback path which consists of an inverter followed by a transmission gate. The static D-latch stores two complementary binary values (0 and 1) at intermediated nodes N_1 and N_2. This conventional latch is more prone to particle strike on intermediated nodes in hold mode (CLK = 0) because, in this state, the intermediate nodes are disconnected from the input (IN) of the latch. A particle strike on the node N_1 (which is held at logic 1) is emulated using a current source $I_{SEU,trip}$ injecting a double exponential current pulse of integral Q. The minimum voltage value at node N_1 at which node N_2 flips from logic 0 to logic 1 is termed as V_{1ebb}. In this case, the PMOS transistor (M_{p1}) of inverter I_1 turns on and changes the logic level of node N_2. The critical charge model developed in this study is based on the fact that the node N_2 is charged from 0 to V_{2C} (the tripping point voltage at node N_2) through the transistor M_{p1} (current I_{Mp1}). The current through transistor M_{n1} (I_{Mn1}) can be neglected because of its negative V_{GS}. Because of the SEU charging of N_1, $V_{SG,p1}$ is nearly equal to V_{DD} while $V_{GS,n1}$ is nearly equal to 0. This is because the value of V_{1ebb} varies from 20 mV to −49 mV for a fan-out (FO) parameter between 0 and 8. Now, Kirchhoff's current law at node N_2 due to SEU on node N_1 can be written

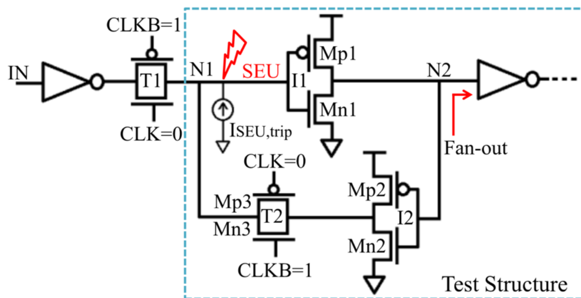


Fig. 28. Static D-latch, which is most commonly used, is susceptible to SEU due to transient fault at node N_1 or equivalently, at node N_2. (After Kumar et al. [149], © IEEE 2019.)

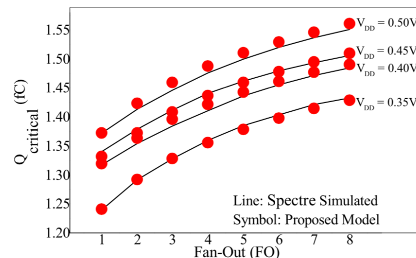


Fig. 29. Validation of the proposed model with SPECTRE simulation for critical charge calculation at V_{DD} = 0.35 V, V_{DD} = 0.4 V, V_{DD} = 0.45, and V_{DD} = 0.5 V in STMicroelectronics 65 nm CMOS technology. (After Kumar et al. [149], © IEEE 2019.)

$$C_{N2}\frac{dV_2}{dt} = I_{Mp1} \quad (64)$$

where C_{N2} is the total capacitance at node N_2. In the subthreshold region, the subthreshold current can be approximated at low V_{DS} by [150]

$$C_{N2}\frac{dV_2}{dt} \approx I_0 exp\left(\frac{V_{GS,p}-|V_{th,p}|}{nV_T}\right) \quad (65)$$

with $I_0 = \mu_0 C_{ox}(W/L)(V_T)^2 \times \exp(\lambda V_{DS})$, where V_T is the thermal voltage, μ_0 is the low-field mobility, W and L are the channel width and length, respectively, C_{ox} is the gate capacitance per unit area and λ is a technological parameter. Knowing that $V_{GS,p} = V_{DD} - V_{1ebb}$, this last quantity can be extracted from (65)

$$V_{1ebb} = (V_{DD} - |V_{th,p}|) - nV_T \times ln\left(\frac{C_{N2}(dV_2/dt)}{I_0}\right). \quad (66)$$

Once the voltage at node N_1 is equal to V_{1ebb}, the feedback path (inverter followed by transmission gate I2-T2) charges node N_1 until $V_2 = V_{2C}$ when it stops charging N_1. Therefore, the critical charge Q_{crit} is obtained as follows

$$Q_{crit} = (V_{DD} - V_{1ebb}) \times C_{N1} \quad (67)$$

where C_{N1} is the total capacitance at node N_1. Equations (66) and (67) constitute the core equations of the model proposed by Kumar et al. to evaluate the critical charge for the static D-latch. In (66), the slope dV_2/dt must be evaluated as a function of the fan-out load, that requires some additional simulations and calculations detailed in [149]. The proposed methodology estimates the critical charge of the static D-latch with a maximum error of 3.4% at different power supplies compared with circuit simulations for a CMOS bulk 65nm technology, as illustrated in Fig. 29. The model also results in 7.5% error at the 32-nm technology node, which is verified using a calibrated TCAD simulation setup [149]. Note the very low values of Q_{crit} in this case: the susceptibility of sequential elements to SEE is high in the near-/subthreshold regime due to their low operating voltage and smaller node capacitances. Finally, the model proposed in [149] can predict the changes in the critical charge accurately for different process corners. This methodology also addresses the issue of critical charge due to process, supply voltage and temperature (PVT) variations.

VII. High-level description at system level

At system-level, the distinction is generally made between faults and data errors. As defined by Jeong et al. in [151], a fault can be classified into a hardware or a software fault depending on where it occurs. A hardware fault, affecting a circuit or system, can be classified into a permanent, an intermittent, or a transient fault according to how long it exists in the considered device. A permanent fault (stuck-at, stuck-open, and bridging faults) remains permanently in the circuit, a transient fault appears and disappears over a brief period of time, and an intermittent fault introduces repetitive broken data in a specific place because of hardware damage [151]. Permanent and intermittent faults occur because of inaccurate specifications, implementation mistakes, or component defects. A transient fault usually occurs because of internal and external perturbation. The data errors that result from a hardware fault include hard and soft errors. The definitions and classification introduced for these errors in section II.A fully apply at this level.

To evaluate system reliability and dependability, the technique of Fault Injection (FI) has been widely adopted. This ensemble of methods is intended to test the behavior of an application running on a given system and to evaluate its tolerance to faults under a realistic set of input stimuli that mimic the final execution environment. Briefly, the basic environment of the FI method includes an FI system and the target system under test (see Fig. 30) [151]. The FI system interacts with the target system for fault generation, control, and analysis. The FI methods can be generally classified into four techniques as follows: hardware-based FI (implemented on the real system hardware), software-based FI (only the code execution on the system is modified), simulation-based FI (using computer simulation tools for circuit/system emulation and FI, see Fig. 30(a)) and emulation-based FI (faults are injected into a design implemented in a FPGA circuit).

For modeling and simulation of SEEs at system-level, simulation-based fault injection (SFI) is a non-intrusive approach that offers a maximum amount of observability and controllability. As illustrated in Fig. 31, SFI approaches can be based on analysis at different abstraction levels, thus enabling different SFI approaches [152].

The lowest level, at circuit simulation level, provides more accurate results but becomes impractical, for time-consuming and computational resource reasons, for evaluating a complete

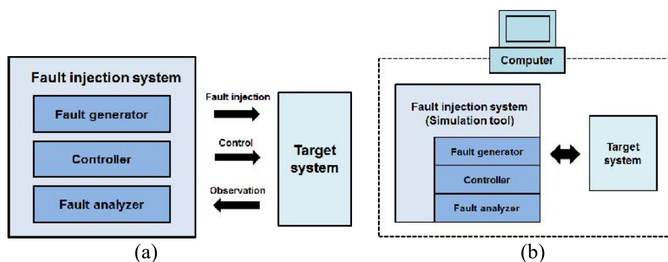


Fig. 30. (a) Fundamental environment of the Fault Injection method, and (b) Simulation-based Fault Injection. (After Jeong et al. [151], © EEI, 2016.)

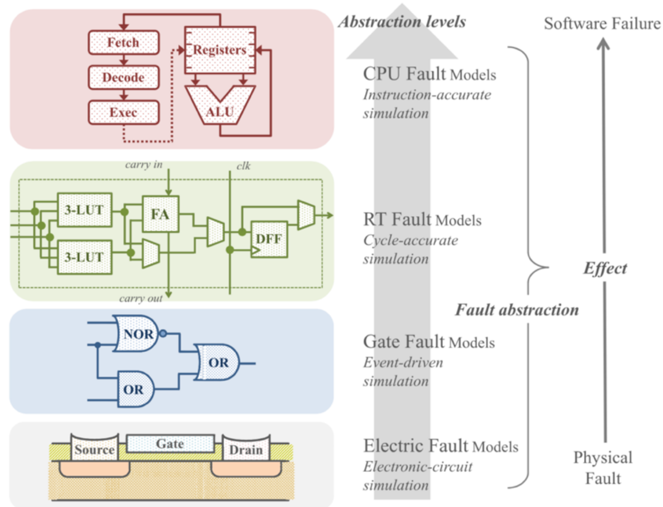


Fig. 31. CPU fault simulation taxonomy. Fault simulation at different abstraction levels is a trade-off between accuracy and simulation performance. (After Ferraretto and Pravadelli [152], © Springer, 2016.)

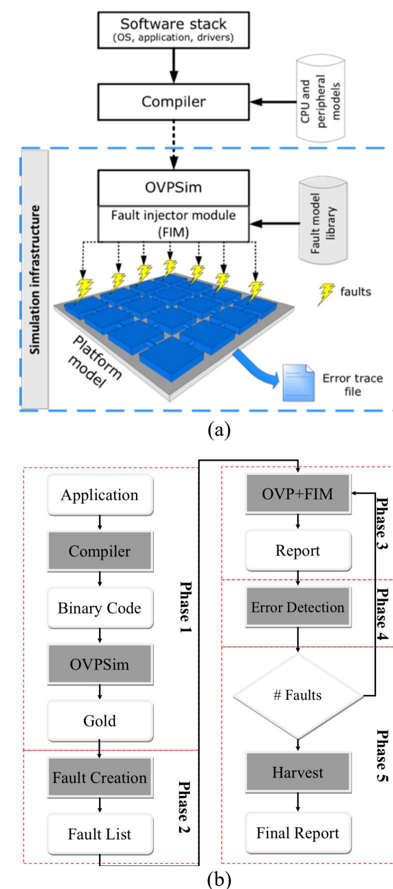


Fig. 32. (a) Proposed fault injection framework organization using OVPSim-FIM, and (b) five phases of proposed fault injection flow. (After Rosa et al. [155], © IEEE, 2015.)

CPU and a software stack on top of it, for example [152]. Event-driven (gate-level modeling using HDL at register transfer level – RTL) simulations are also usually far from being acceptable to simulate a complete CPU. At this other extremity of the system simulation chain, the fastest solutions are represented by purely functional simulators that can almost reach the speed of the simulated hardware. However, simulating low-level faults could be very misleading when the simulation is only functional [152]. A very interesting trade-off between accuracy and simulation performance is provided by SFI solutions based on instruction-accurate virtual platforms. They are also increasingly adopted for exploring and anticipating before hardware implementation how a system responds to faulty conditions. A virtual platform (VP) is a full-system simulator that emulates hardware components (e.g., CPUs, memories), and the execution of real software stacks, on the same machine, as it is running on real physical hardware [153]. Instruction-accurate virtual platforms, such as QEMU [152,154] or OVPSim [68,153,155,156], are based on a dynamic binary translation engine, which enables simulation running real applications at the speed of hundreds of millions of instructions per second (MIPS). These VPs offer a large collection of component models, including processor architectures, peripherals, and memory models. They also facilitate fault injection implementation and fault analysis due to their design flexibility and debugging capabilities [152].

In the study reported in [153,155] by Rosa et al., soft errors were modeled as data errors under the form of single-bit, multiple-bit or event upsets that are generated randomly in registers or memory addresses during the execution of a given software application. To configure, monitor and detect errors during system simulation, a fault injection module (FIM) has been developed in the framework of OVPSim, as illustrated in Fig. 32(a). This module is used to select, from a fault model library (FML), the most appropriate fault injection (FI) model for each set of platform components (e.g., processors, busses, routers, or memory types) [153]. The FIM is also responsible for monitoring the target processor, accessing resources as memories and registers, injecting the faults, capturing unexpected events arising from the simulator, extracting information, and analyzing errors [155].

A typical fault injection flow comprises five phases, as shown in Fig. 32(b) (a complete description of this flow can be found in [155,156]). Briefly, in phase 1, the simulation infrastructure cross-compiles the application source and simulates it on the virtual platform to verify its correctness. It also extracts information using a gold standard, which is required for fault creation [153]. Phase 2 creates register or memory fault patterns consisting of injection time, a target, and a fault mask (i.e., the target bit). Single bit-flip locations in internal components (e.g., registers, memory address) as well as injection times are defined randomly. In phase 3, fault injection is performed. The FIM starts by reading the fault list

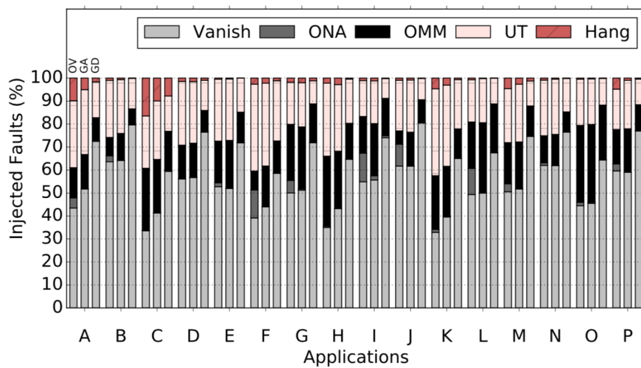


Fig. 33. Benchmarking of 8000-fault injection campaigns for a multicore ARM Cortex-A9 processor performed on three different SFI setups: OVPsim-FIM (OV), gem5-FIM atomic (GA) and gem5-FIM detailed (GD). (After F. Rosa [156].)

and then schedules an event targeting insertion time. After writing the new value in the target register, the simulation restarts. During phase 4, error detection is performed by comparing each application running under fault injection with the golden standard run.

At this level, different error classifications can be implemented, for example the five groups error classification proposed by Cho and discussed in [155]: (i) vanished, no fault traces are left; (ii) application output not affected (ONA), the resulting memory is not modified, however, one or more remaining bits of the architectural state are incorrect; (iii) application output mismatch (OMM), the application terminates without any error indication (however, the resulting memory is affected); (iv) unexpected termination (UT), the application terminates abnormally with an error indication; (v) hang, the application does not finish, and it is preempted using a timeout. Lastly, phase 5 assembles all FIM individual reports to create the final database, final report, and graphics. An example of compilation results comparing different SFI solutions is shown in Fig. 33 [156].

Among all the errors induced by fault injection, single-event functional interrupts at the system level (systems-on-chips - SoC) are undoubtedly the most difficult to characterize and to model because: i) these errors can have multiple causes and ii) during SEFIs the system can behave unpredictably [157]. Usually, SEFIs appear as a spontaneous system reset, a program execution stop (hang-up) or an upset in program execution that can be only repaired by external reset [158]. It is known that SEFIs are caused by upsets in program or data memory (critical bits) or transients and interference on internal lines or peripherical circuitry [158]. Recent studies have also shown that increasing complexity and size of program code, as well as real-time operating system usage, leads to a higher probability of SEFIs that directly affects the reliability of a modern SoCs [159].

VIII. Summary and Conclusion

Single event effects designate and include a sequence of events that extends from particle-matter interactions at the atomic scale to functional errors at circuit or system-levels. As a complex domino effect, they cover approximately 15 orders of magnitudes on the distance scale and 20 orders of magnitude on the time scale, which is considerable and necessarily involves several branches of fundamental and applied physics for their description and understanding. In this review, we have addressed the different ways of modeling and simulating this complex chain of mechanisms, discussing the specific multi-scale, multi-physics and multi-domain nature of SEEs as well as the main underlying physical mechanisms that lead to the occurrence of such effects in device, circuit and systems. However, this review has not covered the vast and exhaustive domain of all types of SEEs, but was limited to the modelling and simulation of SETs and SEUs induced by single events in digital electronics.

An important feature of single-event effects is that they can be studied at different levels, starting from different "precursors": the interaction of a particle with the atoms of a material for the most microscopic description, the creation of electron-hole pairs at device level, the injection of a current pulse at circuit level, and finally the injection of faults at system level. These different description levels correspond to diverse specialized branches in the radiation effect community historically developing different modeling approaches, using specific simulation tools, and even using different technical terms to designate the same effect (a single-bit upset at memory cell level becomes, for example, a logical fault at system-level).

In this survey, we distinguished five different types of methodologies of modeling and simulation of SEEs as a function of the "simulation level" envisaged to perform a given study. These simulation levels schematically extend from atoms to materials, materials to devices, devices to cells, cells to circuits and circuits to systems. For each level, we reviewed and emphasized the specific features of the modeling and simulation methodologies, and we discussed simulation requirements, codes, model inputs and expected outputs.

To go further and with the uninterrupted miniaturization of silicon microelectronics that has fueled the exponential growth of integrated circuits for over half a century, some important challenges remain in the domain of modeling and simulation of SEEs in future nano-devices and related circuits. These challenges will concern the adaptation of the whole panoply of existing methods to new materials, specific architectures, and new domains, including photonic devices, spintronic circuits and quantum computing related circuits and systems, just to cite the most important.

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