Workload Impact on BTI HCI Induced Aging of Digital Circuits: A System level Analysis

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***Abstract*— Workload characterization of digital circuits using industry standard benchmarks gives an insight into the performance and energy characteristics of processor designs. Aging studies of digital circuits due to BTI, HCI is gaining importance since a higher impact on the performance of circuits can be observed as we scale down gate dimensions. For embedded system applications, the workload may very well dictate the lifetime of a system. This article aims to study the influence of different workloads on the degradation of critical path which determines the reliability of a system. A top-down circuit activity and probability analysis is carried out leading to an accurate estimation of aging due to HCI and BTI of critical path elements at the design stage. A dedicated simulation flow has been set up, from RTL simulation down to gate level cell timing analysis mapped onto 28nm FDSOI technology from STMicroelectronics. The objective is to correlate path delay timing with aging of critical path cells. Simulation results indicate that the higher complexity of an execution program may not necessarily lead to a higher rate of degradation of the critical path considering that aging is primarily driven by the workload dependent activity and the probability of critical path combinational logic elements.**

Keywords*— *Workload, Aging, Critical Path, Reliability

I. INTRODUCTION

Computers were designed to perform tasks faster. Speed of operation of microprocessors, power consumption, processor micro-architecture, memory hierarchy, system architecture [6] and task scheduling of application specific software that drive the microprocessors without a comprehensive knowledge of the end user specific requirements has been till the now the major concern for microprocessor and microcontroller designers [8]. It is to simulate these wide range of possible applications of an end user that benchmarks and their associated performance metrics that benchmarks have been developed [10]. Benchmarks are designed to represent emerging workloads. EEMBC (Embedded Microprocessor Benchmark Consortium) deal with benchmarks for embedded systems [11]. Benchmarks scores gives a relative measure of performance of different processors. Using these different benchmarks for system or hardware performance analysis gives information to the designers as to whether design changes need to be made depending on the workload that it will employ for a certain application [9]. Though workload characterization till now has just been used for micro-architecture analysis, for our current aging analysis studies, *the same workloads are considered to influence the aging of the microcontroller circuit* under study in different respective fashions. As observed from our simulations and references [11], [8] considerable variation can be observed between the simulation times of different applications. Number of cycles of certain application to be employed by the end user will then definitely influence the life time of the circuit. The automotive sector is one of the markets of interest for St Microelectronics. Matrix multiplication, FIR filters benchmarks [11] are used to characterize Embedded System Applications for the Automotive sector.

Silicon on Insulator (SOI) technology involves the fabrication of a sandwich structure, where a 25nm Buried oxide layer is sandwiched between a thin undoped silicon layer and the substrate. This undoped layer is an important device matching characteristic [13]. The final SOI thickness of 7nm provides an excellent Short Channel effect (SCE) control without any change in the leakage current for gate size up to 24 nm. FDSOI technology is aimed at high speed, low voltage circuit applications providing a 32% and 84% speed increase for 1V and 0.6V respectively with very little modification to the prevalent fabrication flow at ST Microelectronics [12]. Incidentally, manufacturing process gets simplified because of elimination of well and field implantation steps. Memory access times, can be significantly reduced due to high Iread values for manageable leakage. HCI and BTI effects observed are comparable to the libraries based on Bulk Technology.

This paper makes a direct link between workload at system level and the device level degradations due to HCI and BTI. Considerable amount of research into how HCI and BTI affect the aging of transistors has been done [14] [15]. Both HCI and BTI result in an increase in the threshold voltage [4] thus resulting in slower transistors. HCI degradation is observed predominantly while switching the transistors at high frequency while a transistor at a constant potential degrade gradually due to BTI. Efforts have already been made to consider HCI and BTI effects in the design process [16]. Research into how workload can accelerate the aging has been explored by [2], [4]. This paper investigates an industrial design flow to identify critical paths and critical path elements

of a design that are most susceptible to HCI and BTI corresponding to a certain workload.

II. Design and Flow Methodology

A. openMSP430 Architecture

The design under use is an open-source synthesizable 16 bit microcontroller core from TI MSP430 family based on Von Neumann architecture and written in Verilog HDL. The modules Frontend Unit, Execution unit, Memory backbone in Fig 1 were observed to show the maximum activity based on RTL simulations and so they are the modules that are of interest in relation to this paper. The openMSP430 was further synthesized onto 28nmFDSOI technology.

B. Workload dependent Aging analysis Flow

Activity is defined as the average number of transitions of a net per clock period for the entire simulation cycle. Activity for this paper refers to transition density as mentioned in [20]. Probability in this research paper refers to the probability of observing a logic 1 at a particular net per clock cycle. Thus probability for this paper stands for signal probability of being either a 1 or 0. Signal probability of 1 means the signal is always at 1 and vice versa.

Activity and probability information for all nets in the design corresponding to 10 different Benchmark programs for a full simulation run is obtained.

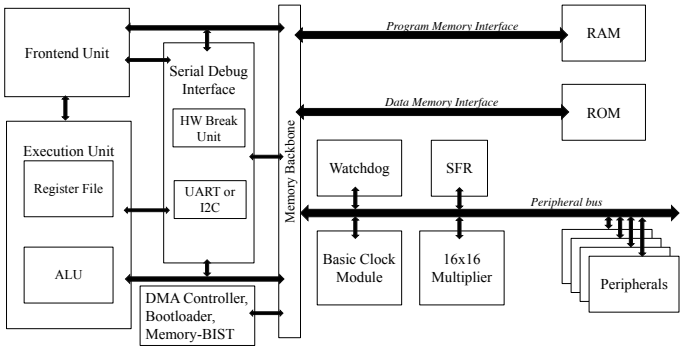

Fig. 1. openMSP430 Design Structure

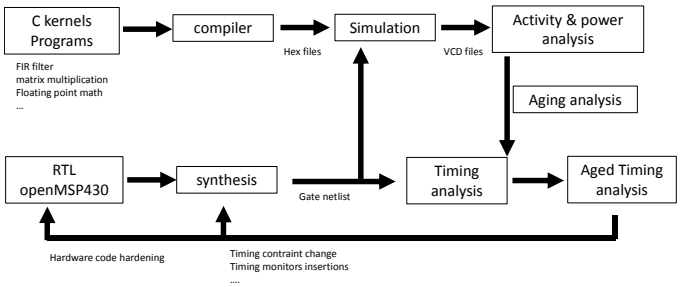

Fig. 2. Workload dependent Aging analysis Flow

III. Hierarchical Approach

A. Path Level Analysis

The activity value varies as we move through the elements along a certain critical path. The activity value of a net depends on the cell elements connected to it and the workload. Activity of the endpoint nets of all chosen critical paths is obtained. These activity values are plotted against their respective path delay values. Aging of critical paths which form 10% of maximum delay has also been referred to as PCP (Potential Critical Paths) [1]. Activity of endpoints here is considered as the activity of the critical paths which provides a means to compare path aging due to HCI and BTI.

The critical paths with highest activity have been highlighted in the graph Fig. 3 (bottom). The cell from which the net originates is expected to see maximum HCI related

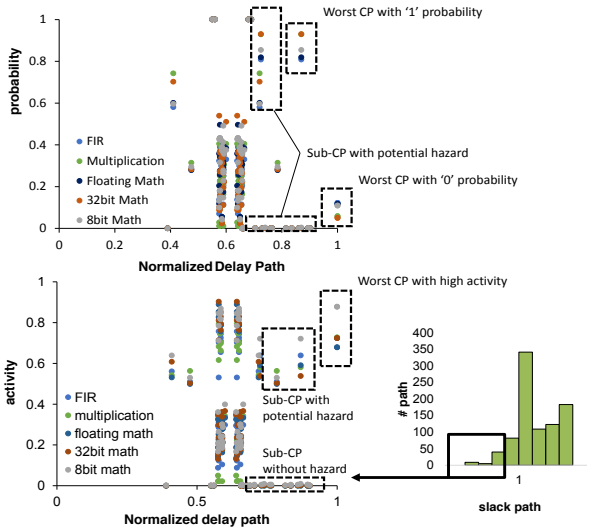

Fig. 3. Path level activity and probability plots

degradation. The nets without activity will have a logic level of 1 or 0 associated with it and this is an indicator of possible worst case degradation due to BTI as in Fig. 3 (top)

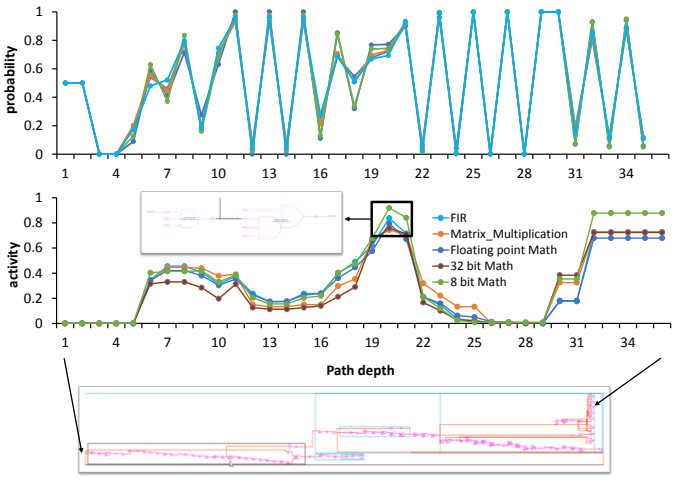

Fig. 4. Critical Path Cell level activity and probability plots

B. Cell Level Analysis

The cell level analysis of the critical path provides complete data on how the individual elements in the critical path ages. In Fig. 4 (bottom), the cells most affected by HCI is identified. In Fig.4 (top), for a different workloads, probability of the nets along the Critical Path being either 1 or 0 provides information on BTI degradation.

A complex workload can be referred to as the workloads that lead to high activity nodes. More the number of such high activity nodes, higher is the complexity of the workload. Higher complexity of the workload does not necessarily lead to a higher activity of all the critical paths but it has an impact on certain potential critical paths [2].

C. Timing Arc degradation

The impact of activity and probability are now reviewed at cell level. Design in Reliability models [17] [18], are models of HCI and NBTI degradation of cells. Using Design in Reliability models, it is possible to evaluate the degradation of cell for a given stimuli and mission profile. Assuming 2 years of operating conditions at Vmax, the degradation of a NAND3A is depicted in Fig 5. At a given input slope and load, delay of rising and falling arcs are simulated. It is noticeable that degradation is a function of both the activity and probability driven respectively by HCI and BTI mechanisms. However, there is coupling between both these mechanisms, as explained in [3]. These effects are not additive but they do interact with each other. For this particular arc, an always '0' at input leads to drastic cell degradation because of PMOS degradation. This gets exacerbated at high activity.

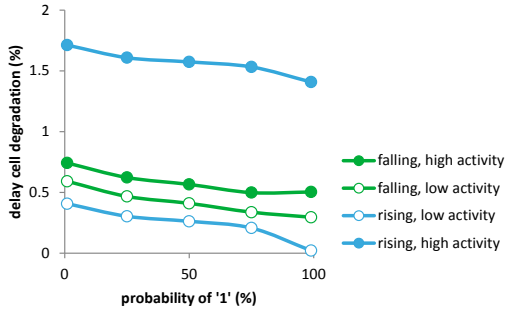

Fig. 5. Timing arcs degradation for NAND3A cell for different probability and activity

CONCLUSION

This paper discusses a flow that provides workload dependent HCI and BTI related degradation information to the designer at the very beginning of the design stage. Workload dependent activity and probability information of the critical path nets of a digital circuit is gathered. Higher the activity and probability on a certain net, higher will be degradation due to HCI and BTI respectively of cells from which the nets originate. A designer can thus improve the reliability of a hardware, by taking into account the HCI and BTI aging for a certain application during the design stage.

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