NBTI Lifetime Evaluation and Extension in Instruction Caches

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***Abstract*—CMOS devices suffer from wearout mechanisms resulting in reliability issues. Negative bias temperature instability (NBTI) is one of the dominant ageing effects that can cause threshold voltage shift on PMOS devices and subsequently impact circuit performance. The static noise margin (SNM) of an SRAM cell may be sharply reduced with unbalanced NBTI stress. This will impact SRAM read stability. From our observations of instruction caches, NBTI stress duty cycles for each cache line generally have similar but unbalanced patterns even when running very different programs. Based on the patterns, we propose an algorithm to evaluate the lifetime of instruction caches by running SPICE simulation. The results predict 6 and 7 years NBTI lifetimes of instruction caches for ARM and MIPS architectures respectively. One of the practical solutions is periodically flipping each cell to balance the degradation rate. However the performance benefits in terms of lifetime are not actually proven before. Using the stress patterns and lifetime evaluation algorithm, our work for the first time prove this technique can extend the lifetime of the cache by two orders of magnitude.**

I. Introduction

As transistor dimensions continue to shrink, reliability is one of the most significant remaining concerns for CMOS technology [1]. Negative bias temperature instability (NBTI) is one of the dominant ageing mechanisms, in which the threshold voltage (V_{th}) of a PMOS transistor [2]–[4] increases over time.

The NBTI effect on CMOS memory devices such as SRAM cache has received much attention [5]–[7]. NBTI leads to degradation of the SRAM static noise margin (SNM) due to time-dependent mismatches [8], [9]. One of the practical solutions is periodically flipping each cell to balance the degradation rate [7], [10]. However, since the storage value is considered unpredictable in these works, the performance benefits of this technique are not actually proven.

Our work presents a method to evaluate NBTI lifetime in instruction caches. The contributions are as follows: 1) a novel analysis of the instruction cache that shows the NBTI stress duty cycles for each cache line generally have similar patterns even when running very different programs; 2) an algorithm of running SPICE simulation to predict the NBTI lifetime for the instruction cache based on this observation; 3) lifetime extension of cell flipping in instruction caches is proven by using the stress patterns and lifetime evaluation algorithm.

This paper is organized as follows. Section II presents the theory and simulation results of NBTI on both a single transistor and an SRAM cell. In Section III, we demonstrate that the pattern of NBTI stress locality does not vary much between different programs and from this cell lifetimes are calculated. The lifetime evaluation algorithm and the simulation results for instruction caches in ARM and MIPS architectures are presented in Section IV, while Section V describes the lifetime extension by cell flipping. Finally, the paper is concluded in Section VI.

II. NBTI Effect and SRAM Cell Degradation

A. Impact of NBTI on Single PMOS Transistor

NBTI can result in an increased V_{th} over time. A PMOS transistor can be switched between the NBTI stress phase and the recovery phase. Si-H bonds are disassociated under negative bias condition ($V_{gs} = -V_{DD}$) and hydrogen spaces and traps are produced at the oxide interface. These hydrogen spaces then diffuse away. Once the stress is removed ($V_{gs} = 0$), some bonds recover because of recombination with hydrogen. Some traps still remain and therefore the recovery is partial.

Thus, the V_{th} shift is proportional to the density of traps at the oxide interface [4], [11]. The traps are produced during the stress phase and some will be neutralized in the recovery phase. Therefore, V_{th} degradation is highly dependent on the stress duty cycle, which is the probability of a logic zero at the gate of a PMOS transistor in a digital circuit.

In [12], the authors propose a long-term NBTI model to quantify V_{th} degradation after a given operation time t:

$$\Delta V_{th}(t) = \left(\frac{\sqrt{K_v^2 \alpha T_{clk}}}{1 - \beta_t^{1/2n}} \right)^{2n} \quad (1)$$

$$where$$

$$\beta_t = \left(1 - \frac{2\xi_1 t_e + \sqrt{\xi_2 C (1-\alpha) T_{clk}}}{2t_{ox} + \sqrt{Ct}} \right)$$

where α is the key parameter – the stress duty cycle. K_v is a function of supply voltage, temperature and technology while T_{clk} is the equivalent stress-recovery period. n is either 1/4 or 1/6 depending on the diffusion spaces (H or H_2). C is the diffusion speed in the gate material. ξ_1 and ξ_2 represent the annealing probabilities in the oxide and the gate respectively. Finally, t_e is the effective oxide thickness indicating the diffusion distance in the oxide and is less than or equal to the oxide thickness, t_{ox}.

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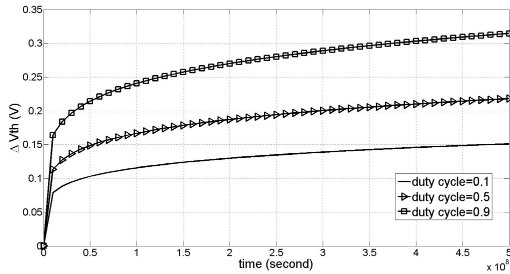

Fig. 1. NBTI simulations on PMOS transistor for different duty cycles (T=300K, Vdd=1.2V, Vtp=-0.276V)

Based on the long-term NBTI model, above, and data from [12], V_{th} shifts are simulated using MATLAB as in Figure 1. The technology parameters are from the Synopsys 90-nm SPICE model. 90-nm technology is, truly, outdated. However, according to the NBTI models proposed already [2], [3], we believe the trends also apply to smaller technologies.

B. Impact of NBTI on 6-T SRAM Cell

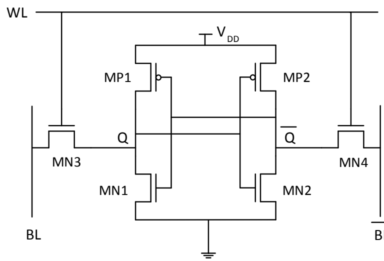

Fig. 2. Six transistors SRAM cell circuit

Figure 2 shows a basic 6-T SRAM cell, in which only the pull-up transistors, MP1 and MP2, would suffer from NBTI [8]. Since MP1 and MP2 are part of cross coupled inverters, only one would be under NBTI stress at any time. This might result in unbalanced V_{th} degradations of these two transistors and thereby lead to a mismatch.

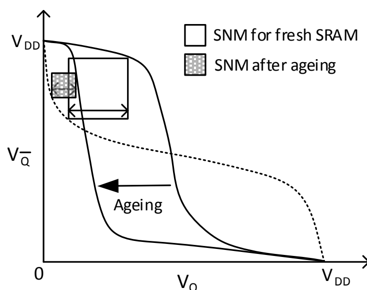

Fig. 3. SRAM cell SNM degradation

The static noise margin (SNM) is the biggest noise voltage the SRAM cell can tolerate. V_{th} mismatch on an SRAM cell can result in an asymmetric transfer characteristic and thereby reduce the SNM, Figure 3.

Using the long-term NBTI model in Equation (1) to modify the SPICE model, the degradation in the SRAM cell can be simulated, Figure 4. A cell with 50% stress duty cycle ages most slowly because MP1 and MP2 are matched. Uneven stress accelerates ageing.

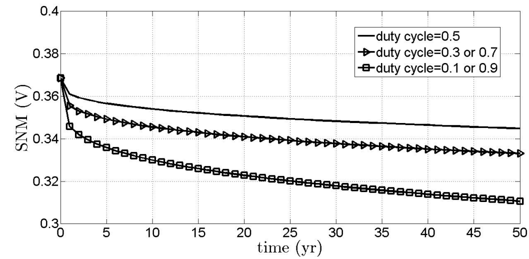

Fig. 4. SNM degradation simulations for different duty cycles (T=300K, Vdd=1.2V, Vtp=-0.276V)

III. Stress Locality of Instruction Cache

The observation is noticed that the data stored in a cache shows very similar patterns when executing different benchmark programs. We ran a test on the instruction caches of ARM and MIPS architectures, using GEM5. 16 benchmark programs, all with more than ten thousand instructions, were chosen. The signal probability of each bit of each cache word is shown in Figure 5. It can be seen that some bits preserve the same values in most locations, consequently leading to NBTI stress locality.

This phenomenon can be explained as following. For any program, we can expect some types of instruction to be used more frequently than the others. Take the ARM processor results in Figure 5a as an example. The most significant four bits are the condition field and ”1110” is used for unconditional instructions. The number of unconditional instructions is much bigger than that of conditional ones in any program. As a result, the most significant four bits have a high probability of being ”1110” as seen in Figure 5a.

If the SNM degrades to a value smaller than expected noise, the storage data might be flipped, which causes a failure when the data is read out. This gives the NBTI lifetime of the instruction cache. 50% signal probability will give the longest lifetime because both inverters in the SRAM cell age at the same rate and so are not mismatched. The bit with the probability furthest from 50% would fail first, which determines the lifetime of the whole SRAM array.

IV. NBTI Lifetime Evaluation of Instruction Cache

According to the stress locality in last section, NBTI lifetime of a instruction cache is predictable. We propose Algorithm1 to evaluate the lifetime. This algorithm uses Monte

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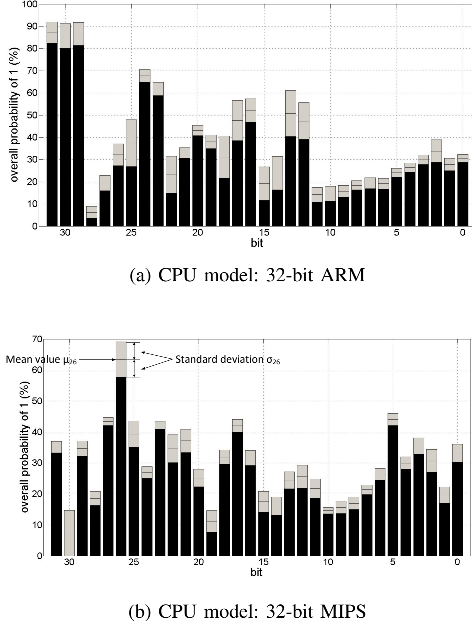


(a) CPU model: 32-bit ARM

(b) CPU model: 32-bit MIPS

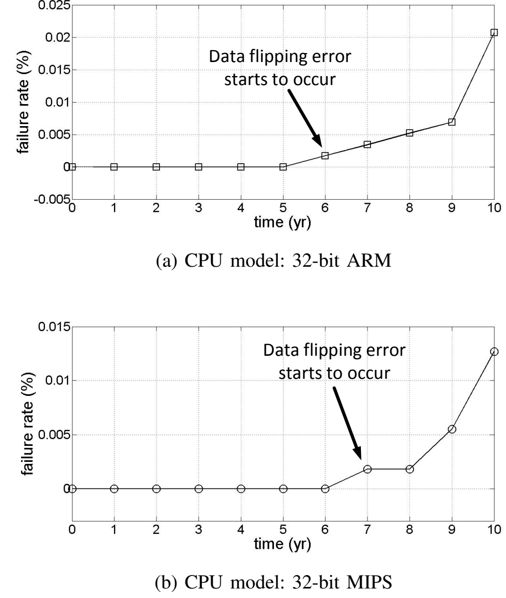
Fig. 5. Probability mean values and standard deviations of one cache word in instruction cache when running 16 benchmark programs

Carlo simulations to detect the moment when stored data is corrupted and also calculates the flipped bit rate over the whole instruction cache.

Algorithm 1 SRAM cache lifetime evaluation

1: **procedure** LIFEEVA
2: $i \leftarrow 0$ ▷ i indicates current bit location
3: $j \leftarrow 1$ ▷ j indicates current iteration times
4: $t \leftarrow 0$ ▷ t indicates current year
5: *Monte Carlo*:
6: $\alpha_1 \sim N(\mu_i, \sigma_i^2)$ ▷ Normal distribution
7: $\alpha_2 \leftarrow 1 - \alpha_1$
8: $\Delta V_{th1} \leftarrow F_{NBTI}(\alpha_1, t)$ ▷ Implement NBTI model
9: $\Delta V_{th2} \leftarrow F_{NBTI}(\alpha_2, t)$
10: $run\ SPICE\ simulation$
11: **if** $Data\ flipping\ error\ occurs$ **then**
12: $lifetime \leftarrow t$
13: **else if** $j < total\ iteration\ times$ **then**
14: $j \leftarrow j + 1$
15: **else if** $i < instruction\ length - 1$ **then**
16: $i \leftarrow i + 1$
17: **else**
18: $t \leftarrow t + 1$
19: $update\ flipped\ bit\ rate$
20: **goto** *Monte Carlo*

To model typical operation, the storage value in each cell is set to both 1 and 0 but with different probabilities: we assume NBTI stress duty cycles are distributed with normal distributions with the means and standard deviations shown in Figure 5. For each bit, we run 1600 simulations to guarantee a 95% confidence level within 1% probability error. The simulation results predict 6 and 7 years NBTI lifetimes for ARM and MIPS architectures respectively, at which point, the stored values in some SRAM cells start to be corrupted, Figure 6.



(a) CPU model: 32-bit ARM

(b) CPU model: 32-bit MIPS

Fig. 6. SRAM cache NBTI lifetimes and failure rates simulations based on Algorithm 1 (T=300K, Vdd=1.2V, Vnoise=+/-0.32V)

V. LIFETIME EXTENSION BY PERIODIC CELL FLIPPING

The motivation for previous cell flipping work, [7], [10], is to avoid a cell holding the same value for a long time. However, since the storage value is considered unpredictable in that work, the performance benefits of periodical cell flipping are not actually proven. On the other hand, in our work, we note that the NBTI stress in the instruction cache stays constant over time.

Figure 7 shows the new probability mean values and standard deviations if cell flipping is applied. By definition, the mean values of the probabilities are at 50%. From this, the new predicted lifetimes can be calculated, as shown in Figure 8. As can be seen, for the same operating conditions, data failures start to occur after more than 300 years in both ARM and MIPS processors. While the exact figure is, of course, dependent on the modelling, it is unarguable that a significant extension to the lifetime of an SRAM instruction cache is achievable by simply flipping cell values periodically.

VI. CONCLUSION

Rapid shrinkage of CMOS transistors has led to concerns about reliability risks such as ageing. The effect of NBTI on the Static Noise Margin of SRAM-based instruction cache is discussed in this paper. NBTI directly affects the

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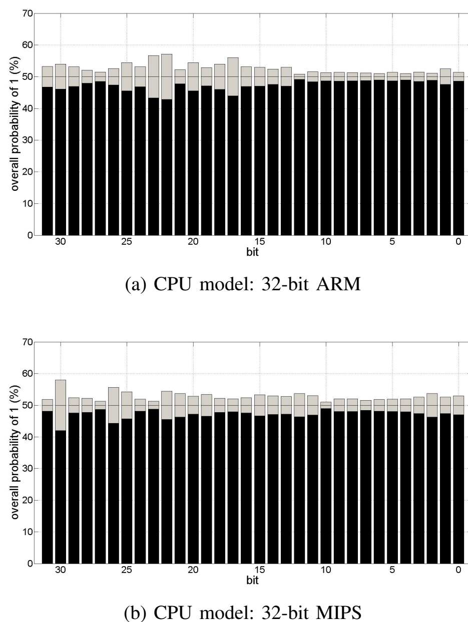
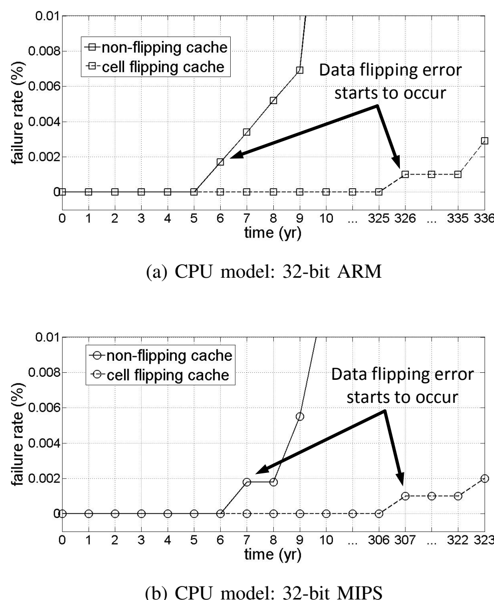


(a) CPU model: 32-bit ARM

(b) CPU model: 32-bit MIPS

Fig. 7. Probability mean values and standard deviations of cell flipping instruction cache



(a) CPU model: 32-bit ARM

(b) CPU model: 32-bit MIPS

Fig. 8. NBTI lifetimes and failure rates simulations for both non-flipping cache and cell flipping one (T=300K, Vdd=1.2V, Vnoise=+/-0.32V)

threshold voltage of PMOS devices and thereby impacts on the performance. In an SRAM cell, an unbalanced NBTI stress duty cycle can reduce the SNM and affect the read stability. From our observations, the NBTI stress duty cycles for an instruction cache generally has similar patterns even running very different programs. Therefore the NBTI lifetime is predictable, and our results suggest 6 or 7 year lifetimes for instruction caches in ARM and MIPS processors by using the proposed lifetime evaluation method. Additionally, the benefit of lifetime extension by periodically flipping each SRAM cell is presented using our proposed stress patterns and lifetime evaluation algorithm. It has been shown the instruction cache lifetimes can be extended by two orders of magnitude by this technique.

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