

Ageing Impact on a High Speed Voltage Comparator with Hysteresis

Illani Mohd Nawi, Basel Halak and Mark Zwolinski

Electronics and Computer Science, University of Southampton
Southampton, SO17 1BJ, U.K

Email: {ibmnlg12,bh9,mz}@ecs.soton.ac.uk

Telephone: +44 (0) 8059 3081

Abstract—The impact of ageing on a high speed comparator with hysteresis in 65-nm CMOS technology using SPICE simulations is investigated. The comparator has been designed to offer immunity to single event transients. The most sensitive transistor was subjected to single events at manufacture time and after ageing, assuming a maximum parameter drift of 10% on all PMOS transistors for 10 years. It was found that NBTI does not significantly affect the single event transient vulnerability of the comparator, at different hysteresis voltages.

Keywords: Single event transients, NBTI, comparator-with-hysteresis, Schmitt trigger, synergism

I. INTRODUCTION

CMOS scaling has been proven to improve a system's performance, however this has led to increased vulnerability to soft errors, particularly single event transients (SETs) as reported by [1], [2], [3] for digital circuits and [4] for analogue circuits. Although a single event transient caused temporary variations to devices, a single glitch could have a major effect on safety critical applications, such as automotive, aerospace and aeronautical applications.

In addition to the increased vulnerability to SETs, the aggressive scaling of CMOS devices has also increased vulnerability to ageing, as reported by [5], [6], [7], [8], [9], [10]. [5] and [6] reported the impact of ageing on digital circuits while [7], [8], [9], [10] focused on the impact of ageing on analogue circuits.

While SETs and NBTI were individually investigated for their impact on CMOS devices, limited work has been done on the interaction between ageing and SETs [11]. Rossi et al., [12], reported that NBTI would reduce the critical charges on the nodes of combinational and sequential circuits while Harada et al., [13], reported that ageing has a significant impact on the effect of SETs and Bagatin et al., [6], stated that NBTI degradation does not significantly affected the single event upset sensitivity of SRAM as long as the parametric drift caused by ageing does not exceed 10%. Additionally, El Moukhtari et al., [14], has indicated a decrease in SET sensitivity under the influence of NBTI for chain of inverters and the same authors, [15], reported a fast increase of SRAM SET vulnerability under ageing.

This paper is structured as follows. Section II outlines the aim of this work while Section III describes the implementation of the comparator with hysteresis. Section IV summarizes the single event transient model used and the

sensitivity analysis significant results. Section V reported the NBTI analysis setup and the summary of impact of NBTI on the SETs for a range of hysteresis voltage and 2 different input frequencies. Finally, Section VI concludes our investigations.

II. AIMS

This work investigated the impact of NBTI on the SET vulnerability of analogue circuits, in particular comparators. As mentioned in our earlier work, [4], SETs in comparators with no memory (feedback), are not problematic as they will be propagated to digital circuitry and corrected at that stage. However, an SET will likely cause a problem in a system with memory, particularly a comparator with hysteresis, such as a Schmitt-Trigger. Schmitt triggers are generally used to increase the noise immunity of a particular device in an open-loop topology or used as bi-stable regulators and generators in a closed-loop topology, and are widely used in aerospace applications.

In our previous work, [4], we noted that a high input hysteresis voltage gives better noise immunity, but tends to "trap" an SET. On the other hand, a low input hysteresis voltage causes any SET to propagate, but reduces the input noise immunity. There is, therefore a possible compromise between these two aims. Our aim in this work is to determine whether these two design aims, and any compromise between them, are affected by NBTI-induced ageing.

To the best of our knowledge, there is no work which studied the relationship between impact of NBTI and the SETs vulnerability in a comparator-with-hysteresis.

III. HIGH-SPEED COMPARATOR IMPLEMENTATIONS

Our comparator is based on a high speed comparator, [17], as shown in Fig. 1. This comparator has been implemented previously in 120-nm technology and is able to work at up to 20 MHz operating frequency [4]. We have improved our previously implemented comparator, [4], to work at higher frequencies, as we have found out that SETs introduced into the previously designed comparator, which last less than 1 clock cycle, will be propagated to the digital circuit and corrected there. This particularly applies to input frequencies of less than 180 kHz. The same comparator has also been used to study the interactions of various other factors on the vulnerability of SETs, at higher frequencies.

In order to improve the operating frequency of the previously designed comparator, we have added a three-stage

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pre-amplifier by Lin et al., [18], as illustrated in Fig. 2. The overall block diagram of the comparator-with-hysteresis is illustrated in Fig. 3. On top of this, we have also transferred our design to 65-nm technology as opposed to 120-nm used in our earlier work. The comparator now would be able to operate up to 1 GHz input frequency.

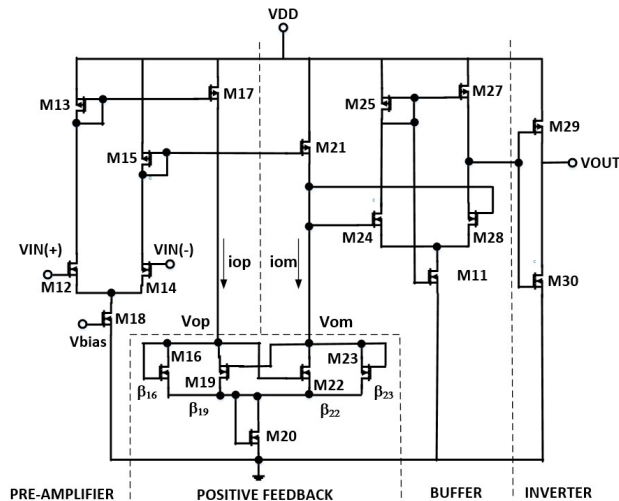


Fig. 1. 3-stage comparator diagram

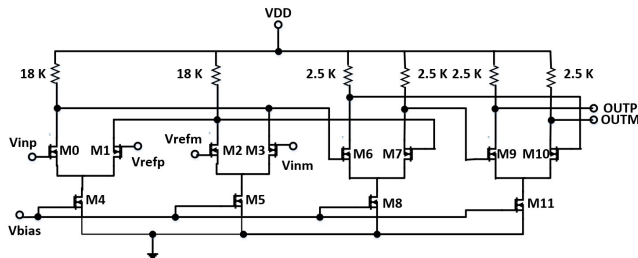


Fig. 2. 3-stage preamplifier

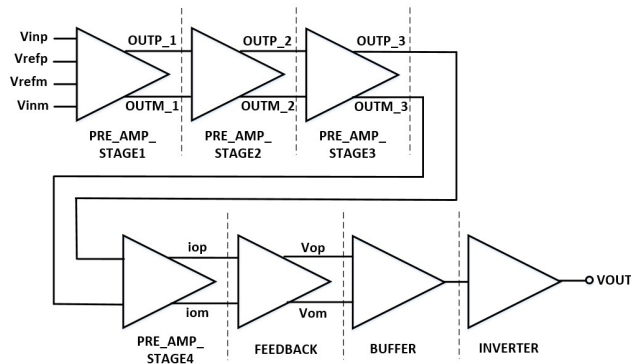


Fig. 3. Overall block diagram of comparator-with-hysteresis

IV. SET MODELING AND SENSITIVITY ANALYSIS

Zhao et al., [19] suggested that the single event upset (SEU) model, commonly used in analysis of soft errors in digital circuits, can be used in the measurement of SETs in comparators. As reported by [19], [20], single event transients

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in digital circuits are normally represented by either double exponential waveforms or a square pulse. Although both models exhibit approximately the same total charge, it has been reported by [21], [22], [23], that the double exponential pulse waveform has the most similarity to actual charge seen from heavy beam ion tests.

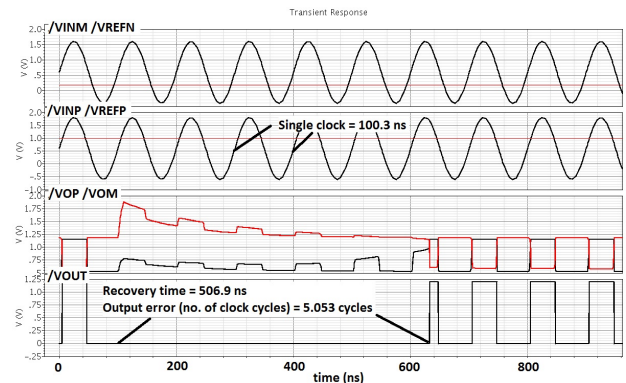


Fig. 4. Output error exhibited by transistor M21 for frequency of 10 MHz and differential input amplitude of 400 mV

TABLE I. RELEVANT EFFECTS OF ASET ANALYSIS

	Vhyst	8 mV
Pre-amplifiers	Recovery time (ns)	506.9
	Output error (cycles)	252.566
	Transistor	M21
Positive feedback	Recovery time (ns)	432.9
	Output error (cycles)	222.8024
	Transistor	M16
Most sensitive	Recovery time (ns)	391.1
	Output error (cycles)	196.3353
	Transistor	M24
Inverter	Recovery time (ns)	400.5
	Output error (cycles)	200.1499
	Transistor	M30
Pre-amplifiers	Recovery time (ns)	0
	Output error (cycles)	0
	Transistor	Various
Positive feedback	Recovery time (ns)	213.9
	Output error (cycles)	107.057
	Transistor	M23
Least sensitive	Recovery time (ns)	0
	Output error (cycles)	0
	Transistor	M26
Inverter	Recovery time (ns)	388.4
	Output error (cycles)	195.274
	Transistor	M29

Similar to our previous work, [4], we have injected SETs into each transistor of the comparator with a double exponential current pulse of 2 mA for 10 ns duration. This approach is based on work by Zhao [19] and [24]. Narasimham, [25], proposed different points of injection on PMOS and NMOS transistors, with the current source placed between VDD and the source for PMOS and between the drain and GND for NMOS transistors. Fig.4 illustrates the transient response of the implementation of our high-speed comparator-with-hysteresis, highlighting the output response and the intermediate voltages with an input frequency of 10 MHz and an input amplitude of 400 mV. The output error in Fig.4 reflects the SET suffered by the most sensitive transistor of the pre-amplifier, M21. The output error is reflected in the form of the number of clock cycles for which the comparator failed to sample a correct output value. The initial point of output error occurs from the point of SET injection and the

end point of the output error is when the output is returned to equilibrium, i.e. sampled a correct value. The errors are found by comparison with a radiation-free comparator. The most sensitive transistor is obtained from SPICE sensitivity analysis.

In our simulations studying the impact of variability on SETs and other factors on SETs, we have identified the most and least sensitivity transistors. This is to simplify our analysis and to focus more on the interactions between the factors rather than interactions within the circuit. Thus, similarly in this work, we have performed the sensitivity analysis and Table I summarizes the significant results for the comparator running at a selected hysteresis voltage of 8 mV for an input frequency of 500 MHz.

V. IMPACT OF NBTI ON SETS

The impact of NBTI on SETs on our comparator with hysteresis was analyzed using the MOSFET Model Reliability Analysis (MOSRA) Tool, which was made available with HSPICE. We used one of the available MOSFET levels provided, and so this is a qualitative study.

The model covers two-stages of simulation, which are the fresh simulation and post-stress simulation stage [26]. At time = 0 (fresh), the stress of selected MOS transistors is calculated based on the behaviour of the circuit and the HSPICE built-in stress model provided. Meanwhile, the degradation effect is simulated at the post-stress stage is based on the information provided from the fresh stage. The degradation effect in our study was set to the maximum parameter drift allowed, usually specified as a 10% decrement by foundries, [6]. Based on this information, 10% decrement means the saturation drain current of the aged PMOS transistor decreases by 10% when the PMOS is switched on for 10 years. It is assumed all PMOS transistors were under stress.

As in Section IV, the SET injection is modelled by a double exponential current pulse to the most sensitive transistor, M21. The analysis of the impact of NBTI on the SET vulnerability of the comparator was performed for a range of hysteresis voltages, from 0 to 64.4 mV. The differential input amplitude is set at 400 mV, with a voltage supply of 1.2V and reference voltage of 800 mV. From the analysis, we have observed that there is no significant impact of NBTI on the SET sensitivity of the comparator for the various hysteresis voltages, as shown in Figs. 5 and 6, which tabulates output errors for a range of hysteresis voltages for 100 MHz and 1 GHz, respectively. From both Figs. 5 and 6, a linear trendline proposes that output error increases gradually at a factor of less than 1 for increasing noise immunity required.

Our results may have been influenced by the selection of parameter drift of 10% for our model, which matches the conclusion by Bagatin, [6], stating that NBTI does not significantly affected the SETs as long as the parametric drift is within 10%. This particular study may only be applicable for devices within standard operating voltages, [6]. From the same analysis, we have also observed how the input voltage frequency impacted the severity of ASETs on the comparator-with-hysteresis.

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VI. CONCLUSIONS

The systematic approach of analysing the impact of NBTI on the SETs on comparator-with-hysteresis has concluded that NBTI has no significant impact on the SET sensitivity. From the same analysis, we have observed the dependence of the severity of SETs on input voltage frequency and hysteresis voltage, which we are currently analysing. As for the NBTI effects on our comparator, the findings would only match devices which are within the maximum parameter drift values. Hence, as part of future work, similar analysis shall be extended to be modelled to have parameter drift exceeding 10%, in order to have a better understanding of the relationship between NBTI and SETs. We aimed to come up with reliable correlations between hysteresis voltage and SET immunity under NBTI influence with extension of this initial work.

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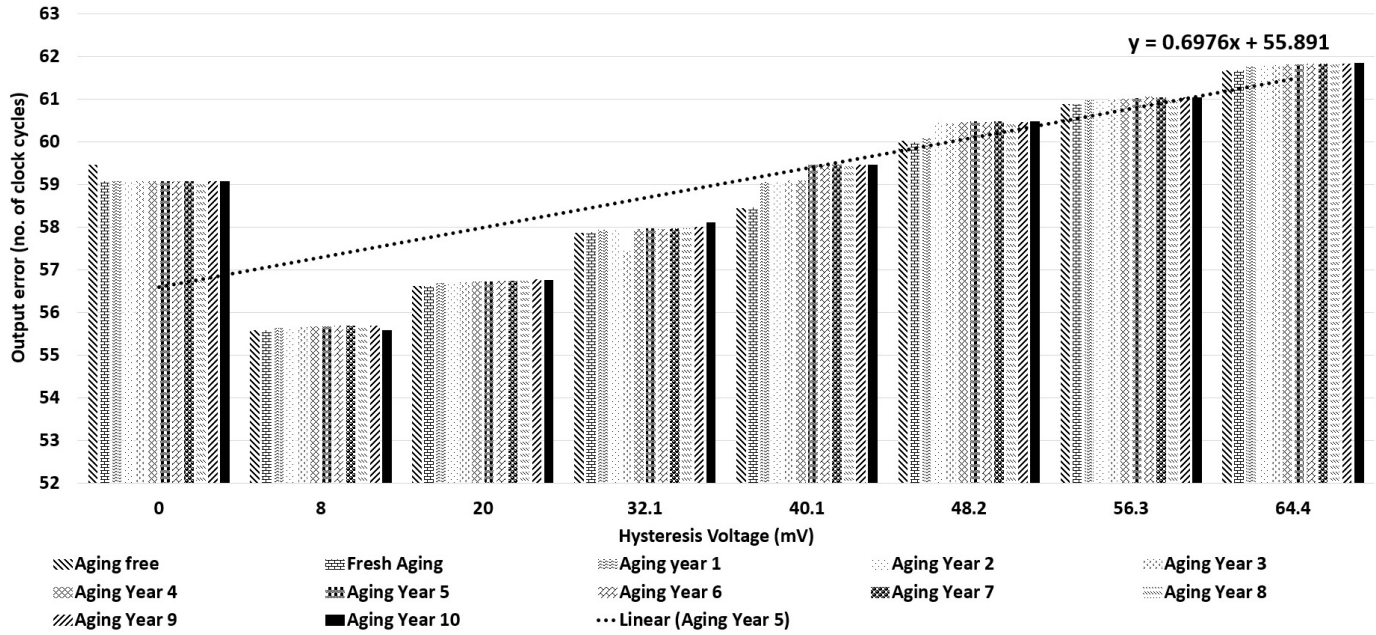


Fig. 5. Output error versus hysteresis voltage under aging impact, including aging-free for freq = 100 MHz

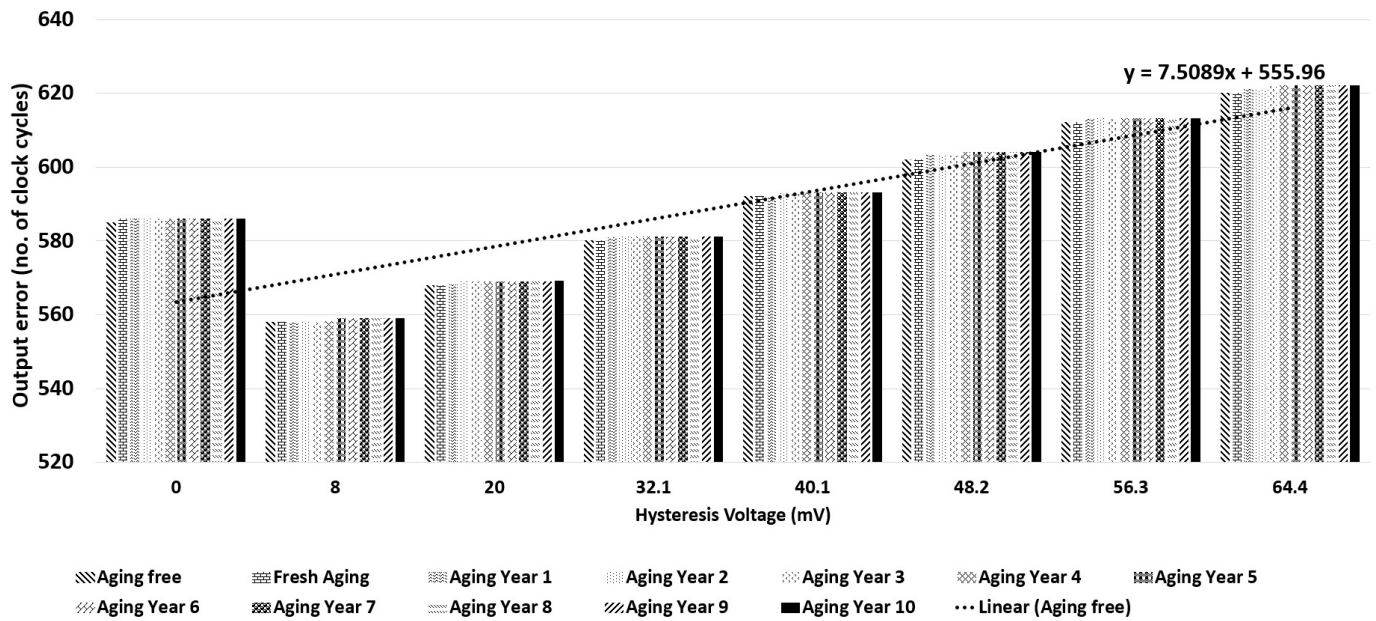


Fig. 6. Output error versus hysteresis voltage under aging impact, including aging-free for freq = 1 GHz