Static Aging Analysis Using 3-Dimensional Delay Library

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***Abstract*—The growing concern about time-dependent performance variations of CMOS devices due to aging-induced delay degradation has increased with shrinking technology dimensions of the devices . One of the main causes of aging is Negative Bias Temperature Instability (NBTI). Modeling NBTI-induced delay at gate level depends on the real stress activity of gate inputs which are related to the workload applied from the higher level of abstraction (e.g. Application). Having estimated values about the degradation delays can make design stage to consider this issue as a design constrain and even to precisely allocate the online aging sensors. this paper propose a method to include the stress probability within technology library as three dimensional look-up tables for Static Timing Analysis(STA) process of the design as an approach named Static Aging Analysis(SAA). the purpose of this approach is instead of estimating only the timing delay at time zero, estimating NBTI-induced delays for predefined lifetime of the product.**

***Keywords*—Negative Bias Temperature Instability (NBTI); Signal Probability; Static Timing Analysis.**

I. Introduction

NBTI can lead to an increase in threshold voltage over time. The first observations of a threshold voltage instability were made in the 1960s in MOS transistors, in which it was found that both bias and temperature affect the threshold voltage. From that time and until the year 2000, when introduction of nitrogen atoms into the oxide was achieved, Bias Temperature Instability (BTI) remained unimportant phenomenon. Since then, negative BTI has become a more important concern, both in academia and industry [1].

In general, there are two possible approaches of aging mitigation techniques either proactive or reactive. Proactive approach works as an estimator for aging behaviour and always based on a model that describes how aging effects (NBTI, HCI and TDDB) are modeled by physicists in low level [2]–[4]. Usually this approach needs to take into account different contributors of time-dependent variations (e.g. signal probability, switching activity, temperature and supply voltage). Another approach is to monitor online the real behaviour of aging through delay sensors [5], [6]. The last approach is more precise and short-cutting the complexity of modeling the aging effects on the system level. However, the main problem of online sensors is area overheads and to moderate this drawback, limited numbers of nodes are needed to be monitored. In order to define the locations and how many sensors to be inserted, offline analysis of aging is inevitable.

This paper propose a method to inject the accurate calculation of the duty cycles derived from the application level to design new library targeting the aging prediction as a method called Static Aging Analysis(SAA). To achieve this we have used a tool to derive the actual stress-recovery ratio of each logic gate from application then build three-dimensional look-up tables for the NBTI-induced timing delays. To the best of our knowledge this is the first aging analysis method which is based on predefined stress-probability library.

The organization of the remainder of the paper is as follows. A concise review of the stress and recovery of NBTI, NBTI mitigation techniques and NBTI modeling are conferred in Section II. Analysis of three-dimensional delay library is presented in Section III. Experimental setup and results are given in section IV and finally Section V. concludes the paper.

II. Background And Related Work

A. NBTI Stress-Recovery sources

Basically, NBTI is generated due to a change in the physical characteristics of a transistor by generating interface traps at the channel and dielectric. The gates of PMOS transistors are negatively biased with respect to the source (i.e. $V_{gs} = -V_{dd}$). Generally, BTI consists of two different phases:

1) Stress: Some interface traps are generated at the interface of substrate/gate oxide layers due to applying electrical stress (i.e. negative bias for PMOS) that leads to breaking of some of the SiH or SiO bonds. Consequently, the threshold voltage of the transistor increases over the time.

2) Relaxation/Recovery: some of the generated interface traps are removed from the interface. However, the relaxation phase cannot completely compensate for the effect of the stress phase and therefore the overall effect of NBTI is a degradation in the threshold voltage of the transistor. The amount of this degradation depends on the ratio between the stress period and the total period (duty cycle).

B. NBTI Mitigation Techniques

In this section, the literature of the mitigation techniques used for aging is presented. A feasible solution to reliability problems including aging is to eliminate or even to reduce the design uncertainties that exist in current design technologies. However, in practice, there is more than one contributor to these uncertainties including EDA tool limitations and complex

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environmental stress conditions [7]. Another solution is conservative design under the worst-case scenarios at the design stage. However, circuits do not always run at the worst-case condition and such an over-designed approach is extremely costly in terms of power and area. At gate level, NBTI manifests itself as time-dependent gate delay and finally leads to timing violations. Adding some margins to the critical path is not a solution because the critical path at time zero may not still be the critical path after some years due to aging. Potential Critical Paths (PCPs) or NBTI Critical Paths take into account the effect of NBTI in static path analysis. In [8], critical gates (gates within PCPs) are identified and optimization methodologies (i.e. gate resizing or reducing temperature) proposed for these critical gates. However, NBTI has a dependence on dynamic operation, such as supply voltage, spatial or temporal temperature and signal probability and these parameters vary dynamically from gate to gate. Another solution, proposed in [9], uses signal probability to restructure the logic gates and arrival times of the input signal to reorder the pins. However, signal probabilities are assumed to be 50% for input signals and for larger systems, signal probability is dynamic and based on the application. Another technique to control NBTI is to control the signal probability using the Input Vector Control (IVC) technique. However, both NBTI and leakage power have a cross dependency on input patterns [4], [10].

C. Long-Term NBTI Model

At device level, many models have been proposed as predictive models to simulate the real degradation in transistor performance. Until now, there is no universally accepted theory or model, therefore all information is based on accepted experimental results. Reaction-diffusion (RD) is one of the most prevalent NBTI models in the literature [8], [4], [11], [3]. Many developments have been proposed to the model to increase the accuracy of the model. The following formulas describe the NBTI-induced degradation threshold voltage using long-term RD model:

$$\Delta V_{th} = \left(\sqrt{K_v^2 \, T_{clk} \, (\frac{\alpha}{1 - \beta_t^{\frac{1}{2n}}})} \right)^{2n} \tag{1}$$

$$K_v = \left(\frac{q t_{ox}}{\epsilon_{ox}}\right)^3 K^2 C_{ox} (V_{gs} - V_{th}) \sqrt{C} exp\left(\frac{2E_{ox}}{E_0}\right) \tag{2}$$

$$\beta_t = 1 - \frac{2\xi_1 t_{ox} + \sqrt{\xi_2 C (1-\alpha) T_{clk}}}{2t_{ox} + \sqrt{Ct}} \tag{3}$$

α is the signal probability and it reflects the fraction of time spent in the stress state over a period of time, and T_{clk} reflects the frequency of stress and recovery phases. The rest of the parameters are described in detail in [3]. We simulate the 90nm technology node using MATLAB with the following parameters: initial $V_{th} = 0.276V, V_{gs} = 1.2V, T = 350K, t_{ox} = 2.15nm$. Fig. 2. shows how duty cycles have a big impact on V_{th} degradation.

- For duty cycle (α)=0.1, V_{th} increases by 130mV (increases 47% from the initial V_{th})
- For duty cycle (α)=0.5, V_{th} increases by 180mV (65%)
- For duty cycle (α)=0.9, V_{th} increases by 210mV (76%)

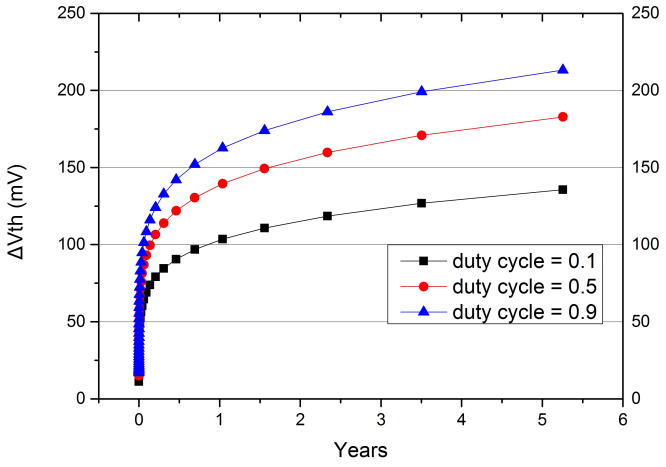

Fig. 1. V_{th} degradation for different duty cycles.

III. 3-Dimensional Delay Library

The standard library that used to estimate the timing and power at the synthesis stage based on pre-calculated look-up tables considering the input transition delay and output capacitance load as two-dimensional LUTs for each standard cell in the library. To generate NBTI induced library for the purpose of estimating the effect of NBTI for pre-defined lifetime of the product, three-dimensional LUT delay library could be built considering the Signal Probability SP(0) as the third dimension along with input transition and output load capacitance. Debatably, signal probability is not the only observable parameter from the application level to transistor level, temperature is possibly observed as a function of switching activity of the transistor. However, the temperature is environment dependent and the spatial deviation of the temperature in a small area is normally small. So, considering the signal probability derived at the application level will not estimate the degradation delay with 100% accuracy, but it will increase the accuracy of the estimation. Further optimization needs to be considered: for example, during the design phase, by restructuring the gates with high signal probabilities. Delay sensors might also be inserted in a limited number of paths to consider other sources of ageing that are difficult to observe during the design phase (e.g. Temperature).

IV. Experimental Setup And Simulation Results

A. Signal Probabilities Extraction

We extract signal probabilities (duty cycles) of the nets from different workloads using Mibench benchmark as workload on OpenRisc 1200 processor (see TABLE I and Fig. 3.).To obtain the duty cycles (signal probabilities SP(0)) of the nets for a specific application, we started from the VCD file to obtain SP(0). The VCD file implicitly contains both switching activity that is used to estimate the dynamic power at the design phase and the signal probability that we use

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to estimate the NBTI effect on performance degradation. So, we built a compiler using open source software (JFLEX and CUP) available in [12] to generate a file contains the SP(0) for all the nets of the processor. Getting VCD file for the gate level needs to simulate the post-synthesized processor. We synthesis OpenRisc using 90nm Technology from Synopses using limited number of netlists that have only one level of transistors to avoid getting hidden signal probabilities inside the multilevel cells. The results show that there is likely stress probability within the nets with different workloads and the signal probability highly related to the architecture rather than the workload as shown in the Fig. 3.).

TABLE I. SIGNAL PROBABILITIES PERCENTAGES FOR MIBENCH WORKLOADS

	Automotive		Telecomm			Network	secuirty
SP(0) Range	qsort	susan	adpcm	crc	fft	dijkstra	sha
0-0.09	26%	20%	24%	20%	24%	20%	20%
0.1-	3%	3%	0%	3%	0%	3%	4%
0.2-	4%	3%	2%	2%	2%	3%	3%
0.3-	2%	2%	2%	2%	2%	1%	1%
0.4-	3%	3%	2%	2%	2%	3%	3%
0.5-	7%	5%	4%	5%	4%	4%	5%
0.6-	4%	2%	3%	3%	3%	2%	2%
0.7-	9%	6%	4%	6%	4%	3%	5%
0.8-	4%	6%	1%	7%	1%	8%	6%
0.9-1	39%	51%	58%	51%	58%	53%	51%

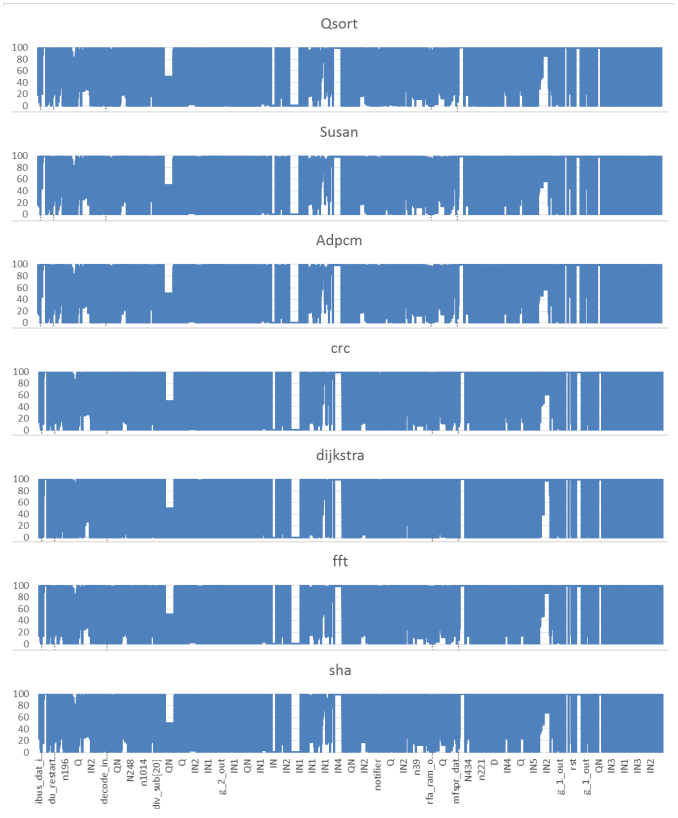

Fig. 2. Horizontal axises: Compressed information about the net names of OpenRisc Processor, vertical axises: Percentages of Signal Probabilities SP(0) for MiBench Workload.

B. Three-Dimensional LUT Generation

Basically, the library file contains four look-up tables, two for rising and falling propagation delays, and two for transition delays that used as an input parameter to calculate the propagation delay for the next cell. To induce signal probabilities SP(0) into the library, we used HSpice simulation to generate the timing delays. the figure Fig. 4. shows the output rising delays when the SP(0) barely stressed and the figure Fig. 5. shows the output rising delays when the SP(0) almost totally stressed. the results show that up to 81% difference between the the cases mentioned above. Choosing how many steps for SP(0) would define the complexity of the delay calculation inside the Static Aging Analyzer. So, some specific steps need to be calculated and any other intermediate values could be either taken the worst case or interpolated from two points.

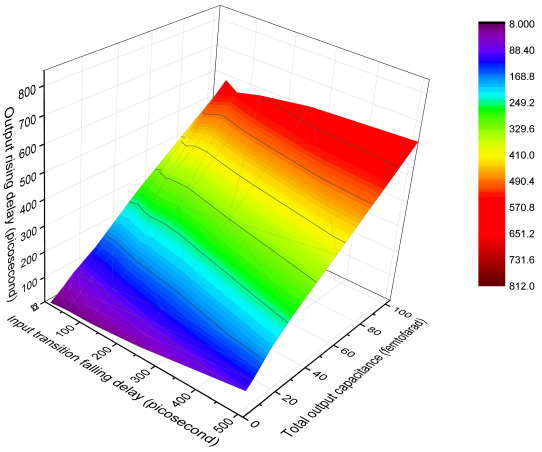

Fig. 3. Output Rising Delays when SP(0)=0.1.

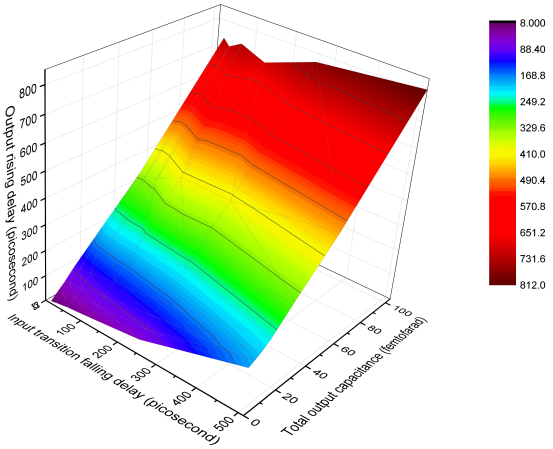

Fig. 4. Output Rising Delays when SP(0)=0.9.

V. CONCLUSION AND FUTURE WORK

This work has proposed an approach to include the signal probabilities driven from the workload to the gate-level timing library. This work could make estimating NBTI-induced delay more feasible during the design and could help to abate the number of aging sensor and location. However, this approach required a logic synthesizer to read these three-dimensional LUT and may make optimization during cell mapping to reduce highly stressed signal in the critical path. Future work will

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consider the use this table by building this logic synthesizer to identify the most vulnerable part for aging in the processor.

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