Implementation of a High Measurement Rate VLP System

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Abstract

Optical positioning systems have raised interest in recent years, due to the centimeter accuracy in three-dimension environments they are able to provide, thanks to the use of light emitting diodes (LED) and diode photoreceptors. This work is based on the design and implementation of the signal processing algorithms for an optical indoor positioning system. It is configured using some LED beacons placed at known positions and the corresponding receivers to be positioned moving in the coverage area. The definition and design of the hardware architecture for the processing associated to the receiver, for the case of a Quadrant Photodiode Angular Diversity Aperture (QADA) detector is proposed, analyzing different aspects involved in the final performance, such as the fixed-point notation used in the hardware definition. Furthermore, the implementation of the proposal includes an analog conditioning stage, an acquisition system, as well as a FPGA-based (Field-Programmable Gate Array) System-on-Chip (SoC) for implementing the necessary hardware and software elements, required to estimate the final position coordinates of the QADA receiver. In addition to the description of the positioning system and all its stages, some preliminary experimental tests are also shown, including position estimation for two specific locations, achieving the validation of a processing system associated with indoor positioning systems capable of handling high data rates (in the range of Msps).

Keywords

Optical positioning systems, acquisition system, FPGA.

1. Introduction

Modern advancements have facilitated the development of various applications and services based on location-based services (LBS) as tracking of individuals, objects, and vehicles (e.g., indoor navigation for guiding people within a building, automatic guided vehicle (AGV) navigation, drones, etc.). The most commonly used Local Positioning Systems (LPS) can be classified according to the five technologies that can be used: optical, mechanical, magnetic, acoustic, and radiofrequency. Among them, LPS that utilize optical signals can use Light Emitting Diodes (LEDs) already deployed across the majority of existing infrastructure [1].

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Optical-based LPSs based on both, visible or infrared (IR) light signals, has gained attention due to their low cost, easy integration into the working environment, and absence of health risks [2, 3, 4]. These systems are employed for both outdoor and indoor positioning purposes, although, generally, the majority of research focuses on indoor positioning, as ambient light has a significant impact on such systems [4]. In indoor environments, whereas the transmitter is typically a lamp or an array of LEDs, the receivers can be classified into image sensor-based positioning systems and photoreceptor-based systems. Image sensor-based positioning systems employ cameras, such as those found in conventional mobile phones or CMOS cameras [3, 5]. However, they require image processing algorithms that slow down position calculations and increase complexity [6].

Photodiodes [7] [8], as well as an array of photodiodes [9] [10], find application in photoreceptor-based positioning systems. These devices generate a current when exposed to light, which is utilized in estimating the position of the receiver through the implementation of an appropriate positioning algorithm. Notably, one such algorithm is derived from the four currents of a Quadrant Photodiode Angular Diversity Aperture (QADA) [9]. The most commonly used positioning techniques based on optical signals are fingerprinting, triangulation, trilateration, or multilateration, by using Angle-of-Arrival (AoA) measurements [13], Time-of-Flight (ToF) measurements [1], or Received Signal Strength (RSS) measurements [11] [12]. These methods can be combined or used separately. There are other methods that can be involved, such as proximity-based approaches [14]. The disadvantages of determining ToFs or Time Differences of Flight (TDoF), along with the required synchronization, lie in the fact that estimation errors of 1 ns result in positioning errors in the range of 30 cm due to the high speed of light [15].

One of the alternatives for real-time implementation of processing and control algorithms often involved in these LPS, specifically in the case of IRLPS (Infrared Local Positioning Systems), is the use of System-on-Chip (SoC) architectures that combine hardware resources with general-purpose processors [16]. These often support high-speed signal processing, typical of an FPGA (Field-Programmable Gate Array), along with the versatility provided by the processor to communicate with other system resources and handle specific tasks that may not be suitable for hardware implementation.

In the case of using QADA receivers with aperture, it is crucial the conditioning block for the sensor signals. This block must operate within a linear range that accommodates wide dynamic signal margins, enabling the provision of both the total output (representing all received radiation from an emitter) and the differential outputs (indicative of beam deviations in horizontal and vertical directions) of the QADA. To enable independent use of the positioning algorithms regardless of the received radiation level, the differential signals must be subsequently normalized with respect to the total signal.

This work focuses on the implementation of an indoor optical positioning system. It is based on a set of LED beacons as transmitters and a QADA (Quadrant Photodiode Angular Diversity Aperture) as receiver. The positioning technique employed is based on AoA measurements between the transmitters and the receiver. The proposed approach includes the low-level conditioning and acquisition system, and all the blocks (hardware and software) needed to obtain the final positioning estimates, and implemented by means of a FPGA-based architecture after the acquisition stage. The novelty of this work is the definition of an efficient System-on-

Chip architecture for the implementation of the signal processing associated with an indoor optical positioning system, where high data rates can be handled (in the range of Msps). The architecture includes the specific peripherals for implementing the demodulation, as well as the matched filtering with the emitted codes, for the three channels coming from the QADA receiver involved in the LPS. On the other hand, the final positioning algorithm, based on the AoA derived from the peaks detected in the correlation signals, is implemented in the processing system, as it deals with a least squares estimator and some trigonometrical considerations.

The remainder of the manuscript is organized as follows: Section II provides an overview of the positioning system; Section III describes the block for signal conditioning and acquisition; Section IV details the proposed architecture within the programmable logic of the SoC and the positioning algorithm; Section V presents some preliminary experimental results; and, finally, conclusions are discussed in Section VI.

2. Description of the Positioning System

The IR positioning system consists of an array of transmitters and a receiver, as shown in Fig. 1. The transmitters are four LED beacons, which are located on the ceiling, emitting each one a signal modulated with a particular code. The employed codes are LS sequences of 1151 bits generated from 512-bit Golay pairs, with an 127-long interference-free window (IFW) [18]. The emitted sequences are BPSK (Binary Phase Shift Keying) modulated with a square carrier at 25 kHz (that can be extended up to 250 kHz). The receiver is composed by one (or more) circular QADA photodetector (model qp50-6-18u-to8) moving anywhere of the coverage area. This photodetector is covered by a square aperture with a side of $l = 2.75$ mm and a separation $h_{ap} = 2.6$ mm, as shown in Fig. 2. This ensures that the light beam always impacts within the sensing area of the QADA, and avoids edge-related issues (non-linearities in subsequent calculations) [17]. The reception is sampled at a frequency of 250 kHz (that can be extended up to 2.5 MHz), resulting in an oversampling ratio of 10 samples per carrier period.

The QADA is composed of four photodiodes, which provide the corresponding currents depending on the projected illumination in their quadrants. The outputs of the QADA are first connected to a conditioning stage, which consists of transimpedance amplifiers. At this stage, the sum of the four outputs $r_{sum}[n]$, the difference between the upper and lower quadrants $r_{bt}[n]$, and the difference between the right and left quadrants $r_{lr}[n]$ are obtained. It is worth noting that the signals coming from the amplification stage are proportional to the light intensity detected by the different quadrants. Finally, these signals are digitized by an analog-to-digital converter (ADC), before going into the digital processing blocks of the system.

Due to the parallelism of the proposed processing and the high data rate intended to be handled while capturing the incoming signals, the implementation of the positioning system is carried out on a FPGA-based System-on-Chip (SoC), which includes programmable logic and multiple processors. The proposed hardware architecture for the reception block, as shown in Fig. 3, is based on three processing stages: Demodulation, Correlation, and Peak Correlation Detection [19]. Firstly, the three mentioned input signals are demodulated, and then passed to the correlation stage with the transmitted LS sequence. Subsequently, the maximum correlation value is obtained for every correlated signal. On the other hand, the software processing consists
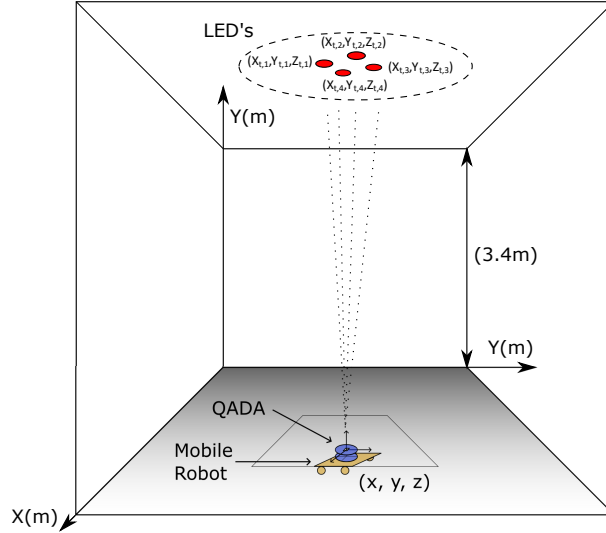
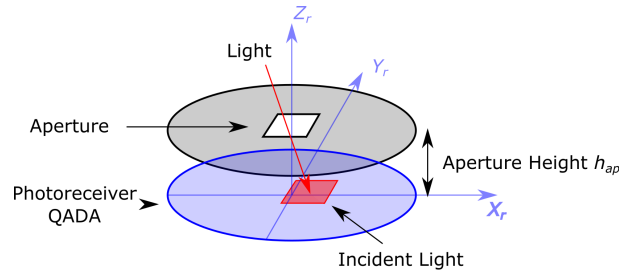**Figure 1:** General overview of the proposed positioning system.

Figure 2: Geometrical representation of the Quadrature Angular Diversity Aperture (QADA) receiver.

of two stages: calculation of impact points and position estimation. Firstly, the central point of incidence of the light is obtained and, secondly, the position coordinates (x, y, z) of the target are estimated. All these blocks (hardware, software) will be explained in more detail in the next Section.

3. Conditioning System with Adjustable Gain

As depicted in Fig. 4, three output signals are generated from the four photocurrents supplied by the QADA: global current (r_{sum}), differential current in the left-right axis (r_{lr}), and differential current in the bottom-top axis (r_{bt}). It is essential that the amplification of these three signals is identical across all the output channels to facilitate the later normalization of the differential currents with respect to the global one. This normalization step is key for accurately calculating the central point of incidence of the beam passing through the aperture.

Usually, the QADA manufacturer provides the analog conditioning system through an evaluation board [20], which has been expanded in this study, as illustrated in Fig. 4. The conditioning
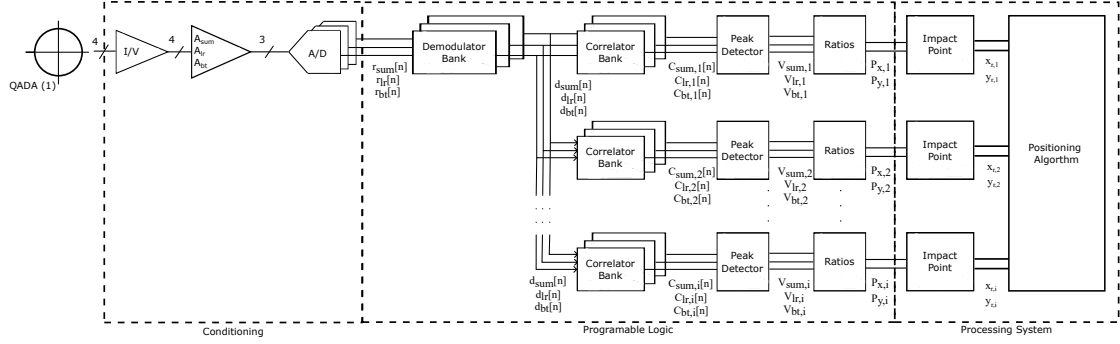
Figure 3: General block diagram of the proposed architecture, consisting of the different peripherals involved in the processing of the signals coming from the QADA sensor.

stage of the QADA outputs incorporates transimpedance amplifiers with continuous and low-frequency (backlighting) signal cancellation [21]. To ensure operation under typical conditions of natural or artificial illumination, the system incorporates a filter that eliminates low-frequency components in the radiation received by the QADA. These low-frequency components come from background radiation caused by natural light or artificial systems' dimming frequencies. Exploiting the fact that the useful emissions are coded and modulated at relatively high frequencies, this filtering stage mitigates undesired signals.
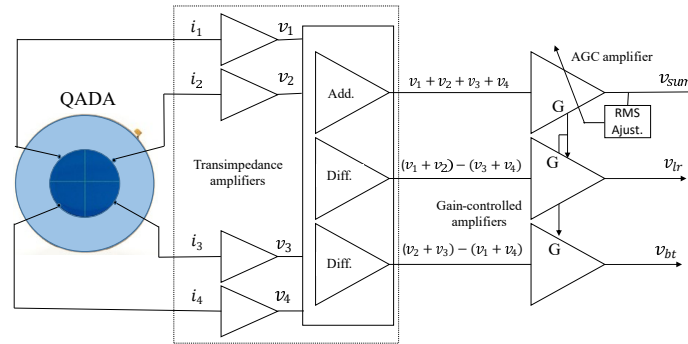

Figure 4: Block diagram of the conditioning system.

Additionally, a high dynamic range automatic gain control (AGC) is applied to the three channels, where the one processing the global signal r_{sum} assumes a master function, that is, it provides the gain G determined by its AGC to the other two channels. In any positioning system, the relative positions between transmitters and receiver vary, resulting in a wide range of signal levels to be managed (differences of up to 100 dB among diverse situations). These signal level variations may occur due to the distance between the emitter and the receiver, or the angles at which the rays pass through the sensor aperture. This defines some limitations on the permissible relative emitter-receiver distances and orientations. A high gain can lead to amplifier saturations, whereas a small gain restricts the reception of low-amplitude signals. To address this challenge, the AGC is incorporated, which dynamically adapts the received

levels at every circumstance. It is implemented using the Analog Devices AD8338 [22]. For the channel representing the global sum of signals r_{sum}, a configuration is employed where the gain is self-adjusted based on the root mean square (RMS) value of the received signal. This channel is selected because it always presents the highest signal level. The self-adjusted gain ensures that the output r_{sum} maintains a fixed RMS value of 10 mV. The obtained gain G at this stage is then used to drive the gain of the amplifiers in the other two channels, r_{lr} and r_{bt}, which operate as programmable gain amplifiers.

The acquisition stage uses an Analog-to-digital converter (ADC) connected to the FPGA board through the FMC HPC connector. An AD9249-65EBZ board is used, which is based on the 14-bit AD9249 that allows conversion rates up to 65 Msps. The FPGA design in charge of addressing this stage consists of two modules: a 3-Wire SPI controller to interact with the SPI circuitry of the AD9249, and an interface block to acquire and process the input data. The block diagram of the proposed design is depicted in Fig. 5.

The 3-Wire SPI controller is made up of a finite state machine (FSM) that manages the three signals in the bus before, during and after a SPI transaction. Furthermore, a busy port is used to report to external devices whether it is busy in a transaction or, on the contrary, is available to start a new one. This peripheral is provided with an AXI4-Lite interface to allow the designer to set up the bus features, as well as the serial clock frequency by means of the processor available in the architecture.
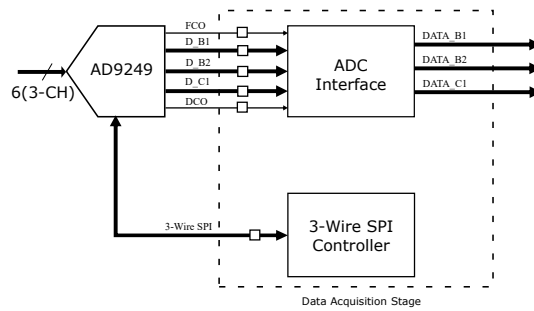

Figure 5: Block diagram of the architecture proposed for managing the AD9249 converter.

On the other hand, the core element of this design is the interface block with the ADC. Its purpose is to carry out the serial data acquisition of the 16 channels. The AD9249 provides the LVDS serial data D_B1 and D_B2, a bit clock DCO and a frame clock FCO, as labeled in Fig. 5. Firstly, these signals are introduced into a differential input buffers to obtain the resulting single-ended signals. Subsequently, a Double Data Rate (DDR) flip-flop stage is used to capture data in both bit clock edges. The data are fed into the block output synchronized with the rising edges of the frame clock, which determines the start of a new data frame. Furthermore, a prescaler is added for downsampling if necessary. This configuration allows high-speed acquisition rates up to 16.25 Msps.

4. Proposed Architecture

The following Subsections describe every stage involved in the proposed hardware architecture; it should be noted that the stages use a fixed-point model [19], where the main objective of such quantification is to implement the highest possible resolution without adding possible errors derived from it.

4.1. Demodulation Stage

Since the demodulation symbols involved in (1) are square wave signals with values of $+1$ and -1 [19], the demodulator proposed in Fig. 3 can be simplified by discarding the multiplications and reducing the demodulation to a summation of the input sample, the output sample, and twice the intermediate sample (2). This architecture requires a shift register to store the necessary previous samples, and the length of the register depends on the number of samples in the demodulation symbol itself. The demodulation stage obtains then the input signals, $r_{sum}[n]$, $r_{bt}[n]$, and $r_{lr}[n]$.

$$d[n] = \sum_{k=0}^{(M/2)-1} r[n-k] - \sum_{k=M/2}^{M-1} r[n-k] \tag{1}$$

$$d[n] = r[n] - r[n-M] + 2 \cdot r\left[n - \frac{M}{2}\right] + d[n-1] \tag{2}$$

4.2. Correlation Stage

In the correlation bank in Fig. 3, an efficient correlator is designed for a Complementary Set of Sequences (CSS) using Golay pairs (2-CSS) [23] [24]. This scheme, also known as 2-ESSC (efficient set of sequences correlator) as shown in Fig. 6, provides two outputs that simultaneously correspond to the correlation of the input signal $d[n]$ with the two complementary sequences S_i from the set. The delay blocks Z^{-D_N} in the efficient correlator are scaled by a factor of $\beta = 10$ to accommodate oversampling in the LS sequences transmission.

The use of this 2-ESSC architecture implies some advantages compared to traditional straightforward implementations of correlators. In the straightforward version, it requires $M \cdot L$ multiplications and $M \cdot (L-1)$ additions to correlate the input signal with M sequences from the set. In contrast, the 2-ESSC only requires $\frac{M}{2} \cdot \log_2 L$ multiplications and $M \cdot \log_2 L$ additions. Here, $M = 2$ is the number of Golay sequence pairs, $N = 7$ denotes the number of stages used when generating the Golay pair, and $L = M^N$ is the length of the sequences [18].

For the correlation of LS codes, using two 2-ESSC, a matched filter is implemented, as described in (3, 4). This is actually an adaptation of a generic efficient correlator for LS codes, which is referred to as Efficient LS Code Correlator (ELSC) [19]. Compared to other types of correlators, such as a straightforward one, the ELSC requires fewer operations.

$$C[n] = \sum_{i=0}^{K/2-1} h_{k,i} z^{-(\frac{K}{2}-i-1)\cdot L_0} \left[z^{-(\frac{K}{2}\cdot L_0 + W)} C_{R,S_{\pi_i,0}}[n] + C_{R,S_{\pi_i,1}}[n] \right] \tag{3}$$

$$C_{k+K/2}[n] = \sum_{i=0}^{K/2-1} h_{k,i} z^{-(\frac{K}{2}-i-1)\cdot L_0} \left[z^{-(\frac{K}{2}\cdot L_0 + W)} C_{R,S_{\pi_i^*,0}}[n] + C_{R,S_{\pi_i^*,1}}[n] \right] \qquad (4)$$
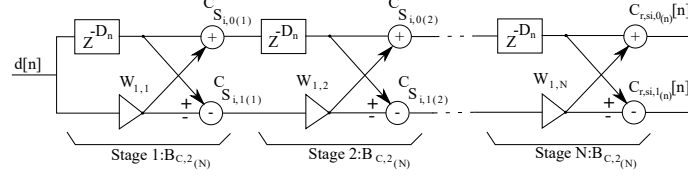

Figure 6: Block diagram of the 2-ECSS architecture.

Note that $C[n]$, with $0 \le k \le \frac{K}{2}$, represents the correlation of the demodulated input signal $d[n]$ with the transmitted LS code; and $h_{k,i} \in -1, 1$ represents the elements of the Hadamard matrix used for generating the LS code. Similarly, $C_{R,S_{\pi_i,0}}(z)$ and $C_{R,S_{\pi_i,1}}(z)$ represent the correlation between the signal $d[n]$ and the sequences S_0 and S_1 from the sets used in the generation of the LS code itself. As previously mentioned, for clarity's sake, the demodulated sequences, $d_{sum}[n]$, $d_{lr}[n]$, and $d_{bt}[n]$, obtained from the aforementioned efficient demodulators explained earlier, are correlated using this architecture.

4.3. Detection of the Maximum Correlation Values

To maximize the detection accuracy, the search of the maximum value is performed on the correlated signal for the global sum signal, denoted as $C_{sum}[n]$, as it has the highest amplitude among the three signals. From the maximum value of this sequence, V_{sum}, the maximum values of the other two signals, V_{lr} and V_{bt}, can be determined at that same instant. These values are further normalized, as expressed in (5), with respect to the sum value V_{sum}.

$$\hat{P}_x = \frac{V_{lr}}{V_{sum}}$$
$$\hat{P}_y = \frac{V_{bt}}{V_{sum}} \qquad (5)$$

4.4. Estimation of Central Impact Points

The central incidence point (x_r, y_r) of the transmitted light beams on the QADA receiver can be calculated by using the previously obtained ratios $\hat{P}_x$ and $\hat{P}_y$ and the side length l of the square aperture as shown in (6).

$$\begin{bmatrix} x_r \\ y_r \end{bmatrix} = \frac{-l}{2} \cdot \begin{bmatrix} \hat{P}_x \\ \hat{P}_y \end{bmatrix} \qquad (6)$$

An offline calibration process can be made to obtain the intrinsic parameters of the sensor if there is a misalignment between the aperture and the sensor (see Fig. 2) [17]. It should be

noted that the manufacturing process of the aperture is quite strict and must be achieved with the highest possible accuracy (square shape and thickness of the aperture),the fabrication and placement of the aperture is done with the utmost accuracy, but there will still be imperfections that can be compensated for with calibration.

4.5. Final Position Estimation

The last step is to estimate the position of the QADA receiver, based on the previously calculated image points $(x_{r,i}, y_{r,i})$ in Fig. 3. In order to estimate the target position, it is necessary to know the positions $(x_{t,i}, y_{t,i}, z_{t,i})$ of each LED emitter, the focal height of the aperture used (h_{ap}), and an initial estimate of the QADA position (prior estimate). From these data, the position estimate (x, y) can be estimated using a least squares estimator (LSE), such that $(x, y) = (\mathbf{A}^T \cdot \mathbf{A})^{-1} \cdot \mathbf{A}^T \cdot \mathbf{b}$ according to (7).

$$
\mathbf{A} = \begin{bmatrix} -y_{r,1} \ x_{r,1} \\ -y_{r,2} \ x_{r,2} \\ -y_{r,3} \ x_{r,3} \\ -y_{r,4} \ x_{r,4} \end{bmatrix} \qquad \mathbf{b} = \begin{bmatrix} y_{t,1} \cdot x_{r,1} - x_{t,1} \cdot y_{r,1} \\ y_{t,2} \cdot x_{r,2} - x_{t,2} \cdot y_{r,2} \\ y_{t,3} \cdot x_{r,3} - x_{t,3} \cdot y_{r,3} \\ y_{t,4} \cdot x_{r,4} - x_{t,4} \cdot y_{r,4} \end{bmatrix} \tag{7}
$$

Where $(x_{r,i}, y_{r,i})$ are the position of the photoreceptor. Once the estimation of the position coordinates (x,y) is implemented, the z coordinate is obtained by trigonometric considerations (8), where the distances d_i between the estimated position and the projection of the QADA photoreceptor in the transmitter's plane are taken into account.

$$
z_i = z_{t,i} - h_{ap} \cdot \left(1 + \sqrt{\frac{(x - x_{t,i})^2 + (y - y_{t,i})^2}{x_{r,i}^2 + y_{r,i}^2}} \right) \tag{8}
$$

5. Experimental Results

Some preliminary experimental tests have been carried out in a $3 \times 3 \ \text{m}^2$ room with a height of 3.4 m, as shown in Fig. 1. Four LED beacons simultaneously transmit their corresponding 1151-bit LS codes, BPSK modulated with a carrier frequency of 250 kHz at a sampling rate of 2.5 MHz, then using a CDMA (Code Division Multiple Access) technique. The LED beacons are located in the ceiling of the room, distributed at the four corners of a square with approximately a side of 1.2 m. The receiver is located on the floor of the room, thus, the final distance between transmitters and the receiver is longer than 3.4 m. The circular QADA receiver has a square aperture with a side of $l = 2.75$ mm on it, with a separation of $h_{ap} = 2.6$ mm. The hardware setup used to perform the measurements is shown in Fig. 7; it includes the conditioning module, the acquisition module and the SoC with the hardware architecture.

For the test only the estimation of the (x, y) coordinates will be taken into consideration, not the z coordinate, since the positioning system is evaluated only in 2D. However, it should be noted that the errors in the estimation of the (x, y) coordinates are added to the possible errors in the z coordinate, due to the method of calculating it, according to (8). Tests are performed in a noisy environment, exposed to artificial and natural light. To validate the proposal, two test
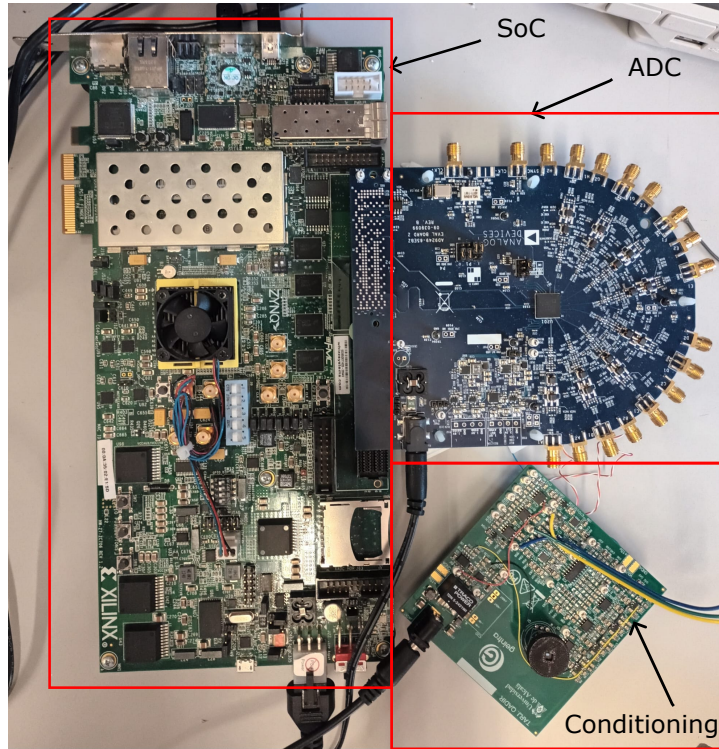
Figure 7: Position estimates for a point on the floor under the beacon B2.

points are considered, no. 1 located under the beacon B2, and no. 2 in the middle of the square formed by the beacons. Therefore, they are located at the position $(x, y, z) = (-1.63, 1.89, 0)$ m for point no. 1 (see Fig. 8), and at the position $(x, y, z) = (-1, 1.4, 0)$ m for point no. 2 in the middle of the scenario (see Fig. 9). Thirty position estimates are obtained at each point, from which we can obtain the mean value and standard deviation shown in Table 1. It is possible to observe that the averaged estimated coordinates are close to the real position, whereas the standard deviations of errors remains below 20 cm in the worst case. Note the appearance of a few outliers (see Fig. 8 and 9) possibly due to impulsive noise in the environment in which the tests were carried out.

Table 1
Averaged estimated positions and standard deviations for the test points

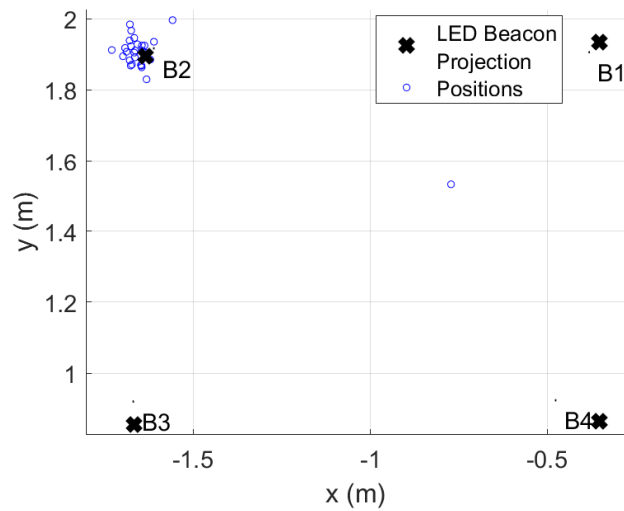| Points	Mean estimated coordinates			Standard deviation		
	X (m)	Y (m)	Z (m)	X (m)	Y (m)	Z (m)
No. 1	-1.626	1.896	0.013	0.190	0.080	0.124
No. 2	-1.015	1.368	0.044	0.129	0.156	0.059

Figure 8: Position estimates for a point on the floor under the beacon B2.
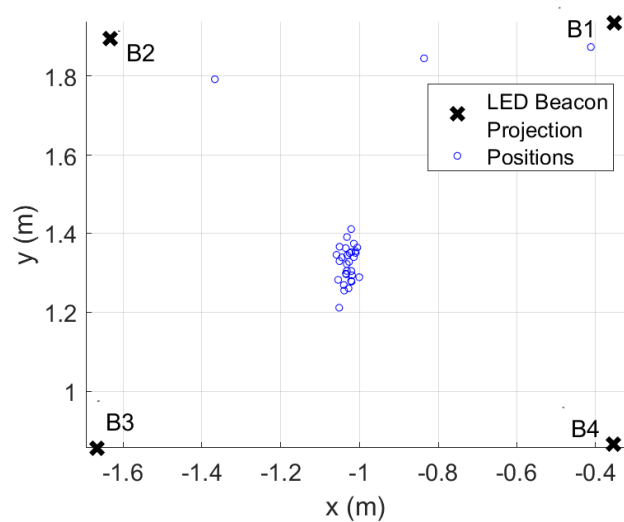

Figure 9: Position estimates for a point on the floor, placed in the middle of the square formed by the four LED beacons.

6. Conclusions

This work has defined and designed an efficient architecture for the implementation of the signal processing associated with an indoor 3D infrared positioning system. The positioning technique employed is based on AoA measurements between the LED transmitters and a QADA receiver. The proposed architecture involves an analog conditioning stage, an acquisition stage, and a FPGA-based SoC that implements all the different hardware and software modules necessary

to estimate the final position of the QADA receiver. Some preliminary experimental results have been obtained for two test points, where the achieved standard deviation of the position estimates are below 20 cm, thus proving the feasibility of the proposal.

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