Methodology of FPGA Implementation and Performance Evaluation of Polar Coding for 5G Communications

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Abstract

This article is devoted to the study of noise immunity of an infocommunication system with Polar Coding (P-C). The results of evaluating the performance of the Successive Cancellation (S-C) decoder are presented. The main contribution of this paper is the result of the compromise between high latency and Field Programmable Gate Array (FPGA) resources to implement a P-C decoder for 5G communications. The stages of channel polarization, the mathematical description of P-C, and the features of their description in binary channels are presented separately. This is achieved by the method of mathematical modeling of information and statistical characteristics of P-C for different code configurations. To check the correctness of the decisions made, a comparative description of the advantages and disadvantages of P-C decoding algorithms is given. The specifics of the FPGA implementation of the S-C algorithm have been studied. Based on the results of the experiment, the noise immunity of the P-C channel was assessed when changing the length of the code block, adding Cyclic Redundancy Check (CRC), and reversing bits at different code rates. It is expected that the results will be useful in optimizing the design process of real P-C circuits.

Keywords

5G, FPGA, polar codes, decoding, SNR.

1. Introduction

Providing tasks related to the transmission of information in mobile telecommunications is certainly accompanied by a variety of error scenarios [1–3]. Among the main factors in the occurrence of errors, emphasis should be placed on random noise, as well as the imperfection of devices, which distorts streaming data on the receiving side. In such situations, where the concept of the receiver correcting such errors without additional information from the transmitter is involved, the forward error Correction (FEC) Format Is Implemented [4].

When implementing 5G NR technology [5–7], the solution to the above problems is carried out by implementing the physical layer channel coding format through the integration of P-C and QCLDPC codes [8–10]. In general, 5G implementation contains the concept of increasing capacity for the eMBB deployment scenario—mobile communications; URLLC—ultra-reliable communication with minimal latency and mMTC—machine-type mass communications. This broad palette of 5G [11] implementations places a demand on channel encoders/decoders to support a variety of code lengths for both user and control data, including robust implementation of automatic repeat request (HARD) data.

Analysis of reliable P-C application scenarios allows us to confidently assert that such codes

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can increase communication throughput and, importantly, are characterized by simplified encoding/decoding procedures. In this case, you should pay attention to the S-C algorithm [12], which, due to its satisfactory complexity, has shown its effectiveness in real applications. Another important property of this algorithm is that it creates wide possibilities in the context of improving hardware architecture. We must emphasize that for P-C the compromise between high latency and FPGA resources is a problem area for reliable decoder implementations in the task of ensuring high throughput of information channels [13, 14].

A significant part of the available literature does not take into account the specifics of codes for 5G scenarios, as well as the process of encoding them, taking into account their further widespread use in the design of encoding circuits using FPGAs. The work [15] proposes a concept for implementing performance enhancement by introducing Polar Code Modulation with Physical Network Coding (PM-PNC) over Two-Way Relay Channels (TWRC). The article [16] focuses on describing a proposed method for building a Multi-Kernel (MK) P-C for 5G, based on large kernels of the same size to improve the quality of error correction. The paper [17] proposes a new coding scheme for 5G and P-C MIMO-OFDM systems to improve the efficiency of channel error correction. The use of Convolutional Neural Networks (CNN) technology along with the use of P-C was proposed, which resulted in a significant increase in the reliability of the circuits. The proposed work [18] compares LDPC and P-C for robust implementations of 5G NR-URLLC channel coding schemes. An assessment of P-C performance for the described scenarios is given. Reasonable and balanced recommendations for the design and practical application of polar codes are reflected in several current publications [19–22].

Before formulating the problem statement for the research presented in the article, we will touch upon certain aspects of P-C. We emphasize that P-C is a family of Error Correction Codes (ECC), which are capable of achieving the throughput of memoryless symmetric channels. Such codes, with sufficient correction capacity, can satisfy the requirements for high-quality error correction for current block lengths and reliable decoding algorithms. It is these key factors that determine the intensive use of such codes in 5G applications.

Analysis of the principles of P-C decoding allows us to give such a characteristic to decoding algorithms. In the case of SC, an alternating bit evaluation of the message from 1 to N is implemented based on the format of the decision procedure. Therefore, it is important to note that the asymptotic performance of the S-C generally corresponds to the channel capacity, although in the case of finite code lengths, it is not always satisfactory. In this context, S-CL (successive cancellation list) decoding minimizes errors [23]. Note that practical schemes for using P-C can be implemented in a concatenated format with other codes, in particular CRC [12]. We also have to decouple the recursive P-C decoding scheme using Bhattacharyya Parameters (BP) [24]. Analysis of the above-described works of leading authors allows us to formulate the main issues that are addressed in the article. Thus, the complexity of the code determines the amount of energy consumed by the decoder, the amount of memory used, latency, and the overall computing power. Channel coding uses a set of operations on a data stream aimed at error correction. In such a context, to improve coding performance, it is necessary to synthesize highly productive code for efficient channel error localization. It is also important to solve the problem of synthesizing a decoding scheme with minimal cost, satisfactory encoding rate, and computational complexity.

The proposed work contains an addition to the works of the authors described above regarding the study of a communication system with an S-C decoder on an FPGA. Using MATLAB tools, the effectiveness of the proposed FPGA solutions was studied and the decoding noise immunity was assessed.

2. Channel Polarization and Polar Encoder

From the point of view of designing P-C using FPGAs, it is quite important to maintain a balance between the delay value and the available matrix resources, which will directly affect the increase in the performance of a high-throughput decoder.

The general form of description of the P-C code word is x, implemented by representing the code length as $N=2^n$ and by K as the number of information bits. In addition, frozen bits in the form N-K are described.

$$x = u \cdot G_N, \tag{1}$$

where $G_N = B_N \cdot F_2^{\otimes n}$ is the representation of the generator matrix; B_N is the form of the permutation matrix, $F_2^{\otimes n}$is the n-th Kronecker degree.

$$F_2 = \begin{vmatrix} 1 & 0 \\ 1 & 1 \end{vmatrix}, \tag{2}$$

Formula 3 represents the generator matrix for $N = 8$. Thus, the encoding scheme equivalent to the generator matrix is shown in Fig. 1 [10]. We used the concept of polarization for a Binary-Input Discrete Memoryless Channel (B-DMC) W and described the channel capacity $I(W)$.

$$G_8 = \begin{vmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 & 1 & 1 & 0 & 0 \\ 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 \\ 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \end{vmatrix}, \tag{3}$$

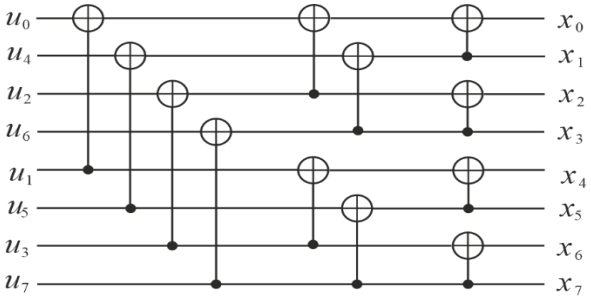


Figure 1: Polar encoder circuit for $N = 8$

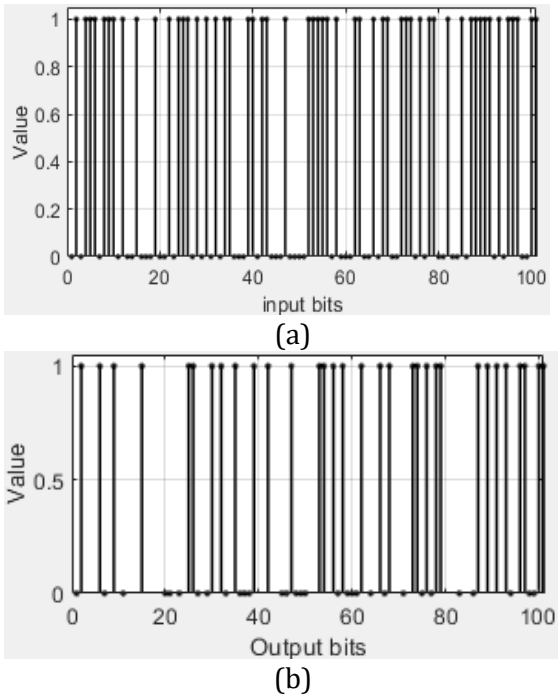
We denote as W^N the channel corresponding to N using the W channel; thus $W^N: X^N \to Y^N$ from $W^N(y_1^N|x_1^N) = \prod_{i=1}^N W(x_i, y_i)$. In the description, parameters such as symmetric channel capacity [25] and the BP were used:

$$I(W) = \sum_{y\in Y}\sum_{x\in X}\frac{1}{2}W(y|x) \times \tag{4}$$

$$\times \log_2 \frac{W(y|x)}{0{,}5[W(y|0)+W(y|1)]} Z(W) = \sum_{y\in Y}\sqrt{W(y|0)W(y|1)}, \tag{5}$$

where $W(y|x)$ we denote the transition probabilities between output y and input x.

It should be noted that the parameters used act as measures of rate and degree of reliability. So, by $I(W)$ we mean the highest rate while ensuring reliable communication through W. Then $Z(W)$ is interpreted as the upper limit on the probability of error in the case of a maximum likelihood decision. We emphasize that in this case $Z(W)$ and $I(W)$ belong to the values [0, 1]. An example of the action of a binary channel with erasure (B-EC) on a sequence of bits is shown in Fig. 2. Channel capacity $I(W)\approx1$ in the case of $Z(W)\approx0$, and $I(W)\approx0$ in the case of $Z(W)\approx1$ is described by formulas 6 and 7 [26].



(a)

(b)

Figure 2: An example of the action of a B-EC on a sequence of (a) input and (b) output bits

An example of channel capacity calculation for $N = 8$ is shown in Fig. 3. We used the following indicators for calculation:

- Code length $N = 8$.
- Code rate $R = 0.5$.
- Number of information bits $K = N*R = 4$.
- Number of frozen bits $F = N\text{-}K = 4$.
- Positional configuration of information bits $A_i \in (5,3,2,1)$.
- Positional configuration of the bits subjected to freezing $A \in (8,7,6,4)$.

Therefore, before transmitting the sequences, the indices of the ascending-sorted data sequence are divided into two sets. Thus, in this design, the first set is formed by indices

of data transmitted in the absence of interference in the channel. While the second set covers known indices that are frozen and transmitted over noisy channels.

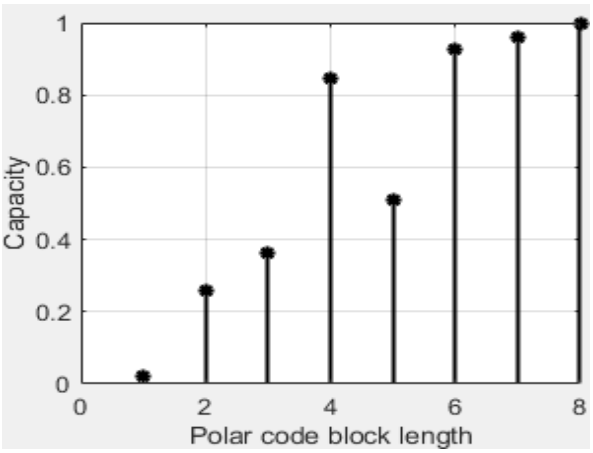
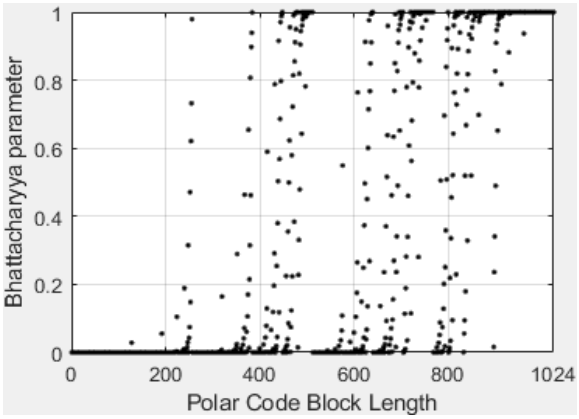
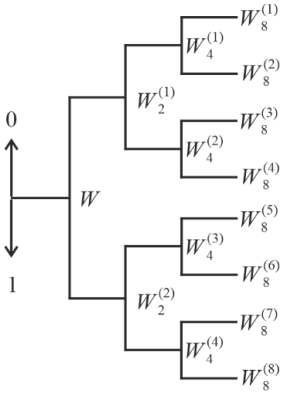


Figure 3: Channel capacity calculation

Binary Symmetrical Channel (B-SC) and B-EC refer to symmetrical channels. The polarization operation can then be interpreted as the formation of *N* independent copies of a given B-DMC channel W of another set of N channels $\left\{W_N^{(i)}: 1 \le i \le N\right\}$ exhibiting the effect of polarization in such an interpretation that when N becomes large, the symmetric terms of the capacity $I\left(W_N^{(i)}\right)$ are directed to 0 or 1 for all indices (see Fig. 4a). This operation consists of a channel combining step and a channel splitting step. In Fig. 4a we present the effect of channel polarization for conditions when W enters the B-EC with probability ε=0.5. Fig. 4a shows that $I\left(W_N^{(i)}\right)$ tends to be close to 0 for small i and 1 for large i (is the node number, Fig. 4b) The binary tree formed by channel polarization is shown in Fig. 4b.



(a)



(b)

Figure 4: Channel formation process (a) Channel polarization, (b) Binary tree formed by channel polarization

An initial tree node is connected to channel W. Such a node W forms a top path $W_2^{(1)}$ and a bottom path $W_2^{(2)}$ that is connected to two nodes at level 1. The path $W_2^{(1)}$ in turn generates branches of $W_4^{(1)}$ and $W_4^{(2)}$ so on. Path $W_2^{(i)}$ is located at level n of the tree at node number i, counting from above.

Let's analyze Fig. 4a. By the concept under consideration, the upper limit of BP corresponds to the state of the channel with the highest noise level, while the lower limit characterizes the state of the minimum noise. Consequently, the ideal state is determined by the discontinuity area in the BP extrema. At the transmitter side, K information bits are inserted into the noiseless channels, and N-K frozen bits are inserted into the corresponding pure noise channels to create an input vector u_1^N to be transmitted by the W channel. We use the BP parameter as a measure of reliability. Then such a parameter sets the upper limit on the probability of decision error for the maximum probability in the case of a transmission channel of a binary configuration.

3. Polar Decoder Concept

The basic polar decoding algorithm is already mentioned in the S-C article. There are also known decoding algorithms with higher

performance for relatively short codewords but with greater complexity, such as the S-CL algorithm, the successive cancellation list decoding algorithm using CRC (CA-S-CL) [7], and the Belief Propagation (PB) algorithm [8]. The PB algorithm is well known for its application in LDPC decoding [7], in which soft messages are exchanged between nodes. In addition, the S-LC method stores a list of solutions and selects the best solution using sorting. Both have better performance, especially since the SLC algorithm provides the best BER gain for P-C with short block lengths. We will focus on the S-C decoding algorithm for FPGA implementation due to its satisfactory complexity.

Fig. 5 shows the FPGA implementation of the S-C decoder.

Each decoding stage is made up of $N/2$ nodes of type f and g (see Fig. 5), which are connected in a structure conceptually similar to a Fast Fourier Transform (FFT) butterfly. Nodes implement basic Likelihood Functions (LLR) like:

$$f(a,b) = 2arth\left[th\left(\frac{a}{2}\right)\cdot th\left(\frac{b}{2}\right)\right], \quad (6)$$

$$g(\hat{u}_s,a,b) = (1-2\hat{u}_s)a + b, \quad (7)$$

Estimated values are calculated as follows:

$$\hat{u}_i = \begin{cases} 0, & \dfrac{\Pr\left(y|\hat{u}_0^{i-1},u_i=0\right)}{\Pr\left(y|\hat{u}_0^{i-1},u_i=1\right)} \geq 1 \\ 1, & \text{otherwise} \end{cases} \quad (8)$$

Equation (8) can be replaced by the minimum sum approximation, which is described by the expression:

$$f(a,b) = \min(|a|,|b|), \quad (9)$$

where a, b is the LLR.

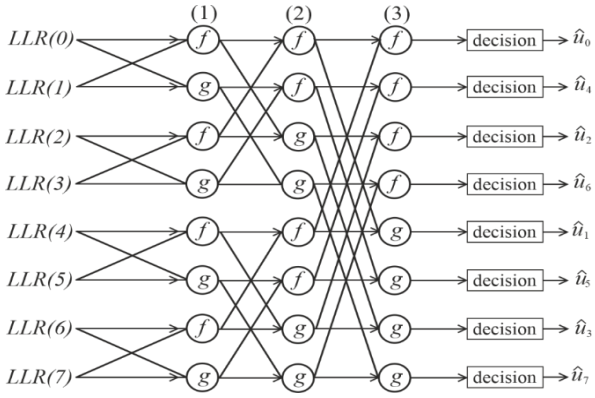


Figure 5: P-C decoder code tree, N = 8

This approximation is typical for calculating the control node for the LDPC code [9]. The node g implementing (7) is a conditional addition/subtraction conditional on the value of the decision bit $\hat{u}_s$, where $\hat{u}_s$ is the bit representing the partial sum modulo 2 of the previously calculated bits. The rule for calculating partial sums of $\hat{u}_s$ is based on a structure that copies the corresponding P-S. Inside the Flow Data Graph (FDG) decoder there is an integrated FDG encoder. Then the partial sum $\hat{u}_s$ for node, $g_{1,2}$ is equal to $\hat{u}_2 \otimes \hat{u}_3$, and the corresponding partial sum $g_{3,4}$ is equal to $\hat{u}_6$. This means that to update node g, its output must determine $\hat{u}_6$. Then for hard messages, we get the following rule:

$$\hat{s}_{i+1,j} = \begin{cases} s_{i,j} \oplus s_{i,j+2^{i-1}}, & \left|\dfrac{j-1}{2^{i-1}}\right| \bmod 2 = 0 \\ s_{i,j}, & \text{otherwise} \end{cases} \quad (10)$$

This approximation is used to calculate the control node. The S-C decoding algorithm is implemented by solving the following problems. In the first stage, the LLR (12) is determined and a hard decision is made. In the next, second stage, solutions are recursively propagated from the current nodes to the corresponding previous stage.

$$LLR_{i,j} = \quad (11)$$

$$\begin{cases} \min\left(\left|LLR_{i+1,j}\right|,\left|LLR_{i+1,j+2^{i-1}}\right|\right), \left|\dfrac{j-1}{2^{i-1}}\right| \bmod 2 = 0 \\ (1-2s_{i,j-2^{i-1}})LLR_{i+1,j-2^{i-1}} + LLR_{i+1,j}, \text{otherwise} \end{cases}$$

Thus, the end of the decoding process is the selection of the codeword with the most reliable path. In general, one can point to the improved performance of SCL compared to SC. This is especially noticeable at low noise levels and low LLR values. However, the SCL algorithm is more complex than the SC algorithm and, in addition, the decoder has an increased delay compared to the decoder implemented in the article using the SC algorithm.

Conducting a brief digest of P-C decoding algorithms, we emphasize that the CA-SCL algorithm [27] is an improved SCL algorithm for medium and short-length code structures. We emphasize that CRC is a frequency structure used to localize errors in several information transmission schemes. In this case, the K-bit encoder input block contains a structure of k information bits and an m-bit CRC sequence. CA-SCL-based decoding then performs a CRC check to reliably determine

the codeword. This design is characterized by increased productivity.

It is necessary to mention the design of the BP decoder described by Arikan [26]. The structure of FDG here is similar to SC. However, in this case, the transfer of hard decisions is replaced with BP by estimates between check nodes and variable nodes. In this case, you can get a performance gain compared to SC, but using the concept of parallelism is quite problematic. Consequently, the BP decoder has increased complexity and limited throughput compared to the SC implementation

4. Development of a Low Complexity Decoder

The graph configuration (Fig. 5) during S-C decoding is formed by 2n trees in binary form [28, 29]. To optimally use the resources of the FPGA circuit, one tree was built in binary form with the option of having custom nodes.

This architectural design of the P-C decoder was based on the use of the same pair of LLRs for a pair of nodes of type f and g. This approach allows you to concentrate nodes of type f and g in one processor unit. As noted above, one evaluation tree of a binary design was used—$\hat{u}_i$ (8). In this configuration, we received a decoder formed from 2^n-1 processing units, and here the LLR is estimated by making a hard decision. In addition, the set of bit decisions used for the g nodes in the processing units is concentrated in memory for current use.

Let's consider an eight-point P-C model based on the formation of two combinational decoders with N=4. This format is used to implement the parallel computing structure, and the generated graph for N = 8 is used to generate the input data of combinational decoders. The calculation of node g is implemented by supplying the output of the encoder with correctly identified bits and using the output of the decoder to make decisions at node g in the next stage. In the structure of the binary tree for the S-C decoder, when some of the blocks are inactive, an updated set of LLR channels is added.

To implement a node of type f, in the minimum sum (min-sum) approximation, the circuit includes a component that solves the ABC function to calculate the absolute value of the output. A comparator circuit is used to identify the minimum value. The circuit includes two multiplexers, where the first determines the minimum code value and generates the comparator output signal. Then the output of this multiplexer and its additional code are transmitted to the input of the second multiplexer in Fig. 6a.

The output signal of the XOR element generates a multiplexer selection signal. We calculate the min-sum using the following form:

$$output = sign(l_a) * sign(l_b) * \min\big(abs(l_a),\ abs(l_b)\big). \quad (12)$$

The node function g is formed by conditional addition/subtraction, which depends on the bit value $\hat{u}_s$ at the corresponding point in the decoder functional graph. Depending on the value, "a" is selected in one of the warehouses, or the additional code "a" is selected (Fig. 6b). This component implements the adder. Node g is defined by the following expression:

$$g(\hat{u}_s, a, b) = (1 - 2\hat{u}_s)a + b, \quad (13)$$

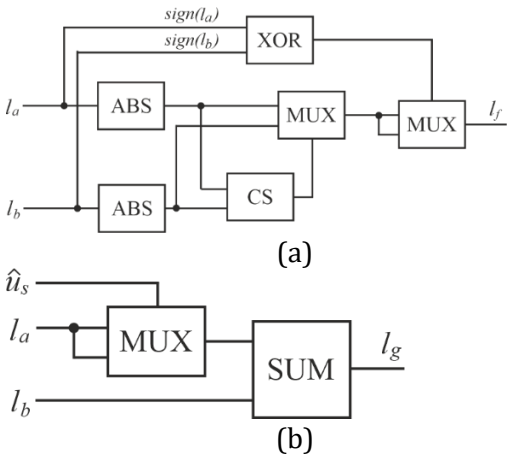


Figure 6: Block diagram of nodes (a) f: ABS is the absolute value, CS is the compare and select, MUX is the multiplexer, and (b) g: SUM is the adder

5. Experimental Studies of the Decoder

We conducted the research by implementing the communication system in MATLAB, Fig. 7.

To implement the P-C encoder and decoder, we selected the FPGA System-on-Chip (SoC)

Intel DE10-Standard Development Kit. The Cortex-A9 processor has two integrated cores with programmable logic. The Cyclone V SE 5CSXFC6D6F31C6N SoC integrates an ARM-based Hard Processor System (HPS), consisting of a processor, peripherals, and memory interfaces coupled to an FPGA fabric.

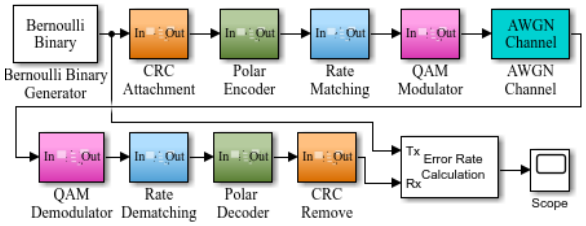


Figure 7: Block diagram of the communication system with P-C

To ensure the tasks of transmitting information in a communication system via P-C, we supplemented the structure of the encoded message with a CRC. The main purpose of adding redundancy is to increase noise immunity. Fig. 8 shows the general shape of the resulting frame and the shape of the generator polynomial:

$$g_{CRC-11}(D) = D^{11} + D^{10} + D^9 + D^5 + 1, \quad (14)$$

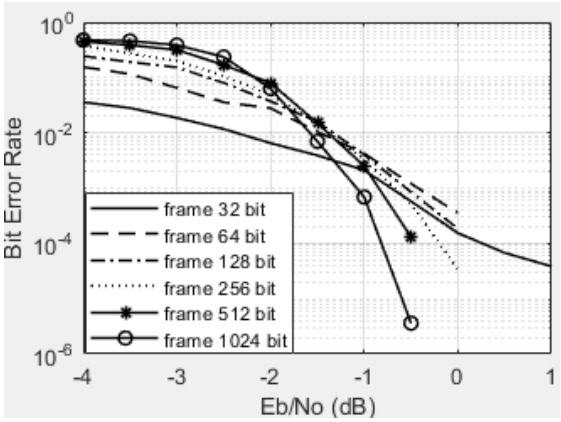
Figure 8: Appending CRC to data bits

Using the above expression, the following bit sequence is formed: CRC-11 = [1 1 1 0 0 0 1 0 0 0 0 1]; CRC is effective as an external error detection code. In the case when the code length m does not agree with the length of the encoded frame ($2^{\log(M)}$), it is necessary to use the rate matching procedure by puncturing in *N-M* positions, with a total codeword length of *N*.

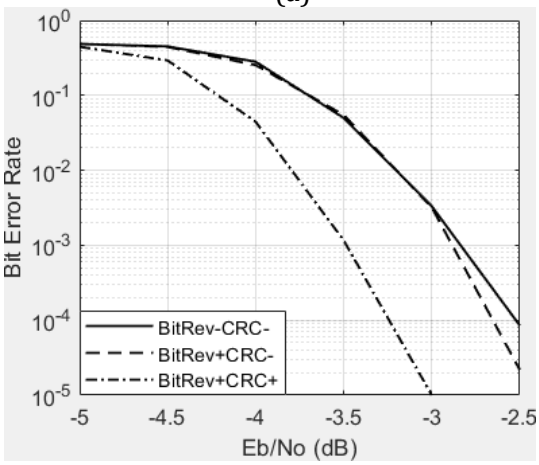
The next step is to carry out digital phase modulation and transmit the signals into the channel. The following operations are performed in the receiver: demodulation; rate restoration when the encoded sequence size (*N*) is updated, in particular by the number of punctured positions (*P*) of the codeword and is sent to the decoder; polar decoding to restore the transmitted message (described above in the article); redundancy implemented in the form of CRC is removed.

Fig. 9a shows the results of a study of the number of bit errors from the signal-to-noise ratio (SNR) for a communication system with BPSK modulation and different code block lengths.

There is no bit reversal, a CRC of 11 bits is connected. For a P-C with block length $M = 32$ and code rate $R = 1/2$, the number of informative bits taking into account CRC: $K = 16$. The number of encoded bits at the output of the P-C encoder is $n = 32$. In this case, there is no puncturing of P-C positions for rate matching [30].



(a)



(b)

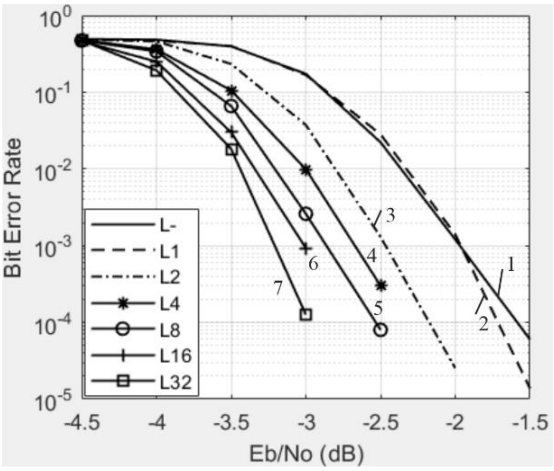
Figure 9: Dependence of BER on Eb/N0 for a communication system (a) With different code block lengths: 1 is the 32 bits; 2 is the 64 bits; 3 is the 128 bits; 4 is the 256 bits; 5 is the 512 bits; 5 is the 1024 bit; (b) With CRC and bit reversal

Fig. 9b shows the results of a study of BER versus SNR [31] for a communication system with CRC and bit reversal.

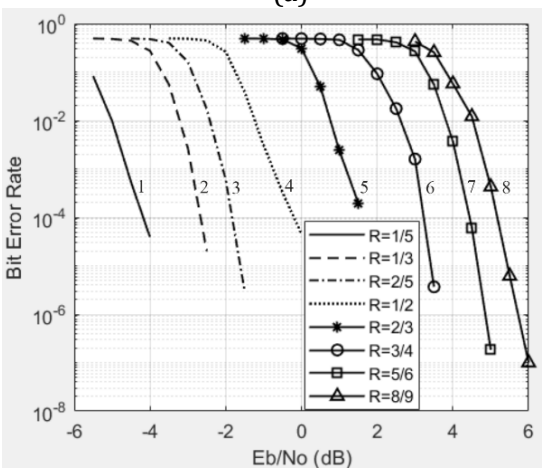
From the results obtained, we can conclude that with an increase in the size of the data block (codeword) from 64 bits to 1024 bits, the noise immunity of the communication system increases by 1 dB.

From the results obtained, we can conclude that the presence of bit reversal accelerates the BER attenuation by 0.2 dB. Connecting CRC increases noise immunity by 0.5 dB.

In Figs. 10a and 10b we present the results of a study of the number of BER from the SNR for a communication system [32] with different exclusion list sizes (L) and different code rates, respectively.



(a)



(b)

Figure 10: Dependence of BER on Eb/N0 for a communication system (a) With different decoder list sizes lengths: 1 is the no list; 2 is the L = 1; 3 is the L = 2; 4 is the L = 4; 5 is the L = 8; 6 is the L = 16; 7 is the L = 32; (b) With different code rates: 1 is the R = 1/5; 2 is the R = 1/3; 3 is the R = 2/5; 4 is the R = 1/2; 5 is the R = 2/3; 6 is the R = 3/4; 7 is the R = 5/6; 8 is the R = 8/9

For modeling, the length of the code word was M = 4000, the length of the code word at the output of the encoder N = 4096, and the number of punctured bits P = 96.

From the obtained dependencies we can conclude that the SLC decoder makes it possible to increase the noise immunity of the communication system: even the list size L = 2 increases the noise immunity by 0.7 dB compared to the classic SL decoder. Further increasing the list size does not provide a significant performance improvement: increasing the list size from L = 2 to L = 32 increases noise immunity by 0.8 dB, but adds significant latency. Increasing the code rate has a greater impact on the bit error rate: increasing the code rate from 1/5 to 8/9 requires a 10 dB increase in the signal-to-noise ratio, but allows a 4.5 times higher data rate.

6. Conclusion

A study of the P-C communication system was carried out. The encoder, P-C decoder, and the principles of channel polarization are considered. The effect of the B-EC channel on a sequence of bits is analyzed. The capacity $I(W)$ of each virtual polarized channel and the principles of dividing these channels into “bad” and “good” by BP value are determined.

A study of the number of bit errors from the signal-to-noise ratio was carried out for a communication system with BPSK modulation and different code block lengths, cyclic redundancy code and bit reversal, different sequential exclusion list sizes, and different code rates. From the results obtained, we can conclude that with an increase in the size of the data block (codeword) from 64 bits to 1024 bits, the noise immunity of the communication system increases by 1 dB. The presence of bit reversal accelerates the BER attenuation by 0.2 dB. Connecting CRC increases noise immunity by 0.5 dB.

Using an SLC decoder with a list size of L = 2 increases the noise immunity of the communication system by 0.7 dB compared to the classic SLC decoder. Further increasing the list size L = 32 increases noise immunity by 0.8 dB, but adds a significant delay. Increasing the code rate has a greater impact on the bit error rate: increasing the code rate from 1/5 to 8/9 requires an increase in the SNR by 10 dB, but allows you to increase the data transmission rate by 4.5 times.

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