# DF-Threads: A Scalable and Efficient Execution Paradigm for Edge Computing and HPC

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**Abstract**
Scalable and distributed computing systems are widely deployed but hide a large toll in terms of energy consumption. A wider adoption of dataflow concepts at any level of the software/hardware stack of HPC system can lead to a reduction of the intrinsic inefficiency of current systems. By leveraging structured parallel programming based on FastFlow, we are exploring the effectiveness of DataFlow Threads (DF-Threads) in tandem with such programming model for Edge Computing and HPC.

## 1. Introduction

Dataflow methodologies have been explored at multiple levels of granularity. At the instruction level, superscalar processors have effectively implemented this by enabling instructions to execute out-of-order as soon as their operands are ready [1, 2].

Programming paradigms such as OmpSs2 and OpenMP manage data flow among tasks and orchestrate the scheduling of potentially large dataflow/asynchronous tasks across available computational resources, including CPU cores, GPU cores, and accelerators [3, 4, 5], while new programming workflows are deemed more appropriate for the Compute Continuum [6, 7].

Despite these advancements, the hardware-software interface still faces challenges: i) a streamlined and efficient mechanism for managing thread-level parallelization, and ii) a widely accepted memory consistency model.

These challenges stem from the requirements for synchronization, consistency, and coherency—a persistent issue exacerbated by the proliferation of cost-effective, massively parallel systems and domain-specific accelerators. The TERAFLUX [8] and AXIOM projects [9, 3] have investigated DataFlow-Threads (DF-Threads) as a potential solution for improving performance scalability while providing a straightforward interface for future massively parallel systems [10, 11, 4] DF-Threads can be integrated into the architecture with the addition of a few new instructions, thereby enhancing existing processors to offer more efficient and effective parallelism. Our experiments indicate nearly perfect scalability for systems with over 1000 general-purpose x86_64 (extended) cores operating on off-the-shelf Linux-based operating systems [12, 13].

In this work, for the first time, a dataflow-based structured parallel programming model like FastFlow [14, 15] is connected to a lower-level dataflow execution model like the DF-Threads. The main objective of this work is to improve the overall energy efficiency and programmability of HPC applications.

## 2. A Brief introduction to DF-Threads and FastFlow

The FastFlow framework [14] consists of a header-only C++ template library that allows programmers to create parallel applications structured as dataflow graphs. Adhering to the thread-based parallelism model, in each FastFlow node embodies a sequential computational unit executed by a dedicated thread. Communication between nodes relies on non-blocking synchronization for fast data processing, especially in high-frequency streaming environments.

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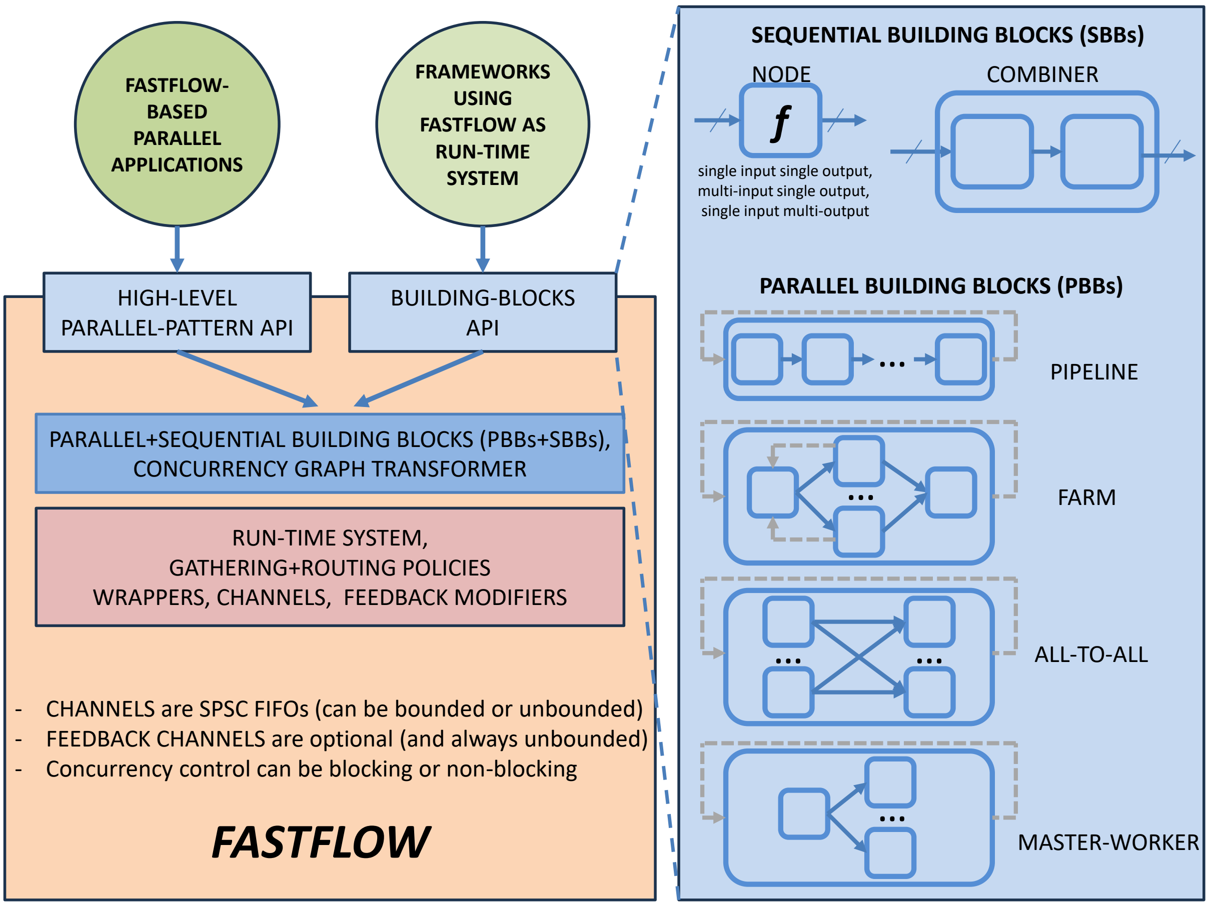

FASTFLOW-BASED PARALLEL APPLICATIONS
FRAMEWORKS USING FASTFLOW AS RUN-TIME SYSTEM
HIGH-LEVEL PARALLEL-PATTERN API
BUILDING-BLOCKS API
PARALLEL+SEQUENTIAL BUILDING BLOCKS (PBBs+SBBs), CONCURRENCY GRAPH TRANSFORMER
RUN-TIME SYSTEM, GATHERING+ROUTING POLICIES WRAPPERS, CHANNELS, FEEDBACK MODIFIERS
- CHANNELS are SPSC FIFOs (can be bounded or unbounded)
- FEEDBACK CHANNELS are optional (and always unbounded)
- Concurrency control can be blocking or non-blocking
FASTFLOW
SEQUENTIAL BUILDING BLOCKS (SBBs)
NODE
COMBINER
f
single input single output, multi-input single output, single input multi-output
PARALLEL BUILDING BLOCKS (PBBs)
PIPELINE
FARM
ALL-TO-ALL
MASTER-WORKER

**Figure 1:** (Left) FastFlow software stack. (Right) Graphical notation of the FastFlow's Building Blocks (from [17]).

Within a single node, FastFlow channels manage references to data allocated on the heap rather than to plain data, with ownership of these references being transferred from the sender (producer) to the receiver (consumer). The FastFlow programming paradigm has served as a foundational technology in large projects such as ParaPhrase, REPARA, RePhrase, TextaROSSA [16] and in Flagship-3 of ICSC Spoke-1 (FutureHPC). FastFlow *Building Blocks* define a reduced set of structured parallel components to build and orchestrate skeleton, parallel patterns and more complex parallel structures [17] (Fig. 1).

At a lower level in the software stack is the execution paradigm called "Dataflow Threads" (DF-Threads) [11] which has its roots in the dataflow execution models implemented in machines such as the IBM BlueGene-C (Cyclops64) [18] and the Scheduled Data-Flow (SDF) architecture [19]. The DF-Threads paradigm can be used to provide performance scalability, extensibility, fault tolerance (repeating computations in time and/or space whose inputs are preserved), and isolation. DF-Threads is a hybrid dataflow/controlflow representation of computation that allows for a reduction in excessive synchronization. DF-Threads can also be mapped onto many forms of parallelization provided by other programming models. DF-Threads were introduced in the TERAFLUX project for the x86_64 architecture [11, 4]. In the AXIOM project the DF-Thread execution model was further developed with specific hardware to support scheduling [20].

Given the above premises, it seems natural to connect the high-level programming model provided by FastFlow with the lower-level dataflow support provided by the DF-Threads (Fig. 2). The combination of this two framework can provide a "win-win" solution as it can enhance the support for distributed execution of FASTFLOW, while it can provide a power high-level programming model for the DF-threads.

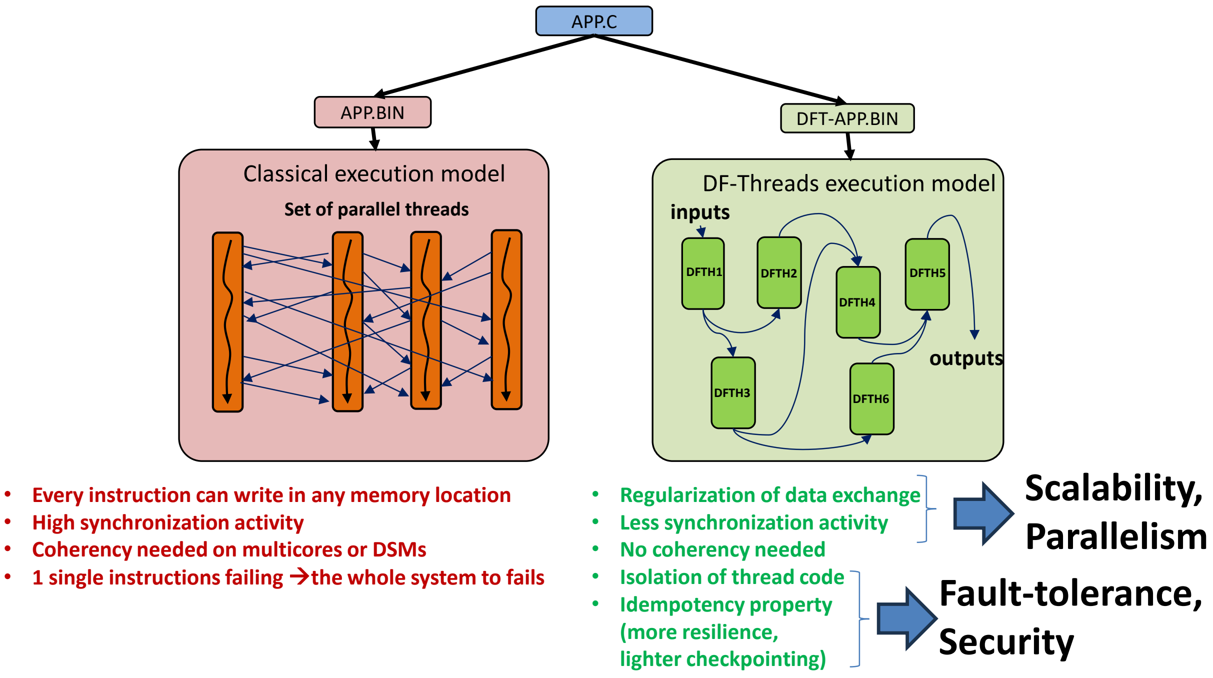
APP.C
APP.BIN
DFT-APP.BIN
Classical execution model
Set of parallel threads
DF-Threads execution model
inputs
DFTH1
DFTH2
DFTH3
DFTH4
DFTH5
DFTH6
outputs
Every instruction can write in any memory location
High synchronization activity
Coherency needed on multicores or DSMs
1 single instructions failing → the whole system to fails
Regularization of data exchange
Less synchronization activity
No coherency needed
Isolation of thread code
Idempotency property (more resilience, lighter checkpointing)
Scalability, Parallelism
Fault-tolerance, Security

**Figure 2:** How DF-Threads work (simplified overview).

## 3. Preliminary Evaluation

### 3.1. Methodology

To show the potential of DF-Threads execution we compare here the execution time in case of a simple benchmark with OpenMPI [21]. The evaluation is based on the HP-Labs COTSon[1] simulator [22], an X86_64 full-system simulator, which also accounts for OS effects. Key parameters for the modeled cores are detailed in Table 1. Furthermore, the simulator has been extended to support DF-Threads [11], including modeling a Distributed Thread Scheduler [23].

Table 1: Multicore architectural parameters.

| Parameter | Description |
|---|---|
| SoC | single-core connected by a shared-bus, IO-hub, MC, high-speed transceivers |
| Core | 3GHz, in-order superscalar |
| Branch Predictor | two-level (history length=14bits, pattern-history table=16kB, 8-cycle missprediction penalty) |
| L1 Cache | Private I-cache 32 KB, 4 ways, 2-cycle latency - private D-cache 32 KB, 2 ways, 3-cycle latency |
| L2 Cache | Private 256 KB, 4 ways, 5-cycle latency |
| L3 Cache | Shared 4GB, 4 ways, 20-cycle latency |
| Coherence protocol | MOESI |
| Main Memory | 4 GB, 100 cycles latency |
| I-L1-TLB, D-L1-TLB | 64 entries, full-associative, 1-cycle latency |
| L2-TLB | 512 entries, direct access, 1-cycle latency |
| Write/Read queues | 200 Bytes each, 1-cycle latency |

### 3.2. Matrix Multiplication Benchmark

For the initial tests, we selected the Matrix Multiplication kernel. The Matrix Multiplication benchmark has the following characteristics: blocked matrix multiplication using the classical 3 nested loops algorithm; matrices [2] of size $n \times n$, where $n = 216, 432, 864$; block size $b = 8$.

[1]Please note that the COTSon simulator is open-source: https://cotson.sf.net and other related open-source software is also available at https://download.axiom-project.eu

[2]Please note that even if this matrix sizes may seem small, they cause a quite large simulation time (in terms of hours or days in case of power estimation). Therefore, our focus is to derive the main properties of the framework while suggesting future

The input matrices' sizes are chosen to avoid particular multiples of powers of 2 to prevent excessive cache conflicts that might skew the evaluation of the system's basic behavior. The threads in each test case are generated so that each thread performs the dot-products of each block, thus the expected number of threads is $n/b$.

In the benchmark, we focus on the computation region of interest, excluding the data preparation and result verification from the evaluation. Additionally, any I/O messages (e.g., 'printf') are removed from the computational part. Consequently, any OS-related activity pertains only to managing the data needed for computation or moved across nodes.

For DF-Threads, the kernel activity is mostly under 10% (except in the case of 16 nodes, where the number of threads $n/b$ is too low, resulting in an imbalance).

### 3.3. DF-Threads versus OpenMPI

In OpenMPI, the workload is distributed among the available worker threads, even in a single-node configuration, which incurs a greater overhead compared to DF-Threads. A direct comparison between OpenMPI and DF-Threads is provided in Fig. 3, where it is evident that:

- OpenMPI slightly benefits from local cores.
- DF-Threads scales well with both the number of cores and the number of nodes, achieving an advantage of about 28x compared to the execution OpenMPI on the same number of nodes for n=216. This is due to the good performance and scaling of DF-Threads as well as the relatively poor performance of OpenMPI for this input size.

For an input size of 864, DF-Threads still shows a significant advantage, about 3.5x over OpenMPI on the same number of nodes, confirming DF-Threads' competitive edge. When comparing a system with 8 nodes and 4 cores per node, DF-Threads achieve a speedup of 14x over OpenMPI (not shown in the figure). The diminishing execution time advantage of DF-Threads vs. OpenMPI highlights a large advantage for DF-Threads in case of smaller granularity. However, our preliminary results confirm that when combined with the power consumption evaluation, the DF-Threads offer a greater advantage also as the number of nodes increases.

### 3.4. FastFlow versus OpenMPI

While FastFlow was originally designed for support shared-memory application running on multicores, the distributed version of FastFlow currently optionally uses the OpenMPI backend. Furthermore, the shared-memory version defaults to using non-blocking concurrency control mode, while the distributed version employs blocking mode for its runtime system.

FastFlow supports various parallel programming paradigms, and matrix multiplication can be implemented using different patterns such as pipelines or task farms. While the framework primarily focuses on shared-memory parallelism, it also supports distributed memory systems using extensions like *FastFlow-DM*.

For distributed systems, leveraging OpenMPI alongside FastFlow can provide an efficient solution. FastFlow's high-level parallel constructs simplify the development process while maintaining performance. Previous experiments on FastFlow targeting distributed systems show that there is a substantial overhead in using MPI based primitives [24]. Therefore, DF-Threads can offer a good opportunity for enhancing the performance of a parallel application, while relying and skeleton, parallel patterns and building blocks offered by FastFlow.

engineering work.

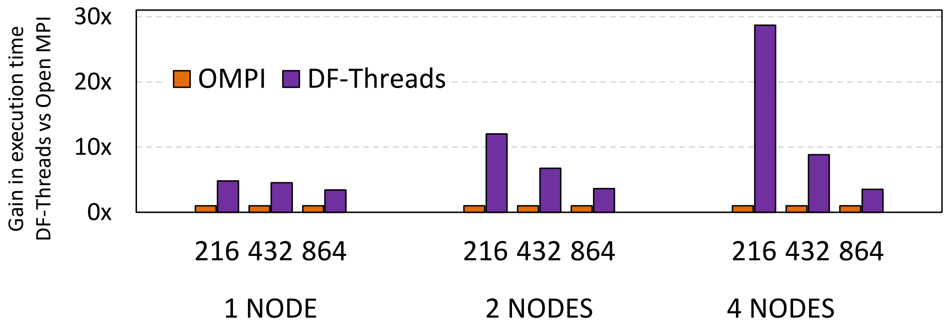

**Figure 3:** (Data adapted from [4]) Gain in execution time of DF-Threads compared to Open MPI (normalized to 1). The benchmark is Blocked Matrix Multiplication for different sizes of the square matrices (216, 432, 864 – the block size is 8 elements) and 1, 2, 4 nodes. FULL-SYSTEM simulation.

### 3.5. Power Savings

The power consumption estimation is also based on the COTSon framework via the MCPAT utility. In the preliminary experiments, with the matrix size $n = 216$ we have measured a consistent power saving when using DF-Threads (Tab.2) of a factor of about 2.7x.

Table 2: Power Consumption of DF-Threads versus OpenMPI for the matrix size $n = 216$, 1 node, 1 core.

| OpenMPI | DF-Threads |
|---|---|
| 0.5115 W | 0.1867W |

## 4. Conclusions

In this paper we analyzed the potentials offered by using a tandem approach based on FastFlow for the high-level programming and on DF-Threads for the underlying execution model. Based on OpenMPI as a common reference for evaluating this potential of improvement, we expect a considerable benefit for both extending FastFlow and DF-Threads. The future work will include a prototype system for demonstrating the combined performance on a set of parallel applications such as P$^3$ARSEC suite [25].

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