David M. Brooks

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Education

Princeton University. Doctor of Philosophy in Electrical Engineering, 2001.

Princeton University. Master of Arts in Electrical Engineering, 1999.

University of Southern California. Bachelor of Science in Electrical Engineering, 1997.

Academic and Professional Experience

Haley Family Professor of Computer Science, School of Engineering and Applied Sciences, Harvard University (March 2014–Present).

Visiting Research Scientist, Facebook Artificial Intelligence Research (SysML Group) (June 2021–June 2023)

Visiting Research Scientist, Facebook Artificial Intelligence Infrastructure Group (July 2017–July 2020)

Gordon McKay Professor of Computer Science, School of Engineering and Applied Sciences, Harvard University (July 2009–February 2014).

John L. Loeb Associate Professor of the Natural Sciences, School of Engineering and Applied Sciences, Harvard University (July 2007–June 2009).

Associate Professor of Computer Science, School of Engineering and Applied Sciences, Harvard University (July 2006–June 2009).

Assistant Professor of Computer Science, Division of Engineering and Applied Sciences, Harvard University (September 2002-July 2006).

Research Staff Member, IBM T.J. Watson Research Center, (September 2001–September 2002).

Research Assistant, Princeton University, (July 1997–September 2001).

Research Intern, IBM T.J. Watson Research Center, (June 2000–September 2000).

Research Intern, Intel Corporation, (June 1999–September 1999).

Honors and Awards

Three papers were selected for inclusion in ISCA-50 25-Year Retrospective: 1996-2020: a collection of significant and often memorable papers from 1996 through 2020 from the International Symposium on Computer Architecture.

Best Paper Award, IEEE/ACM International Symposium on Networks on Chip, 2023.

Best Paper Award from IEEE Micro, 2022.

HPCA Test of Time Award, 2021.

Elected Fellow of the ACM, 2020.

Best Paper Award, Design Automation Conference, 2020.

HPCA Test of Time Award, 2018.

Elected Fellow of the IEEE, 2016.

ISCA Test of Time Award, 2015.

Best Paper Award, International Conference on Computer Design, 2014

IEEE ISLPED Design Contest Award, 2013.

ACM Maurice Wilkes Award, 2012.

Papers selected for IEEE Micro's "Top Picks in Computer Architecture" special issue for papers published in 2005, 2007, 2008, 2009, 2010, 2014, 2015, 2021, and 2022.

Papers selected as an Honorable Mention for IEEE Micro's "Top Picks in Computer Architecture" special issue for papers published in 2014, 2020, 2021, 2022, and 2023.

Best Paper Award, International Symposium on High-Performance Computer Architecture, 2009.

DARPA/MTO Young Faculty Award, 2007.

1st Prize, Phase 2 of SRC SoC Design Challenge, October, 2006.

2nd Prize, Phase 1 of SRC SoC Design Challenge, October, 2005.

Best Paper Award, International Symposium on Microarchitecture, 2005.

National Science Foundation CAREER Award, February, 2005.

IBM Faculty Partnership Award, 2004–2005.

MICRO 2002 paper selected as one of the four Best IBM Research Papers in Computer Science, Electrical Engineering and Math published in 2002.

National Science Foundation Graduate Research Fellow, 1998-2001.

Princeton University Gordon Wu Graduate Fellow, 1997-2001.

University of Southern California Trustee Scholar, 1993-1997.

Refereed Conference Publications

Alicia Golden, Samuel Hsia, Fei Sun, Bilge Acun, Basil Hosmer, Yejin Lee, Zachary DeVito, Jeff Johnson, Gu-Yeon Wei, David Brooks, Carole-Jean Wu. "Generative AI Beyond LLMs: System Implications of Multi-Modal Generation", *International Symposium on Performance Analysis of Systems and Software (ISPASS)*, May, 2024.

Maximilian Lam, Jeff Johnson, Wenjie Xiong, Kiwan Maeng, Udit Gupta, Minsoo Rhu, Hsien-Hsin S Lee, Vijay Janapa Reddi, Gu-Yeon Wei, David Brooks, Edward Suh. "GPU-based Private Information Retrieval for On-Device Machine Learning Inference", *ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, April, 2024.

Celine Lee, Abdulrahman Mahmoud, Michal Kurek, Simone Campanoni, David Brooks, Stephen Chong, Gu-Yeon Wei, Alexander M Rush. "Guess & Sketch: Language Model Guided Transpilation", *International Conference on Learning Representations (ICLR)*, May, 2024.

Sai Qian Zhang, Thierry Tambe, Nestor Cuevas, Gu-Yeon Wei, David Brooks. "CAMEL: Co-Designing AI Models and Embedded DRAMs for Efficient On-Device Learning", *International Symposium on High-Performance Computer Architecture (HPCA)*, March, 2024.

Maico Cassel dos Santos, Tianyu Jia, Joseph Zuckerman, Martin Cochet, Davide Giri, Erik J. Loscalzo, Karthik V Swaminathan, Thierry Tambe, Jeff Jun Zhang, Alper Buyuktosunoglu, Kuan-Lin Chiu, Giuseppe Di Guglielmo, Paolo Mantovani, Luca Piccolboni, Gabriele Tombesi, David Trilla, John-David Wellman, En-Yu Yang, Aporva Amarnath, Ying Jing, Bhoopesh Mishra, Joshua Park, Vinayaka Suresh, Adve Adve, Pradip Bose, David Brooks, Luca P. Carloni, Kenneth L. Shepard, and Gu-Yeon Wei. "A 12nm Linux-SMP-Capable RISC-V SoC with 14 Accelerator Types, Distributed Hardware Power Management, and Flexible NoC-Based Data Orchestration," *IEEE International Solid-State Circuits Conference (ISSCC)*, February, 2024.

Yunho Jin, Chun-Feng Wu, David Brooks, Gu-Yeon Wei. "S^3: Increasing GPU Utilization during Generative Inference for Higher Throughput," *Conference on Neural Information Processing Systems (NeurIPS)*, December, 2023.

Syed Talal Wasim, Kabila Haile Saboka, Abdulrahman Mahmoud, Salman Khan, David Brooks, Gu-Yeon Wei. "Hardware Resilience Properties of Text-Guided Image Classifiers", *Conference on Neural Information Processing Systems (NeurIPS)*, December, 2023.

Samuel Hsia, Udit Gupta, Bilge Acun, Newsha Ardalani, Pan Zhong, Gu-Yeon Wei, David Brooks, and Carole-Jean Wu. "MP-Rec: Hardware-Software Co-design to Enable Multi-path Recommendation," *International Conference on Architectural Support for Programming Languages and Operating System (ASPLOS)*, March, 2023. **Selected as an Honorable Mention for the Top Picks in Computer Architecture in 2023.**

Bilge Acun, Benjamin Lee, Fiodar Kazhamiaka, Kiwan Maeng, Udit Gupta, Manoj Chakkaravarthy, David Brooks, and Carole-Jean Wu. "Carbon Explorer: A Holistic Framework for Designing Carbon Aware Datacenters," *International Conference on Architectural Support for Programming Languages and Operating System (ASPLOS)*, March, 2023. **Selected as an Honorable Mention for the Top Picks in Computer Architecture in 2023.**

Alexander Hankin, Abdulrahman Mahmoud, Mark Hempstead, David Brooks, Gu-Yeon Wei. "VelociTI: An Architecture-level Performance Modeling Framework for Trapped Ion Quantum Computers," *IEEE International Symposium on Workload Characterization (IISWC)*, October, 2023.

Matthew Joseph Adiletta, Jesmin Jahan Tithi, Emmanouil-Ioannis Farsarakis, Gerasimos Gerogiannis, Robert Adolf, Robert Benke, Sidharth Kashyap, Samuel Hsia, Kartik Lakhotia, Fabrizio Petrini, Gu-Yeon Wei, David Brooks. "Characterizing the Scalability of Graph Convolutional Networks on Intel PIUMA", *IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, April, 2023.

Alexander Hankin, Lillian Pentecost, Dongmoon Min, David Brooks, Gu-Yeon Wei. "Is the Future Cold or Tall? Design Space Exploration of Cryogenic and 3D Embedded Cache Memory", *IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, April, 2023.

Yu-Shun Hsiao, Zishen Wan, Tianyu Jia, Radhika Ghosal, Abdulrahman Mahmoud, Arijit Raychowdhury, David Brooks, Gu-Yeon Wei, Vijay Janapa Reddi. "Mavfi: An end-to-end fault analysis framework with anomaly detection and recovery for micro aerial vehicles", *Design, Automation Test in Europe Conference Exhibition (DATE)*, April, 2023.

Thierry Tambe, Jeff Zhang, Coleman Hooper, Tianyu Jia, Paul N Whatmough, Joseph Zuckerman, Maico Cassel Dos Santos, Erik Jens Loscalzo, Davide Giri, Kenneth Shepard, Luca Carloni, Alexander Rush, David Brooks, and Gu-Yeon Wei. "A 12nm 18.1 TFLOPs/W Sparse Transformer Processor with Entropy-Based Early Exit, Mixed-Precision Predication and Fine-Grained Power Management," *International Solid-State Circuits Conferences (ISSCC)*, February, 2023.

Maico Cassel dos Santos ,Tianyu Jia ,Martin Cochet, Karthik Swaminathan, Joseph Zuckerman, Paolo Mantovani, Davide Giri, Jeff Jun Zhang, Erik Jens Loscalzo, Gabriele Tombesi, Kevin Tien, Nandhini Chandramoorthy, John-David Wellman, David Brooks, Gu-Yeon Wei, Kenneth Shepard, Luca P. Carloni, and Pradip Bose. "A Scalable Methodology for Agile Chip Development with Open-Source Hardware Components," Proceedings of the IEEE International Conference on Computer-Aided Design (ICCAD), November, 2022.

Srivatsan Krishnan, Zishen Wan, Kshitij Bhardwaj, Paul Whatmough, Aleksandra Faust, Sabrina Neuman, Gu-Yeon Wei, David Brooks, and Vijay Janapa Reddi. "Automatic Domain-Specific SoC Design for Autonomous Unmanned Aerial Vehicles," *International Symposium on Microarchitecture*, October, 2022. **Selected as an Honorable Mention for the Top Picks in Computer Architecture in 2022.**

Tianyu Jia, Paolo Mantovani, Maico Cassel Dos Santos, Davide Giri, Joseph Zuckerman, Erik Jens Loscalzo, Martin Cochet, Karthik Swaminathan, Gabriele Tombesi, Jeff Jun Zhang, Nandhini Chandramoorthy, John-David Wellman, Kevin Tien, Luca Carloni, Kenneth Shepard, David Brooks, Gu-Yeon Wei, and Pradip Bose. "A 12nm Agile-Designed SoC for Swarm-Based Perception with Heterogeneous IP Blocks, a Reconfigurable Memory Hierarchy, and an 800MHz Multi-Plane NoC," *European Solid State Circuits Conference (ESSCIRC)*, September, 2022.

Chun-Feng Wu, Carole-Jean Wu, Gu-Yeon Wei, and David Brooks. "A joint management middleware to improve training performance of deep recommendation systems with SSDs," *ACM/IEEE Design Automation Conference (DAC)*, July, 2022.

Udit Gupta, Mariam Elgamal, Gage Hills, Gu-Yeon Wei, Hsien-Hsin S. Lee, David Brooks, and Carole-Jean Wu. "ACT: Designing Sustainable Computer Systems With An Architectural Carbon Modeling Tool," *International Symposium on Computer Architecture (ISCA)*, June, 2022. **Selected as one of the Top Picks in Computer Architecture in 2022.**

Cheng Tan, Thierry Tambe, Jeff Zhang, Bo Fang, Tong Geng, Gu-Yeon Wei, David Brooks, Antonino Tumeo, Ganesh Gopalakrishnan, Ang Li. "ASAP: automatic synthesis of area-efficient and precision-aware CGRAs," *ACM International Conference on Supercomputing*, June, 2022.

Abdulrahman Mahmoud, Thierry Tambe, Tarek Aloui, David Brooks, and Gu-Yeon Wei. "GoldenEye: A Platform for Evaluating Emerging Data Formats in DNN Accelerators," *IEEE/IFIP International Conference on Dependable Systems and Networks (DSN)*, June, 2022.

Carole-Jean Wu, Ramya Raghavendra, Udit Gupta, Bilge Acun, Newsha Ardalani, Kiwan Maeng, Gloria Chang, Fiona Aga Behram, James Huang, Charles Bai, Michael Gschwind, Anurag Gupta, Myle Ott, Anastasia Melnikov, Salvatore Candido, David Brooks, Geeta Chauhan, Benjamin Lee, Hsien-Hsin S Lee, Bugra Akyildiz, Maximilian Balandat, Joe Spisak, Ravi Jain, Mike Rabbat, Kim Hazelwood. "Sustainable ai: Environmental implications, challenges and opportunities," *Conference on Machine Learning and Systems (MLSys)*, March, 2022.

Lillian Pentecost, Alexander Hankin, Marco Donato, Mark Hempstead, Gu-Yeon Wei, and David Brooks. "NVMExplorer: A Framework for Cross-Stack Comparisons of Embedded Non-Volatile Memories," *IEEE International Symposium on High-Performance Computer Architecture*, February, 2022.

Yuji Chai, Glenn G. Ko, Mark Ting, Luke Bailey, David Brooks, and Gu-Yeon Wei. "CoopMC: Algorithm-Architecture Co-Optimization for Markov Chain Monte Carlo Accelerators," *IEEE International Symposium on High-Performance Computer Architecture*, February, 2022.

Udit Gupta, Samuel Hsia, Jeff Zhang, Mark Wilkening, Javin Pombra, Hsien-Hsin S. Lee, Gu-Yeon Wei, Carole-Jean Wu, and David Brooks. "RecPipe: Co-designing Models and Hardware to Jointly Optimize Recommendation Quality and Performance," *International Symposium on Microarchitecture*, October, 2021.

Thierry Tambe, Coleman Hooper, Lillian Pentecost, Tianyu Jia, En-Yu Yang, Marco Donato, Victor Sanh, Paul Whatmough, Alexander M Rush, David Brooks, and Gu-Yeon Wei. "Edgebert: Sentence-level energy optimizations for latency-aware multi-task NLP inference," *International Symposium on Microarchitecture*, October, 2021.

Mohammad Mehdi Sharifi, Lillian Pentecost, Ramin Rajaei, Arman Kazemi, Qiuwen Lou, Gu-Yeon Wei, David Brooks, Kai Ni, X Sharon Hu, Michael Niemier, Marco Donato. "Application-driven Design Exploration for Dense Ferroelectric Embedded Non-volatile Memories," *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, August, 2021.

Thierry Tambe, En-Yu Yang, Glenn G Ko, Yuji Chai, Coleman Hooper, Marco Donato, Paul N Whatmough, Alexander M Rush, David Brooks, Gu-Yeon Wei. "SM6: A 16nm System-on-Chip for Accurate and Noise-Robust Attention-Based NLP Applications," *Hot Chips 30: A Symposium on High Performance Chips*, August, 2021.

En-Yu Yang, Tianyu Jia, David Brooks, Gu-Yeon Wei. "FlexACC: A Programmable Accelerator with Application-Specific ISA for Flexible Deep Neural Network Inference," *International Conference on Application-specific Systems, Architectures and Processors*, July, 2021.

Jeff Jun Zhang, Nicolas Bohm Agostini, Shihao Song, Cheng Tan, Ankur Limaye, Vinay Amatya, Joseph Manzano, Marco Minutoli, Vito Giovanni Castellana, Antonino Tumeo, Gu-Yeon Wei, David Brooks. "Towards Automatic and Agile AI/ML Accelerator Design with End-to-End Synthesis," *International Conference on Application-specific Systems, Architectures and Processors*, July, 2021.

Maximilian Lam, Gu-Yeon Wei, David Brooks, Vijay Janapa Reddi, and Michael Mitzenmacher. "Gradient Disaggregation: Breaking Privacy in Federated Learning by Reconstructing the User Participant Matrix," *International Conference on Machine Learning*, July, 2021.

Mark Wilkening, Udit Gupta, Samuel Hsia, Caroline Trippel, Carole-Jean Wu, David Brooks, and Gu-Yeon Wei. "RecSSD: Near Data Processing for Solid State Drive Based Recommendation Inference," *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, April, 2021.

Brandon Reagen, Wooseok Choi, Yeongil Ko, Vincent Lee, Gu-Yeon Wei, Hsien-Hsin S Lee, David Brooks. "Cheetah: Optimizing and Accelerating Homomorphic Encryption for Private Inference," *IEEE International Symposium on High-Performance Computer Architecture*, February, 2021. **Selected as an Honorable Mention for the Top Picks in Computer Architecture in 2021.**

Thierry Tambe, En-Yu Yang, Glenn G. Ko, Yuji Chai, Coleman Hooper, Marco Donato, Paul N. Whatmough, Alexander M. Rush, David Brooks, and Gu-Yeon Wei. "A 25mm2 SoC for IoT Devices with 18ms Noise-Robust Speech-to-Text Latency via Bayesian Speech Denoising and Attention-Based Sequence-to-Sequence DNN Speech Recognition in 16nm FinFET," *International Solid-State Circuits Conferences (ISSCC)*, February, 2021.

Udit Gupta, Young Geun Kim, Sylvia Lee, Jordan Tse, Hsien-Hsin S Lee, Gu-Yeon Wei, David Brooks, Carole-Jean Wu. "Chasing Carbon: The Elusive Environmental Footprint of Computing," *IEEE International Symposium on High-Performance Computer Architecture*, February, 2021. **Selected as one of the Top Picks in Computer Architecture in 2021.**

Samuel Hsia, Udit Gupta, Mark Wilkening, Carole-Jean Wu, Gu-Yeon Wei, David Brooks. "Cross-Stack Workload Characterization of Deep Recommendation Systems," *IEEE International Symposium on Workload Characterization*, October, 2020.

Kshitij Bhardwaj, Marton Havasi, Yuan Yao, David Brooks, Jos Miguel Hernndez-Lobato, Gu-Yeon Wei. "A comprehensive methodology to determine optimal coherence interfaces for many-accelerator SoCs," *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, August, 2020.

Glenn G. Ko, Yuji Chai, Marco Donato, Paul N. Whatmough, Thierry Tambe, Rob A. Rutenbar, David Brooks, Gu-Yeon Wei. "A Scalable Bayesian Inference Accelerator for Unsupervised Learning Conference," *IEEE Hot Chips Symposium*, August, 2020.

Thierry Tambe, En-Yu Yang, Zishen Wan, Yuntian Deng, Vijay Janapa Reddi, Alexander M. Rush, David Brooks, Gu-Yeon Wei. "Algorithm-Hardware Co-Design of Adaptive Floating-Point Encodings for Resilient Deep Learning Inference," *Design Automation Conference (DAC)*, July, 2020. **Best Paper Award.**

Udit Gupta, Samuel Hsia, Vikram Saraph, Xiaodong Wang, Brandon Reagen, Gu-Yeon Wei, Hsien-Hsin S. Lee, David Brooks, Carole-Jean Wu. "DeepRecSys: A System for Optimizing End-To-End At-scale Neural Recommendation Inference Conference," *International Symposium on Computer Architecture (ISCA)*, June, 2020.

Liu Ke, Udit Gupta, Carole-Jean Wu, Benjamin Youngjae Cho, Mark Hempstead, Brandon Reagen, Xuan Zhang, David Brooks, Vikas Chandra, Utku Diril, Amin Firoozshahian, Kim Hazelwood, Bill Jia, Hsien-Hsin S. Lee, Meng Li, Bert Maher, Dheevatsa Mudigere, Maxim Naumov, Martin Schatz, Mikhail Smelyanskiy, Xiaodong Wang. "RecNMP: Accelerating Personalized Recommendation with Near-Memory Processing Conference," *International Symposium on Computer Architecture (ISCA)*, June, 2020.

Glenn G. Ko, Yuji Chai, Marco Donato, Paul N. Whatmough, Thierry Tambe, Rob A. Rutenbar, David Brooks, Gu-Yeon Wei. "A 3mm2 Programmable Bayesian Inference Accelerator for Unsupervised Machine Perception using Parallel Gibbs Sampling in 16nm," *IEEE Symposium on VLSI Circuits*, June, 2020.

Yu Emma Wang, Gu-Yeon Wei, David Brooks. "A Systematic Methodology for Analysis of Deep Learning Hardware and Software Platforms," *Third Conference on Machine Learning and Systems*

(MLSys), March, 2020.

Peter Mattson, Christine Cheng, Cody Coleman, Greg Diamos, Paulius Micikevicius, David Patterson, Hanlin Tang, Gu-Yeon Wei, Peter Bailis, Victor Bittorf, David Brooks, Dehao Chen, Debojyoti Dutta, Udit Gupta, Kim Hazelwood, Andrew Hock, Xinyuan Huang, Bill Jia, Daniel Kang, David Kanter, Naveen Kumar, Jeffery Liao, Deepak Narayanan, Tayo Oguntebi, Gennady Pekhimenko, Lillian Pentecost, Vijay Janapa Reddi, Taylor Robie, Tom St John, Carole-Jean Wu, Lingjie Xu, Cliff Young, Matei Zaharia. "MLPerf Training Benchmark," *Third Conference on Machine Learning and Systems (MLSys)*, March, 2020.

Udit Gupta, Carole-Jean Wu, Xiaodong Wang, Maxim Naumov, Brandon Reagen, David Brooks, Bradford Cottel, Kim Hazelwood, Bill Jia, Hsien-Hsin S. Lee, Andrey Malevich, Dheevatsa Mudigere, Mikhail Smelyanskiy, Liang Xiong, Xuan Zhang. "The Architectural Implications of Facebook's DNN-based Personalized Recommendation," *IEEE International Symposium on High-Performance Computer Architecture*, February, 2020. **Selected as an Honorable Mention for the Top Picks in Computer Architecture in 2020.**

Lillian Pentecost, Marco Donato, Brandon Reagen, Udit Gupta, Siming Ma, Gu-Yeon Wei, David Brooks. "MaxNVM: Maximizing DNN Storage Density and Inference Efficiency with Sparse Encoding and Error Mitigation," *International Symposium on Microarchitecture*, October, 2019.

Udit Gupta, Brandon Reagen, Lillian Pentecost, Marco Donato, Thierry Tambe, Alexander M Rush, Gu-Yeon Wei, David Brooks. "MASR: A Modular Accelerator for Sparse RNNs," *International Conference on Parallel Architectures and Compilation Techniques*, September, 2019. **Nominated for Best Paper Award.**

Glenn G Ko, Yuji Chai, Rob A Rutenbar, David Brooks, Gu-Yeon Wei, "Accelerating Bayesian Inference on Structured Graphs Using Parallel Gibbs Sampling," *International Conference on Field Programmable Logic and Applications*, September, 2019.

Brian Plancher, Camelia D. Brumar, Iulian Brumar, Lillian Pentecost, Saketh Rama, David Brooks, "Application of Approximate Matrix Multiplication to Neural Networks and Distributed SLAM," *IEEE High Performance Extreme Computing Conference (HPEC)*, September, 2019.

Paul N Whatmough, Sae Kyu Lee, Marco Donato, Hsea-Ching Hsueh, Sam Likun Xi, Udit Gupta, Lillian Pentecost, Glenn G Ko, David Brooks, Gu-Yeon Wei. "A 16nm 25mm2 SoC with a 54.5x Flexibility-Efficiency Range from Dual-Core Arm Cortex-A53 to eFPGA and Cache-Coherent Accelerators," *Symposium on VLSI Circuits*, June, 2019.

Yu Emma Wang, Yuhao Zhu, Glenn G Ko, Brandon Reagen, Gu-Yeon Wei, David Brooks. "Demystifying Bayesian Inference Workloads," *IEEE International Symposium on Performance Analysis of Systems and Software*, March, 2019.

Carole-Jean Wu, David Brooks, Kevin Chen, Douglas Chen, Sy Choudhury, Marat Dukhan, Kim Hazelwood, Eldad Isaac, Yangqing Jia, Bill Jia, Tommer Leyvand, Hao Lu, Yang Lu, Lin Qiao, Brandon Reagen, Joe Spisak, Fei Sun, Andrew Tulloch, Peter Vajda, Xiaodong Wang, Yanghan Wang, Bram Wasti, Yiming Wu, Ran Xian, Sungjoo Yoo, Peizhao Zhang. "Machine Learning at Facebook: Understanding Inference at the Edge," *International Symposium on High-Performance Computer Architecture*, February, 2019.

Sae Kyu Lee, Paul Whatmough, Niamh Mulholland, Patrick Hansen, David Brooks, Gu-Yeon Wei. "A Wide Dynamic Range Sparse FC-DNN Processor with Multi-Cycle Banked SRAM Read and Adaptive Clocking in 16nm FinFET," *European Solid State Circuits Conference (ESSCIRC)*, September, 2018.

Paul Whatmough, Sae Kyu Lee, Sam Xi, Udit Gupta, Lillian Pentecost, Marco Donato, Hsea-Ching Hseuh, David Brooks, Gu-Yeon Wei. "SMIV: A 16nm SoC with Efficient and Flexible DNN Acceleration for Intelligent IoT Devices," *Hot Chips 30: A Symposium on High Performance Chips*, August, 2018.

Brandon Reagen, Udit Gupta, Robert Adolf, Michael Mitzenmacher, Alexander Rush, Gu-Yeon Wei, David Brooks. "Weightless: Lossy Weight Encoding For Deep Neural Network Compression,"

International Conference on Machine Learning, July, 2018.

Brandon Reagen, Udit Gupta, Lillian Pentecost, Paul N. Whatmough, Sae Kyu Lee, Niamh Mulholland, Gu-Yeon Wei, and David Brooks. "Ares: A Framework for Quantifying the Resilience of Deep Neural Networks," *Design Automation Conference (DAC)*, June, 2018. **Nominated for Best Paper Award.**

Marco Donato, Brandon Reagen, Lillian Pentecost, Udit Gupta, David Brooks, and Gu-Yeon Wei. "On-Chip Deep Neural Network Storage with Multi-Level eNVM," *Design Automation Conference (DAC)*, June, 2018.

Kim Hazelwood, Sarah Bird, David Brooks, Soumith Chintala, Utku Diril, Dmytro Dzhulgakov, Mohamed Fawzy, Bill Jia, Yangqing Jia, Aditya Kalro, James Law, Kevin Lee, Jason Lu, Pieter Noordhuis, Misha Smelyanskiy, Liang Xiong, and Xiaodong Wang. "Applied Machine Learning at Facebook: A Datacenter Infrastructure Perspective," *International Symposium on High-Performance Computer Architecture*, February, 2018.

Paul Whatmough, Saekyu Lee, Niamh Mulholland, Patrick Hansen, Sreela Kodali, David Brooks, and Gu-Yeon Wei. "DNN ENGINE: A 16nm Sub-uJ Deep Neural Network Inference Accelerator for the Embedded Masses," *Hot Chips 29: A Symposium on High Performance Chips*, August, 2017.

Brandon Reagen, Jose Miguel Hernandez-Lobato, Robert Adolf, Michael Gelbart, Paul Whatmough, Gu-Yeon Wei, and David Brooks. "A case for efficient accelerator design space exploration via Bayesian optimization," *International Symposium on Low Power Electronics and Design (ISLPED)*, August, 2017.

An Zou, Jingwen Leng, Yazhou Zu, Tao Tong, Vijay Janapa Reddi, David Brooks, Gu-Yeon Wei, and Xuan Zhang. "Ivory: Early-stage design space exploration tool for integrated voltage regulators," *Design Automation Conference*, June, 2017.

Rafael Garibotti, Brandon Reagen, Yakun Sophia Shao, Gu-Yeon Wei, and David Brooks. "Using dynamic dependence analysis to improve the quality of high-level synthesis designs," *IEEE International Symposium on Circuits and Systems (ISCAS)*, May, 2017.

Svilen Kanev, Sam Likun Xi, Gu-Yeon Wei, and David Brooks. "Mallacc: Accelerating memory allocation," *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, April, 2017.

Paul Whatmough, Sae-kyu Lee, Hyunkwang Lee, Saketh Rama, David Brooks, and Gu-Yeon Wei. "A 28nm SoC with a 1.2GHz 568nJ/Prediction Sparse Deep-Neural-Network Engine with >0.1 Timing Error Rate Tolerance for IoT Applications," *International Solid-State Circuits Conferences (ISSCC)*, February, 2017.

Simon Chaput, David Brooks, and Gu-Yeon Wei. "A 3-to-5V Input $100V_{pp}$ Output 57.7mW 0.42% THD+N Highly Integrated Piezoelectric Actuator Driver," *International Solid-State Circuits Conferences (ISSCC)*, February, 2017.

Yakun Sophia Shao, Sam Xi, Viji Srinivasan, Gu-Yeon Wei, and David Brooks. "Co-Designing Accelerators and SoC Interfaces using gem5-Aladdin," *International Symposium on Microarchitecture (MICRO)*, October, 2016.

Robert Adolf, Saketh Rama, Brandon Reagen, Gu-Yeon Wei, David Brooks. "Fathom: Reference Workloads for Modern Deep Learning Methods," *IEEE International Symposium on Workload Characterization (IISWC)*, September, 2016.

Brandon Reagen, Paul Whatmough, Robert Adolf, Saketh Rama, Hyunkwang Lee, Sae Kyu Lee, Jos Miguel Hernndez-Lobato, Gu-Yeon Wei, and David Brooks. "Minerva: Enabling Low-Power, Highly-Accurate Deep Neural Network Accelerators," *International Symposium on Computer Architecture (ISCA)*, June, 2016.

Mario Lok, Xuan Zhang, Elizabeth Farrell Helbling, Robert Wood, David Brooks, and Gu-Yeon Wei. "A power electronics unit to drive piezoelectric actuators for flying microrobots," *IEEE Custom Integrated Circuits Conference (CICC)*, September, 2015.

Xuan Zhang, Mario Lok, Tao Tong, Simon Chaput, Sae Kyu Lee, Brandon Reagen, Hyunkwang Lee, David Brooks, and Gu-Yeon Wei. "A Multi-Chip System Optimized for Insect-Scale Flapping-Wing Robots," *IEEE Symposium on VLSI Circuits (VLSIC)*, June, 2015.

Sae Kyu Lee, Tao Tong, Xuang Zhang, David Brooks, Gu-Yeon Wei. "A 16-Core Voltage-Stacked System with an Integrated Switched-Capacitor DC-DC Converter," *IEEE Symposium on VLSI Circuits (VLSIC)*, June, 2015.

Svilen Kanev, Juan Pablo Darago, Kim Hazelwood, Parthasarathy Ranganathan, Tipp Moseley, Gu-Yeon Wei, and David Brooks. "Profiling a Warehouse-Scale Computer," *International Symposium on Computer Architecture (ISCA)*, June, 2015. **Selected as one of the Top Picks in Computer Architecture in 2015.**

Sam Xi, Hans Jacobson, Pradip Bose, Gu-Yeon Wei, and David Brooks."Quantifying Sources of Error in McPAT and Potential Impacts on Architectural Studies," *International Symposium on High-Performance Computer Architecture (HPCA)*, February, 2015.

Simone Campanoni, Glenn Holloway, Gu-Yeon Wei, and David Brooks,"HELIX-UP: Relaxing Program Semantics to Unleash Parallelization," *International Symposium on Code Generation and Optimization (CGO)*, February, 2015. **Nominated for Best Paper Award.**

Michael Lyons, Gu-Yeon Wei, and David Brooks. "Multi-Accelerator System Development With The ShrinkFit Acceleration Framework," *International Conference on Computer Design (ICCD)*, October, 2014. **Received Best Paper Award.**

Yakun Sophia Shao, Brandon Reagen, Gu-Yeon Wei and David Brooks. "Aladdin: A Pre-RTL, Power-Performance Accelerator Simulator Enabling Large Design Space Exploration of Customized Architectures," *International Symposium on Computer Architecture (ISCA)*, June, 2014. **Selected as one of the Top Picks in Computer Architecture in 2014.**

Simone Campanoni, Kevin Brownell, Svilen Kanev, Timothy M. Jones, Gu-Yeon Wei, and David Brooks. "HELIX-RC: An Architecture-Compiler Co-Design for Automatic Parallelization of Irregular Programs," *International Symposium on Computer Architecture (ISCA)*, June, 2014. **Selected as an Honorable Mention for the Top Picks in Computer in 2014.**

Pradip Bose, David Brooks, Subhasish Mitra, Karthick Rajamani, Mircea Stan, Kevin Skadron, Gu-Yeon Wei, "Cross-Layer Modeling Framework for Energy-Efficient Resilience," *39th Annual GOMACTech Conference*, April, 2014.

Xuan Zhang, David Brooks, and Gu-Yeon Wei. "A 20μW 10MHz Relaxation Oscillator with Adaptive Bias and Fast Self-Calibration in 40nm CMOS for Micro-Aerial Robotics Application," *IEEE Asian Solid-State Circuits Conference (ASSCC)*, November, 2013.

Yakun Sophia Shao and David Brooks. "Energy Characterization and Instruction-Level Energy Model of Intel's Xeon Phi Processor," *International Symposium on Low Power Electronics and Design (ISLPED)*, September, 2013.

Brandon Reagen, Yakun Sophia Shao, Gu-Yeon Wei and David Brooks. "Quantifying Acceleration: Power/Performance Trade-Offs of Application Kernels in Hardware," *International Symposium on Low Power Electronics and Design (ISLPED)*, September, 2013.

Xuan Zhang, Tao Tong, Svilen Kanev, Sae-Kyu Lee, Gu-Yeon Wei, and David Brooks. "Characterizing and evaluating voltage noise in multi-core near-threshold processors," *IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, September, 2013.

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David Brooks, J.D. Wellman, Margaret Martonosi, and Pradip Bose. "Power-Performance Modeling and Tradeoff Analysis for a High End Microprocessor," *Workshop on Power Aware Computing Systems. (Associated with Symposium on Architectural Support for Programming Languages and Operating Systems.)* November, 2000. (Also in Springer-Verlag Lecture Notes in Computer Science Volume 2008.)

David Brooks and Margaret Martonosi. "Value-based Clock Gating and Operation Packing: Dynamic Strategies for Improving Processor Power and Performance," *ACM Transactions on Computer Systems*, Volume 18, No. 2, May, 2000.

Books

Brandon Reagen, Robert Adolf, Paul Whatmough, Gu-Yeon Wei, and David Brooks. "Deep Learning for Computer Architects," *Synthesis Lectures on Computer Architecture, Morgan & Claypool Publishers*, August, 2017.

Yakun Sophia Shao and David Brooks. "Research Infrastructures for Hardware Accelerators," *Synthesis Lectures on Computer Architecture, Morgan & Claypool Publishers*, November, 2015.

Refereed Workshop and Poster Publications

Yuji Chai, Luke Bailey, Yunho Jin, Glenn Ko, Matthew Karle, David Brooks, Gu-Yeon Wei, H Kung. "SpeedLimit: Neural Architecture Search for Quantized Transformer Models," *Workshop on Efficient Systems for Foundation Models at ICML 2023*, July, 2023.

Mariam Elgamal, Doug Carmean, Elnaz Ansari, Okay Zed, Ramesh Peri, Srilatha Manne, Udit Gupta, Gu-Yeon Wei, David Brooks, Gage Hills, Carole-Jean Wu. "Carbon-Efficient Design Optimization for Computing Systems", *Proceedings of the 2nd Workshop on Sustainable Computer Systems (HotCarbon)*, July, 2023.

Lillian Pentecost, Marco Donato, Brandon Reagen, Udit Gupta, Siming Ma, Gu-Yeon Wei, David Brooks. "MaxNVM: Maximizing DNN Storage Density and Inference Efficiency with Sparse Encoding and Error Mitigation, " *11th Annual Non-Volatile Memories Workshop*, March, 2020.

Lillian Pentecost, Udit Gupta, Elisa Ngan, Gu-Yeon Wei, David Brooks, Johanna Beyer, Michael Behrisch. "CHAMPVis: Comparative Hierarchical Analysis of Microarchitectural Performance," *Workshop on Programming and Performance Visualization Tools (ProTools) co-located with Supercomputing*, November, 2019.

Glenn G Ko, Yuji Chai, Rob A Rutenbar, David Brooks, Gu-Yeon Wei. "FlexGibbs: Reconfigurable Parallel Gibbs Sampling Accelerator for Structured Graphs," *Poster Presentation at International Symposium on Field-Programmable Custom Computing Machines*, April, 2019.

Yakun Sophia Shao, Sam Xi, Viji Srinivasan, Gu-Yeon Wei, David Brooks. "Toward Cache-Friendly Hardware Accelerators," *Sensors to Cloud Architectures Workshop (SCAW-2015), held with HPCA-2015*, February, 2015.

Simone Campanoni, Svilen Kanev, Kevin Brownell, Gu-Yeon Wei, David Brooks. "Breaking Cyclic-Multithreading Parallelization with XML Parsing," *International Workshop on Parallelism in Mobile Platforms (PRISM)*, June, 2014.

Svilen Kanev, Timothy M. Jones, Gu-Yeon Wei, David Brooks, Vijay Reddi. "Measuring Code Optimization Impact on Voltage Noise," *9th IEEE Workshop on Silicon Errors in Logic - System Effects (SELSE-9)*, March, 2013.

Amanda Chih-Ning Tseng and David Brooks. "Analytical Latency-Throughput Model of Future Power Constrained Multicore Processors ," *ISCA Workshop on Energy-Efficient Design (WEED)*, June, 2012.

Michael Lyons, Gu-Yeon Wei, and David Brooks. "Making Every Switch Count: Specialization to Overcome the Power-Wall," *New Directions in Computer Architecture (NDCA) workshop at the International Symposium on Microarchitecture*, December, 2009.

Mark Hempstead, Gu-Yeon Wei and David Brooks. "Navigo: An early-stage model to study power-constrained architectures and specialization," *ISCA Workshop on Modeling, Benchmarking, and Simulations (MoBS)*, June, 2009.

Mark Hempstead, Gu-Yeon Wei and David Brooks. "An accelerator-based wireless sensor network processor in 130nm CMOS," *ISCA Workshop on Architectural Research Prototyping (WARP)*, June, 2009.

Vijay Janapa Reddi, Meeta S. Gupta, Krishna Rangan, Glenn Holloway, Gu-Yeon Wei, Michael D. Smith, and David Brooks. "Voltage Noise: Why It's Bad, and What To Do About It," *5th IEEE Workshop on Silicon Errors in Logic - System Effects (SELSE-5)*, March, 2009.

Xiaoyao Liang, Ramon Canal, Gu-Yeon Wei, and David Brooks. "Process Variation Tolerant Register Files Based on Dynamic Memories," *Workshop on Architectural Support for Gigascale Integration (ASGI-07) held with ISCA-34*, June, 2007.

Wonyoung Kim, Meeta S. Gupta, Gu-Yeon Wei and David Brooks. "Enabling On-Chip Switching Regulators for Multi-Core Processors Using Current Staggering," *Workshop on Architectural Support for Gigascale Integration (ASGI-07) held with ISCA-34*, June, 2007.

Benjamin C. Lee and David Brooks. "Statistically Rigorous Regression Modeling for the Microprocessor Design Space," *Workshop on Modeling, Benchmarking, and Simulation (MOBS'06) held with ISCA-33*, June, 2006.

Xiaoyao Liang and David Brooks. "Latency Adaptation for Multiported Register Files to Mitigate the Impact of Process Variations," *Workshop on Architectural Support for Gigascale Integration (ASGI-06) held with ISCA-33*, June, 2006.

Mark Hempstead, Xiaoyao Liang, Patrick Mauro, Gu-Yeon Wei, David Brooks. "Design and Implementation of An Ultra Low Power System Architecture for Wireless Sensor Network Applications," SRC Techcon, SoC Design Contest 2nd place, Portland, OR, October, 2005.

Benjamin Lee and David Brooks. "Effects of Pipeline Complexity on SMT/CMP Power-Performance Efficiency," *Proceedings of the 6th Workshop on Complexity-Effective Design (WCED'05)*, June, 2005.

Mark Hempstead, David Brooks, Matt Welsh. "TinyBench: The Case For A Standardized Benchmark Suite for TinyOS Based Wireless Sensor Network Devices," *Proceedings of the IEEE Workshop on Embedded Networked Sensors(EmNets'04)*, November, 2004.

Pradip Bose, David Brooks, Alper Buyuktosunoglu, Peter Cook, Kaushik Das, Philip Emma, Michael Gschwind, Hans Jacobson, Tejas Karkhanis, Stanley Schuster, Jim E. Smith, Viji Srinivasan, Victor Zyuban, David H. Albonesi, Sandhya Dwarkadas. "Early-Stage Definition of LPX: A Low Power Issue-Execute Processor Prototype," *Workshop on Power Aware Computing Systems, Held at HPCA-8*, February, 2002.

David Brooks, J.D. Wellman, Margaret Martonosi, and Pradip Bose. "Power-Performance Modeling and Tradeoff Analysis for a High End Microprocessor," *Workshop on Power Aware Computing Systems, at ASPLOS 2000*, November, 2000. (Also in Springer-Verlag Lecture Notes in Computer Science Volume 2008.)

Alper Buyuktosunoglu, Stanley Schuster, David Brooks, Pradip Bose, Peter Cook, David H. Albonesi. "An Adaptive Issue Queue for Reduced Power at High Performance," *Workshop on Power Aware Computing Systems, at ASPLOS 2000*, November, 2000. (Also in Springer-Verlag Lecture Notes in Computer Science Volume 2008.)

David Brooks and Margaret Martonosi. "Adaptive Thermal Management for High-Performance Microprocessors," *Proceedings of the 1st Workshop on Complexity-Effective Design (WCED'00)*, June, 2000.

David Brooks and Margaret Martonosi. "Implementing Application-Specific Cache Coherence Protocols in Configurable Hardware," *Workshop on Communications, Architecture, and Applications for Network-based Parallel Computing, at HPCA-5*, January, 1999. (Also in Springer-Verlag Lecture Notes in Computer Science Volume 1602.)

Invited Papers

Antonino Tumeo, Marco Minutoli, Vito Giovanni Castellana, Joseph Manzano, Vinay Amatya, David Brooks, Gu-Yeon Wei. "Software defined accelerators from learning tools environment," *57th ACM/IEEE Design Automation Conference (DAC)*, July, 2020.

Marco Minutoli, Vito Giovanni Castellana, Cheng Tan, Joseph Manzano, Vinay Amatya, Antonino Tumeo, David Brooks, Gu-Yeon Wei. "SODA: a new synthesis infrastructure for agile hardware design of machine learning accelerators," *IEEE/ACM International Conference On Computer Aided Design (ICCAD)*, November, 2020.

David Brooks, Martin M Frank, Tayfun Gokmen, Udit Gupta, X Sharon Hu, Shubham Jain, Ann Franchesca Laguna, Michael Niemier, Ian OConnor, Anand Raghunathan, Ashish Ranjan, Dayane

Reis, Jacob R Stevens, Carole-Jean Wu, Xunzhao Yin. "Emerging neural workloads and their impact on hardware," *Design, Automation Test in Europe Conference Exhibition*, March, 2020.

David Brooks and John Sartori. "Ultra-Low-Power Processors," *Guest Editor Introduction for IEEE Micro*, November, 2017.

David Brooks. "2017 International Symposium on Computer Architecture Influential Paper Award," *Invited introduction for IEEE Micro*, November, 2017.

Paul Whatmough, Sae-Kyu Lee, David Brooks, and Gu-Yeon Wei. "Sub-uJ deep neural networks for embedded applications," *Asilomar Conference on Signals, Systems, and Computers*, October, 2017.

Sreela Kodali, Patrick Hansen, Naihm Mulholland, Paul Whatmough, David Brooks, annd Gu-Yeon Wei. "Applications of Deep Neural Networks for Ultra Low Power IoT," *IEEE International Conference on Computer Design (ICCD)*, October, 2017.

Ramon Bertran, Pradip Bose, David Brooks, Jeff Burns, Alper Buyuktosunoglu, Nandhini Chandramoorthy, Eric Cheng, Martin Cochet, Schuyler Eldridge, Daniel Friedman, Hans Jacobson, Rajiv Joshi, Subhasish Mitra, Robert Montoye, Arun Paidimarri, Pritish Parida, Kevin Skadron, Mircea Stan, Karthik Swaminathan, Augusto Vega, Swagath Venkataramani, Christos Vezyrtzis, Gu-Yeon Wei, John-David Wellman, and Matthew Ziegler. "Very Low Voltage (VLV) Design," *IEEE International Conference on Computer Design (ICCD)*, October, 2017.

Gu-Yeon Wei and David Brooks. "An SoC Platform Architecture for Mini Autonomous Drones," *Circuit Realization At Faster Timescales (DARPA CRAFT), GOMACTech-17 Conference*, March, 2017.

Tutorials and Special Classes

Udit Gupta, David Brooks, Gu-Yeon Wei, and Carole-Jean Wu, "Personalized Recommendation System and Algorithms," *International Symposium on Computer Architecture*, June, 2020.

Paul Whatmough, Marco Donato, Glenn Ko, Sae-Kyu Lee, David Brooks, Gu-Yeon Wei, "CHIPKIT: Tutorial on Agile Research Test Chips," *International Symposium on Computer Architecture*, June, 2020.

Udit Gupta, David Brooks, Gu-Yeon Wei, and Carole-Jean Wu, "Personalized Recommendation System and Algorithms," *International Symposium on Architectural Support for Programming Languages and Operating Systems*, March, 2020.

Paul Whatmough, Marco Donato, Glenn Ko, Sae-Kyu Lee, David Brooks, Gu-Yeon Wei, "CHIPKIT: Tutorial on Agile Research Test Chips," *International Symposium on Microarchitecture*, October, 2019.

David Brooks, with Yakun Sophia Shao, Sam Xi, Zhenman Fang, and Jason Cong, "Rapid Exploration of Accelerator–Rich Architectures: Automation from Concept to Prototyping," *International Symposium on Microarchitecture*, October, 2016.

David Brooks, with Yakun Sophia Shao, Sam Xi, Gu-Yeon Wei, "Aladdin and gem5-Aladdin: Research Infrastructures for Specialized Architectures," *International Symposium on Workload Characterization (IISWC)*, September 2016.

David Brooks, with Yakun Sophia Shao, Sam Xi, Brandon Reagen, Yu-Ting Chen, Zhenman Fang, Glenn Reinman, and Jason Cong, "Rapid Exploration of Accelerator–Rich Architectures: Automation from Concept to Prototyping," *International Symposium on Computer Architecture*, June, 2015.

David Brooks, with Yakun Sophia Shao, Brandon Reagen, and Mark Hempstead, "Research Infrastructures for Accelerator-Centric Architectures," *International Symposium on High-Performance Computer Architecture*, February, 2015.

David Brooks, "Research Infrastructures for Accelerator-Centric SoC Architectures," *National TsingHua University, Hsinchu, Taiwan*, January, 2015.

David Brooks, with Yakun Sophia Shao, Brandon Reagen, Liang Wang, and Kevin Skadron, "Research Infrastructures for Accelerator-Centric Architectures," *International Symposium on Computer Architecture*, June, 2014.

David Brooks. "Variation-Aware Processor Design," *Sixth International Summer School on Advanced Computer Architecture and Compilation for Embedded Systems (ACACES'10),* Terrassa, Spain, July, 2010.

David Brooks, with Jim Tschanz, Gu-Yeon Wei, and Chris Wilkerson. "Design Variability: Trends, Models, and Design Solutions," *37th International Symposium on Computer Architecture (ISCA 2010),* Saint-Malo, France, June, 2010.

David Brooks, with Keith Bowman, Gu-Yeon Wei, and Chris Wilkerson. "Design Variability: Trends, Models, and Design Solutions," *41st Annual International Symposium on Microarchitecture (Micro-41),* Lake Como, Italy, November, 2008.

David Brooks, with Bronis de Supinski, Benjamin C. Lee, Sally A. McKee, Martin Schulz, and Karan Singh. "Learning and Inference Tutorial (LIT) for Large Design and Parameter Spaces," *13th International Conference on Architectural Support for Programming Languages and Operating Systems,* Seattle, WA, March, 2008.

David Brooks, with Bronis de Supinski, Benjamin Lee, Sally A. McKee, Martin Schulz, and Karan Singh. "Inference and Learning for Large Scale Microarchitectural Analysis," *34th International Symposium on Computer Architecture,* San Diego, CA, June, 2007.

David Brooks. "Microarchitecture-Level Power Simulation: Modeling, Validation, and Design Impact," *Cool Chips VIII,* Yokohama, Japan, April, 2005.

David Brooks, with Kevin Skadron, Antonio Gonzalez, Lev Finkelstein, and Mircea Stan. "Thermal Issues for Temperature-Aware Computer Systems," *31st International Symposium on Computer Architecture,* Munich, Germany, June, 2004.

David Brooks, with Zhigang Hu and Victor Zyuban. "Microarchitecture-Level Power-Performance Simulators: Modeling, Validation, and Impact on Design," *36th IEEE Symposium on Microarchitecture (MICRO-36),* San Diego, CA, December, 2003.

David Brooks, with Kevin Skadron and Mircea Stan. "Thermal Management Issues for Microprocessors," *35th IEEE Symposium on Microarchitecture (MICRO-35),* Istanbul, Turkey, November, 2002.

David Brooks, with Pradip Bose, Mary Jane Irwin, Mahmut Kandemir, Margaret Martonosi, and Vijaykrishnan Narayanan. "Power-Efficient Design: Modeling and Optimizations," *28th International Symposium on Computer Architecture,* Gotenburg, Sweden, June, 2001.

David Brooks, with Pradip Bose and Margaret Martonosi. "Power-Performance Modeling, Analysis and Validation," *Seventh IEEE Symposium on High-Performance Computer Architecture (HPCA-7),* Monterrey, Mexico, January, 2001.

David Brooks, with Pradip Bose and Margaret Martonosi. "Modeling and Analyzing CPU Power and Performance: Metrics, Methods, and Abstractions," *ACM SIGMETRICS Conference on Measurement and Modeling of Computer Systems*, Cambridge, MA, June, 2001.

Invited Talks and Keynotes

"Machine Learning at Scale," Presented at Academia Sinica, Taipei, Taiwan, January 2020.

"Machine Learning at Scale," Presented at IBM, November 2019.

"Machine Learning at Scale," Presented at TSMC, November 2019.

"Machine Learning at Scale," Keynote Presentation at IEEE International Symposium on Performance Analysis of Software and Systems, March 2019.

"Machine Learning at Scale," Presented at National Taiwan University, December 2018.

"Post von Neumann computer architecture," Presented at Army Research Lab, November 2018.

"A Retrospective and Future Challenges in Extreme Heterogeneity," Presented at MODSIM, August 2018.

"Co-designed Systems for Deep Learning Hardware Accelerators," Presented at VLSI-DAT, April 2018.

"An Edge-Based Adaptive Agent," Presented at Intel Corporation, December 2017.

"Beyond the TPU: Opportunities for acceleration in the datacenter ," Presented at Intel Corporation, December 2017.

"The Minerva project: Bringing machine learning to the edge," Presented at Intel Corporation, December 2017.

"Computer Architectures for Deep Learning Applications," Presented at Facebook Corporation, August 2017.

"Computer Architectures for Deep Learning Applications," Presented at Intel Corporation, August 2017.

"Computer Architectures for Deep Learning Applications," Presented at University of Southern California, April 2017.

"Cognitive IoT: Taking Machine Learning to Edge Devices," Presented at Raytheon, April 2017.

"Reducing Datacenter Taxes with Hardware Accelerators," Presented at Intel Corporation, March, 2017.

"Cognitive IoT: Taking Machine Learning to Edge Devices," Presented at the National Taiwan University, March, 2017.

"Computer architectures for deep learning applications," Presented at National Taiwan University, January, 2017.

"Cognitive IoT: Taking Machine Learning to Edge Devices," Presented at MediaTek, Hsinchu, Taiwan, October, 2016.

"Cognitive IoT: Taking Machine Learning to Edge Devices," Presented at Harvard HBS/SEAS Symposium, August, 2016.

"Computer architectures for deep learning applications," Presented at National Taiwan University of Science and Technology, June, 2016.

"Accelerators for Deep Neural Networks," Presented at Intel, Hillsboro, OR, April, 2016.

"Towards specialized computing: Case studies from Robotic Bees to the Google Datacenter," Presented at National Taiwan University, January, 2016.

"RoboBees: A convergence of body, brain, and colony on silicon," Invited Talk at the Workshop on Internet of Things Evolution: Role of MicroArch held in conjunction with the International Symposium on Microarchitecture, December, 2015.

"Reliable system design in the era of specialization," Keynote speech at the IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems, October, 2015.

"The Aladdin Approach to Accelerator Design and Modeling," Presented at Samsung Austin Research Center, October, 2015.

"Workload Characterization in the Era of Specialization ," Keynote speech at the IEEE International Symposium on Workload Characterization, October, 2015.

"Addressing the Computing Technology-Capability Gap: The Golden Age of System Design," Presented at Cray Colloquium Lecture, University of Minnesota, September, 2015.

"Addressing the Computing Technology-Capability Gap: The Golden Age of System Design," Keynote speech at IEEE International Conference on Networking, Architecture, and Storage, August, 2015.

"Accelerator Architectures: High-Level Modeling of Specialization," Presented at Workshop on Modeling and Simulation of Systems and Applications (MODSIM), August, 2015.

"Modeling and Design for Composable, Accelerator-Centric Architectures," Presented at Google, June, 2015.

"Addressing the Computing Technology-Capability Gap: Scaling via Parallelism and Specialization," Keynote speech at the NSF XPS Workshop, June, 2015.

"Circuit and System Design for Robotic Flying Vehicles," Keynote speech at the International Symposium on VLSI Design, Automation and Test, April, 2015.

"Accelerator Architectures: Scaling via Parallelism and Specialization," Presented at Stanford University, April, 2015. v

"Modeling and Design for Composable, Accelerator-Centric Architectures," Presented at National Taiwan University, January, 2015.

"Modeling and Design for Composable, Accelerator-Centric Architectures," Presented at National University of Singapore, January, 2015.

"The Harvard Robobees Project: A Convergence of Body, Brain, and Colony," Presented at Singapore/MIT SMART Research Center, National University of Singapore, January, 2015.

"Design Tools and Modeling Methodologies for Accelerator-Centric Computing: An Architects Perspective," Presented at ICCAD'14 Workshop, "A Roadmap for EDA Research in the Dark Silicon Era," San Jose, CA, November, 2014.

"Modeling and Design for Composable, Accelerator-Centric Architectures," Presented at AMD Research, Boxborough, MA, October, 2014.

"The Harvard Robobees Project: A Convergence of Body, Brain, and Colony," Presented at Duke University, Durham, NC, October, 2014.

"The Harvard Robobees Project: A Convergence of Body, Brain, and Colony," Presented at Microsoft Research, Redmond, WA, August, 2014.

"Modeling and Design for Composable, Accelerator-Centric Architectures," Presented at Qualcomm Research, San Diego, CA, July, 2014.

"Modeling and Design for Composable, Accelerator-Centric Architectures," Presented at Intel, Santa Clara, CA, July, 2014.

"Modeling and Design for Composable, Accelerator-Centric Architectures," Presented at Google, Mountain View, CA, July, 2014.

"Modeling and Design for Composable, Accelerator-Centric Architectures," Presented at MediaTek, Hsinchu, Taiwan, March, 2014.

"The Harvard Robobees Project: A Convergence of Body, Brain, and Colony," Presented at National Cheng Kung University (NCKU), Tainan, Taiwan, March, 2014.

"HELIX+RC: Compiler + architecture co-design yielding automatic parallelization for CMPs," Presented at National Cheng Kung University (NCKU), Tainan, Taiwan, March, 2014.

"The Harvard Robobees Project: A Convergence of Body, Brain, and Colony," Presented at National Chi Nan University (NCNU), Nantou County, Taiwan, March, 2014.

"Modeling and Design for Composable, Accelerator-Centric Architectures," Presented at University of Tokyo, Tokyo, Japan, February, 2014.

"The Harvard Robobees Project: A Convergence of Body, Brain, and Colony," Presented at National Taiwan University (NTU), Taipei, Taiwan, January, 2014.

"Future Computing Platforms: Challenges and Opportunities." Presented at National Taiwan University (NTU), Taipei, Taiwan, January, 2013.

"Modeling and Design for Composable, Accelerator-Centric Architectures." Presented at IBM Thomas J. Watson Research Center, Yorktown Heights, NY, December, 2013.

"Integrated Voltage Regulators: Future of power delivery from mobile to server systems," Presented at Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu, Taiwan, 2012.

"The Harvard Robobees Project," Presented at National Chip Implementation Center (CIC), 2012.

"The Harvard Robobees Project: A Convergence of Body, Brain, and Colony," Presented at VMWare Corporation, 2012.

Michael Lyons, Mark Hempstead, Gu-Yeon Wei, and David Brooks. "Toward An Accelerator-Based Architecture," Invited presentation at the 7th International Conference on High-Performance and Embedded Architectures and Compilers (HiPEAC), January, 2012.

"Robobees: A Convergence of Body, Brain, and Colony," Presented at Texas Instruments Corporation, August, 2011.

"Robobees: A Convergence of Body, Brain, and Colony," Presented at ARM Corporation, April, 2011.

"The Alarms Project: A hardware/software approach to addressing parameter variations," Presented at special session on Post-Silicon Techniques to Counter Process and Electrical Parameter Variability, 16th Asia South Pacific Design Automation Conference, ASP-DAC, January 2011.

"Hardware Specialization and Ultra Low Power Computing in Microrobotic Bees," Invited Talk: 2009 Custom Integrated Circuit Conference, September, 2009.

"Architectural Energy Efficiency," Invited Talk: 2009 Symposium on VLSI Circuits, Short Course on Energy Management for Green SoC's and SiP's, June, 2009.

"Computer Design in the Nanometer Scale Era: Challenges and Solutions," Presented at University of Massachusetts – Amherst, February, 2009.

"Computer Design in the Nanometer Scale Era: Challenges and Solutions," Presented at Massachusetts Institute of Technology, December, 2008.

"Computer Design in the Nanometer Scale Era: Challenges and Solutions," Presented at Brown University, December, 2008.

"Architectures for wireless sensor node design," Presented at Politecnico di Milano, November, 2008.

"Computer Design in the Nanometer Scale Era: Challenges and Solutions," Presented at Stanford University, October, 2008.

"Computer Design in the Nanometer Scale Era: Challenges and Solutions," Presented at Intel, Portland, Oregon. September, 2008.

"Computer Design in the Nanometer Scale Era: Challenges and Solutions," Presented at University of Texas, Austin, September, 2008.

"Synergistic Supply Voltage Control and Management in the Multicore Era," Presented at HP Labs, Palo Alto, California, September, 2008.

"Computer Design in the Nanometer Scale Era: Challenges and Solutions," Presented at Universitat Politecnica de Catalunya, and Intel Barcelona Research Center, July, 2008.

"Computer Design in the Nanometer Scale Era: Challenges and Solutions," Presented at IBM T.J. Watson Research Center, July, 2008.

"Computer Design in the Nanometer Scale Era: Challenges and Solutions," Presented at Tsinghua University, Beijing, China, June, 2008

"Computer Design in the Nanometer Scale Era: Challenges and Solutions," Presented at University of California, Berkeley, May, 2008.

"Computer Design in the Nanometer Scale Era: Challenges and Solutions," Presented at University of Illinois, Urbana-Champaign, April, 2008.

"Computer Design in the Nanometer Scale Era: Challenges and Solutions," Presented at University of Michigan, April, 2008.

"Computer Design in the Nanometer Scale Era: Challenges and Solutions," Presented at North Carolina State University, April, 2008.

"Computer Design in the Nanometer Scale Era: Challenges and Solutions," Presented at Duke University, April, 2008.

"Computer Design in the Nanometer Scale Era: Challenges and Solutions," Presented at University of Wisconsin, Madison, March, 2008.

"Computer Design in the Nanometer Scale Era: Challenges and Solutions," Presented at Intel, Hudson, Massachusetts, March, 2008.

"Reducing the Energy Footprint of Data Centers Panel," Presented at VMworld, September, 2007.

"Pushing the Bounds of Low-Power Computing: An Event-Driven Architecture for Sensor Network Applications," Presented at Chalmers University of Technology, June, 2007.

"Architectural Approaches to Technology-Driven Computer Design," Presented at Carnegie Mellon University, October, 2006.

"Architectural Approaches to Technology-Driven Computer Design," Presented at Lawrence Livermore National Laboratory, August, 2006.

"Architectural Approaches to Technology-Driven Computer Design," Presented at IBM T.J. Watson Research Center, May, 2006.

"Pushing the Bounds of Low-Power Computing: An Event-Driven Architecture for Sensor Network Applications," Presented at Princeton University, November, 2005.

"Pushing the Bounds of Low-Power Computing: An Event-Driven Architecture for Sensor Network Applications," Presented at Penn State University, September, 2005.

"Performance, Energy, and Thermal Considerations for SMT and CMP Architectures," Presented at Intel, Hudson, Massachusetts, March, 2005.

"Pushing the Bounds of Low-Power Computing: An Event-Driven Architecture for Sensor Network Applications," Presented at Boston University, March, 2005.

"Pushing the Bounds of Low-Power Computing: An Event-Driven Architecture for Sensor Network Applications," Presented at University of Connecticut, March, 2005.

"Pushing the Bounds of Low-Power Computing," Presented at IBM Research, Yorktown Heights, NY, January, 2005.

"Adaptive Alarm-Based Approaches to High-Performance/Low-Cost Computing," Presented at Harvard Industrial Partnership Meeting, October, 2004.

"Computer Architecture for Thermal Management," Presented at Harvard Applied Mechanics and Mathematics Study Group.

"Power-Aware Computing: Background, Modeling, and Design," Presented to Intel VSSAD, Hudson, MA, April, 2004.

"Power-aware Computing: Applications and Architectures," Presented at Harvard Industrial Partnership Meeting, November, 2003.

"Architectural and System Level Power Analysis and Optimization," Presented at the Low-Power Circuit and System Design Workshop, International Conference on Computer Design, September, 2003.

"Optimizing Pipelines for Power and Performance," Presented to Intel VSSAD, Hudson, MA, February, 2003.

Released Software, Benchmarks, and Tools

Sam Xi, Yuan Yao, Gu-Yeon Wei, and David Brooks. SMAUG: Simulating Machine Learning Accelerators Using gem5-Aladdin, 2020.

Yu Emma Wang, Gu-Yeon Wei, and David Brooks. `ParaDNN`: Parameterized Deep Neural Network Models for Performance Evaluation, 2020.

Lillian Pentecost, Udit Gupta, Brandon Reagen, Gu-Yeon Wei, and David Brooks. Ares: A framework for quantifying the resilience of deep neural networks, 2019.

Yakun Sophia Shao, Sam Xi, Gu-Yeon Wei, and David Brooks. `gem5-Aladdin`. Integration of `gem5` and `Aladdin` simulators, 2016.

Bob Adolf, Saketh Rama, Brandon Reagen, Gu-Yeon Wei, and David Brooks. `Fathom`. A collection of workloads for benchmarking modern machine learning techniques, 2016.

Sam Xi and David Brooks. `McPAT CPU Models`. Validated McPAT power models for a commercial high-performance multicore CPU, 2015.

Brandon Reagen, Bob Adolf, Yakun Sophia Shao, Gu-Yeon Wei, and David Brooks. `MachSuite`. A benchmark suite for high-level synthesis and accelerator-centric architectures, 2014.

Yakun Sophia Shao, Brandon Reagen, Gu-Yeon Wei, and David Brooks. `Aladdin`. A Pre-RTL, Power-Performance Accelerator Simulator Enabling Large Design Space Exploration of Customized Architectures, 2014.

Emma Wang, Yakun Sophia Shao, and David Brooks. `LLVM-Tracer`. An LLVM instrumentation pass to print out a dynamic LLVM IR execution trace, including dynamic values and memory addresses, 2014.

Yakun Sophia Shao, Emma Wang, and David Brooks. `WIICA`. A Workload ISA Independent Characterization for Applications tool, 2013.

Svilen Kanev and David Brooks. `XioSim`. A detailed user-mode microarchitectural simulator for the x86 architecture, 2009.

David Brooks and Margaret Martonosi. `Wattch`. An Architectural-Level Power-Performance Analysis Toolkit, 2000.

Patents

Capacitor Reconfiguration Of A Single-Input, Multi-Output, Switched-Capacitor Converter, US Patent #:10,250,130, Granted 2019.

Device and Method for Hybrid Feedback Control of a Switch-Capacitor Multi-Unit Voltage Regulator, US Patent #:10,199,931, Granted 2019.

Fully Integrated 3-Level DC/DC Converter for Nanosecond-Scale Dynamic Voltage Scaling with Fast Shunt Regulation, Patent Application PCT/US2011/062319, Filed Nov. 2011.

Adaptive Event-Guided System and Method for Avoiding Voltage Emergencies, US Patent #:8,949,666, Granted 2015.

Adaptive Issue Queue for Reduced Power at High Performance, US Patent #: 7,865,747, Granted 2011.

Process Variation Tolerant Circuit With Voltage Interpolation And Variable Latency, US Patent #: 7,667,497, Granted 2010.

Processor with Low Overhead Predictive Supply Voltage Gating for Leakage Power Reduction, US Patent #: 7,134,028, Granted 2006.

System and Method of Operand Value Based Processor Optimization by Detecting a Condition of Pre-Determined Number of Bits and Selectively Disabling Pre-Determined Bit-Fields by Clock Gating, US Patent #: 6,745,336, Granted 2004.

Memory Structures Having Selectively Disabled Portions for Power Conservation, US Patent #: 6,298,002, Granted 2001, US Patent #: 6,473,326, Granted 2002, US Patent #: 6,577,524, Granted 2003.

Research Funding

Research Grants

Semiconductor Research Corporation AI HW, "Low-Cost AIHW Specialization via Chiplet-based System-in-Package Architectures," 2024–2026.

Department of Energy, "Design Space Exploration of Tiled Architectures for Recommendation Systems," 2023.

National Science Foundation, "PPoSS: Planning: Streamware - A Scalable Framework for Accelerating Streaming Workloads," 2021-2023.

Department of Energy, "Abisko: Deep Codesign of an Energy-Optimized, High Performance Neuromorphic Accelerator," 2022-2024.

Defense Advanced Research Projects Agency, PI of sub-contract through IBM, "Embedded AI for Autonomous Vehicles: Efficient Programmability of Cognitive Heterogeneous Systems (EPOCHS)," 2018–2022.

Semiconductor Research Corporation and Defense Advanced Research Projects Agency, Associate Director, "Center for Applications Driving Architectures (ADA)," 2018–2022.

Semiconductor Research Corporation, PI, "Multi-Objective Bayesian Optimization for SoC Design Space Exploration," 2018–2020.

Intel Corporation, "An Edge-Based Adaptive Agent," 2017-2019.

National Science Foundation, PI, "SHF:Medium:A Cloudless Universal Translator," 2017–2025.

National Science Foundation, PI, "CSR: SMALL: Virtualized accelerators for scalable, composable architectures", 2017–2020.

National Science Foundation, co-PI, "RoboBees 2.0 towards autonomous micro air vehicles," 2017-2019.

Defense Advanced Research Projects Agency, co-PI of sub-contract through NVIDIA, "MATCH: Efficient Resilience in Embedded Computing," 2016–2019.

Intel Corporation, PI, "Accelerating the Datacenter Tax," 2016–2019.

Intel Corporation, co-PI, "A virtualized SoC platform architecture for mini autonomous drones," 2015–2017.

National Science Foundation, co-PI, "InTrans: A virtualized SoC platform architecture for mini autonomous drones," 2015–2017.

National Science Foundation, co-PI, "Automatically Scalable Computation," 2014–2018.

Semiconductor Research Corporation and Defense Advanced Research Projects Agency, Computational Thrust Lead, "Center for Future Architectures Research (C-FAR)," 2013–2017.

Defense Advanced Research Projects Agency, PI of sub-contract through IBM, "Efficient Resilience in Embedded Computing," 2012–2018.

Intel Corporation, co-PI, "An accelerator-based brain SoC for RoboBees," 2013-2014.

National Science Foundation, Principal Investigator, "Exploration of energy-optimized computing architectures using integrated voltage regulators," 2012–2015.

National Science Foundation, co-PI, "Prototyping Platform to Enable Power-Centric Multicore Research," 2011–2014.

Intel Corporation, PI, "Many-Accelerator Systems and the Accelerator Store: A New Frontier in Computer Architecture," 2010–2011.

Gigascale Systems Research Center, Principal Investigator, "Fine-Grained Accelerator Architectures for Power, Performance, and Portability," 2009–2012.

National Science Foundation, Senior Personnel, IIS-0926148, "RoboBees: A Convergence of Body, Brain and Colony," 2009–2014.

National Science Foundation and Semiconductor Research Corporation, co-PI (PI is Gu-Yeon Wei), "Flexible voltage stacking for chip multiprocessors," 2009–2013.

Semiconductor Research Corporation, Principal Investigator (co-PI is Gu-Yeon Wei), "Scalable Pre-RTL Power Modeling Infrastructure for MP-SOC Architectures," 2008–2012.

National Science Foundation, Principal Investigator (co-PIs are Robert Dick, Russ Joseph, and Gu-Yeon Wei), CCF-0720566, "Integrated Power Delivery - Hardware-Software Techniques to Eliminate Off-Chip Regulation from Embedded Systems," 2007–2012.

National Science Foundation, Principal Investigator (co-PI is Gu-Yeon Wei), CCF-0702344, "Reliability in the Face of Variability under Nanoscale Technology Scaling," 2007–2012.

Defense Advanced Research Projects Agency, Principal Investigator (Young Faculty Award), "Microwatt Computing – Application-Driven Architectures for Wireless Sensor Devices," 2007.

National Science Foundation, Principal Investigator, CCF-0448313, "CAREER: A Framework for Early-Stage Computer Architecture Design Space Exploration and Optimization," 2005–2010.

National Science Foundation, Principal Investigator (co-PIs are Gu-Yeon Wei and Michael Smith), CCF-0429782, "An Adaptive Alarm-Based Approach to High-Performance/Low-Cost Computing", 2004–2007.

National Science Foundation, co-PI (PI is Margo Seltzer, other co-PIs are Wei, Kung, Tarokh), SCI-0330244, "SENSORS: Hourglass: An Infrastructure for Sensor Network", 2003–2007.

Research Gifts

Facebook Corporation, Principal Investigator, "Hardware and Software System Design for AI ML Applications," 2020.

Facebook Corporation, Principal Investigator, "Hardware and Software System Design for AI ML Applications," 2019.

Intel Corporation, Principal Investigator, "Multi-Objective Bayesian Optimization for SoC Design Space Exploration," 2017–2020.

Google Corporation, Principal Investigator, "Tools and Benchmarking for Deep Learning," 2017.

Facebook Corporation, Principal Investigator, "Research in Performance and Power-Efficient Computer Architecture," 2015.

Google Corporation, Principal Investigator, "Accelerating the Datacenter Tax," 2015.

Google Corporation, Principal Investigator, "A System Analysis Framework for Accelerator-Centric Architectures," 2012.

Microsoft Corporation Research Gift, Principal Investigator (co-PIs is Simone Campanoni), "ILDJIT Compiler Infrastructure," 2010.

Microsoft Corporation Research Gift, Principal Investigator (co-PIs are Gu-Yeon Wei and Michael Smith), "A Synergistic Approach To Adaptive Power Management," 2008.

Intel Research Gift, Principal Investigator (co-PI is Michael Smith), "Integrated, Software-Managed Power and Reliability for Next-Generation CMP machines," 2007–2009.

Intel Research Gift, Principal Investigator (co-PI is Gu-Yeon Wei), "Reliability in the face of variability under nanoscale technology scaling," 2007–2009.

Sun Microsystems Research Gift, Co-Principal Investigator (PI is Gu-Yeon Wei), "Advanced memory design in deep submicron technologies," 2007–2009.

Semiconductor Research Association SoC Design Challenge, 1st Prize Award in Phase 2 includes cash prize and design fabrication on IBM .18um process (submission co-lead with Gu-Yeon Wei), 2006.

Harvard Cooke/Clark Fund, "Software-Managed Power Management for Next-Generation Chip Multiprocessors," 2005–2007.

Catalyst Foundation, "μWatt Computing - Application-Driven Circuits and Architectures for Wireless Sensor Devices," 2005–2006.

Intel Research Gift, Principal Investigator, "Thermal-Aware Microprocessor Design: Studying the Impact of Advanced Cooling Technologies on Chip Floorplans and Microarchitecture," 2004–2007.

IBM Faculty Partnership Award, 2003–2005.

Equipment/Software Donations

Taiwan Semiconductor Manufacturing Corporation, Chip Fabrication in 16nm CMOS, 2023.

Taiwan Semiconductor Manufacturing Corporation, Chip Fabrication in 16nm CMOS, 2022.

Taiwan Semiconductor Manufacturing Corporation, Chip Fabrication in 16nm CMOS, 2021.

Taiwan Semiconductor Manufacturing Corporation, Chip Fabrication in 28nm CMOS, 2018.

Taiwan Semiconductor Manufacturing Corporation, Chip Fabrication in 28nm CMOS, 2017.

Intel Corporation, Intel HARP-2 Platform, 2016.

Intel Corporation, Intel HARP Platform, 2016.

Taiwan Semiconductor Manufacturing Corporation, Chip Fabrication in 40nm CMOS, 2014.

Taiwan Semiconductor Manufacturing Corporation, Chip Fabrication in 40nm CMOS, 2012.

Analog Devices Equipment Donation, ADI Test Boards, 2008.

SRC Design Contest, Chip Fabrication Expenses, 2005.

University Teaching

Harvard University. Computer Science 141: Computing Hardware. Digital Logic Design and Basic Computer Architecture. Fall 2005, Fall 2006, Fall 2007, Fall 2008, Fall 2009, Fall 2011, Fall 2012, Fall 2014, Fall 2015, Fall 2016, Spring 2019.

Harvard University. Computer Science 146: Computer Architecture. Introduction to Quantitative Approach to Computer Architecture. Fall 2002, Spring 2004, Spring 2005, Spring 2013, Spring 2015, Spring 2017, Fall 2019, Spring 2021, Spring 2023, Spring 2024.

Harvard University. Computer Science 246: Advanced Computer Architecture. Spring 2003, Fall 2003, Fall 2004, Spring 2006, Spring 2007, Spring 2008, Spring 2009, Spring 2010, Fall 2010, Spring 2013, Spring 2015, Spring 2017, Fall 2019, Spring 2021, Spring 2023, Spring 2024.

Harvard University, Computer Science 247: Advanced Topics in Computer Architecture. ISCA-50 Retrospective, Fall 2023.

Harvard University. Computer Science 247: Advanced Topics in Computer Architecture. Machine Learning and Computer System Co-Design, Fall 2018.

Harvard University. Computer Science 247: Advanced Topics in Computer Architecture. Great Moments in Computing, Spring 2012, Spring 2016

Harvard University. Computer Science 247: Advanced Topics in Computer Architecture. Accelerator Centric Computing, Fall 2013.

Harvard University. Computer Science 290: PhD Grad Cohort Research Seminar, Fall 2020.

Research Advising

Graduated Doctoral Students

Iulian Brumar, Computer Science, PhD 2024, Harvard University
Thesis title: "Early-Stage Non-Conventional Hardware Accelerator Discovery via Optimization Methods and Compiler Analysis"

Thierry Tambe, Electrical Engineering, PhD 2023, Harvard University
Thesis title: "Architecting High Performance Silicon Systems for Accurate and Efficient On-Chip Deep Learning"

Siming Ma, Electrical Engineering, PhD 2023, Harvard University
Thesis title: "Device, Circuit, and Algorithm Co-Design for Efficient Neural Network Inference in Hardware"

Udit Gupta, Computer Science, PhD 2022, Harvard University
Thesis title: "Enabling High Performance, Efficient, and Sustainable Deep Learning Systems At Scale"

Lillian Pentecost, Computer Science, PhD 2022, Harvard University
Thesis title: "Enabling Emerging, Heterogeneous Memory Systems"

Yu Emma Wang, Computer Science, PhD 2019, Harvard University
Thesis title: "Performance Analysis for Machine Learning Applications"

Sam Likun Xi, Computer Science, PhD 2018, Harvard University
Thesis title: "Advancing System-Level Analysis and Design of Specialized Architectures"

Brandon Reagen, Computer Science, PhD 2018, Harvard University
Thesis title: "On the Design and Optimization of Specialized Hardware with Applications in Deep Learning"

Svilen Kanev, Computer Science, PhD 2016, Harvard University
Thesis title: "Efficiency in Warehouse-scale Computers: A Datacenter Tax Study"

Saekyu Lee, Electrical Engineering, PhD 2016, Harvard University
Thesis title: "High Efficiency Power Delivery for Chip Multiprocessors Using Voltage Stacking"

Yakun Sophia Shao, Computer Science, PhD 2016, Harvard University
Thesis title: "Design and Modeling of Specialized Architectures"

Kevin Brownell, Electrical Engineering, PhD 2015, Harvard University
Thesis title: "Architectural Implications of Automatic Parallelization with HELIX-RC"

Tao Tong, Electrical Engineering, PhD 2015, Harvard University
Thesis title: "Improving SoC Power Delivery with Fully Integrated Switched-Capacitor Voltage Regulators"

Michael Lyons, Computer Science, PhD 2013, Harvard University
Thesis title: "Towards a Hardware-Accelerated Future"

Wonyoung Kim, Electrical Engineering, PhD 2013, Harvard University
Thesis title: "Reducing Power Loss, Cost and Complexity of SoC Power Delivery using Integrated 3-Level Voltage Regulators"

Krishna Rangan, Electrical Engineering, PhD 2011, Harvard University
Thesis title: "Hardware-based Thread Scheduling for Power-Efficient and Variation-Resilient Chip Multiprocessors"

Vijay Janapa (VJ) Reddi, Computer Science, PhD 2010, Harvard University
Thesis title: "Software-Assisted Hardware Reliability: Enabling Aggressive Timing Speculation Using Run-Time Feedback from Hardware and Software"

Meeta Gupta, Electrical Engineering, PhD 2009, Harvard University
Thesis title: "Variation-Aware Processor Architectures with Aggressive Operating Margins"

Mark Hempstead, Electrical Engineering, PhD 2009, Harvard University
Thesis title: "Accelerator-Based Architectures for Wireless Sensor Network Applications"

Xiaoyao Liang, Electrical Engineering, PhD 2008, Harvard University
Thesis title: "Joint Architecture and Circuit Resilience to Mitigate the Impact of Process Variations"

Benjamin Lee, Computer Science, PhD 2008, Harvard University
Thesis Title: "Statistical Inference for Efficient Microarchitectural Analysis"

Yingmin Li, Computer Science, PhD 2006, University of Virginia (co-advised with Kevin Skadron)
Thesis Title: "Physical Constraints Aware Chip Multiprocessor Architecture"

Current Doctoral Students, including co-advisees
Yuji Chai, Computer Science, Post-Quals, Harvard University.

Max Lam, Computer Science, Post-Quals, Harvard University.

Matt Adiletta, Computer Science, Post-Quals, Harvard University.

Yunho Jin, Computer Science, Post-Quals, Harvard University.

Mariam Elgamal, Electrical Engineering, Post-Quals, Harvard University.

Nestor Cuevas, Electrical Engineering, Pre-Quals, Harvard University.

Alicia Golden, Computer Science, Pre-Quals, Harvard University.

Jennifer Zhou, Computer Science, Pre-Quals, Harvard University.

Masters Students (Research Advising)
Yeongil Ko, SM 2022, Harvard University.

Mark Wilkening, SM 2022, Harvard University.

En-Yu Yang, SM 2021, Harvard University.

Saketh Rama, SM 2020, Harvard University.

Robert Adolf, SM 2015, Harvard University.

Khalid Al-Hawaj, Meng 2015, Harvard University.

Amanda Chih-Ning Tseng, SM 2014, Harvard University.

Xiao Guo, SM 2012, Harvard University.

Judson Porter, SM 2012, Harvard University.

Jian Li, SM 2010, Harvard University (secondary advisor).

Durlov Khan, SM 2008, Harvard University, Advised from 2007–2008.

Jarod Oatley, SM 2006, Harvard University, Advised from 2005–2006.

Undergraduate Students (Research Advising)
Jaylen Wang, SB 2022, Harvard University, Advised from 2021-2022.

Joseph Zuckerman, SB 2019, Harvard University, Advised from 2018-2019.

Jon Cruz, SB 2017, Harvard University, Advised from 2016-2017.

Antuan Tran, AB 2017, Harvard University, Advised from 2016-2017.

Joy Hui, SB 2016, Harvard University, Advised from 2015-2016.

Svilen Kanev, AB 2012, Harvard University, Advised from 2009–2012.

John Tsai, AB 2012, Harvard University, Advised in 2012.

Peter Bailis, AB 2011, Harvard University, Advised from 2010–2011.

Kristen Lovin, AB/SM 2008, Harvard University, Advised from 2005–2008.

Patrick Mauro, AB 2007, Harvard University, Advised in 2004.

Lukasz Strozek, AB/SM 2006, Harvard University, Advised from 2005–2006.

John Sheu, AB 2004, Harvard University, Advised from 2003–2004.

Yau Chin, AB 2004, Harvard University, Advised from 2003–2004.

Visitors and Research Staff

Abdulrahman Mahmoud, 2021–Present (Post-Doctoral Fellow)

Sai Qian Zhang, 2022 (Post-Doctoral Fellow)

Alex Hankin, 2022–2023 (Post-Doctoral Fellow)

Devashree Tripathy, 2021–2022 (Post-Doctoral Fellow)

Chun-Feng Wu, 2021–2022 (Post-Doctoral Fellow)

Jeff (Jun) Zhang, 2020–2022 (Post-Doctoral Fellow)

Tianyu Jia, 2020–2021 (Post-Doctoral Fellow)

Georgios Zacharopoulos, 2021-2021 (Post-Doctoral Fellow)

Burcin Cakir, 2019–2020 (Post-Doctoral Fellow)

Glenn Ko, 2018–Present (Post-Doctoral Fellow)

Kshitij Bhardwaj, 2018–2020 (Post-Doctoral Fellow)

Wooseok Choi, 2018–2020 (Post-Doctoral Fellow)

Yuan Yao, 2017–2020 (Post-Doctoral Fellow)

Marco Donato, 2017–2020 (Post-Doctoral Fellow)

Paul Whatmough, 2015–2017 (Post-Doctoral Fellow)

Saketh Rama, 2015–2016 (Pre-Doctoral Research Fellow)

Rafael Garibotti, 2014–2015 (Post-Doctoral Fellow)

Xuan Zhang, 2011–2015 (Post-Doctoral Fellow)

Simone Campanoni, 2009–2014 (Post-Doctoral Fellow)

Timothy Jones, January 2010–January 2011 (Post-Doctoral Fellow)

Javier Lira, January 2010–July 2010 (PhD student visiting from UPC-Barcelona, advisors Professors Carlos Molina and Antonio Gonzalez)

Glenn Holloway, 2006–Present (Research Staff)

Simone Campanoni, 2008 (PhD student visiting from Politecnico di Milano, advisor Professor Stefano Crespi Reghizzi)

Ramon Canal, 2006–2007 (Visiting Faculty Member from UPC-Barcelona)

Jiyang Kang, 2006–2007 (Visiting Researcher from Samsung Corporation)

University Service

Co-Chair of the Graduate Admissions Committee, Computer Science and Applied Math, Fall 2020 – Spring 2021.

Director of Graduate Studies, Computer Science and Applied Math, Fall 2020.

Director of Graduate Studies, Computer Science and Applied Math, Fall 2019.

Area Dean for Electrical Engineering, January 2019 – June 2019.

Director of Graduate Studies, Computer Science and Applied Math, Fall 2018.

Committee Member, SEAS Faculty Resource Advisory Committee, 2017–Present.

Co-Chair, Graduate Education Policy Committee, 2014–2017.

Co-Director of Graduate Studies, Computer Science and Applied Math, 2013–2017.

Committee Member, Graduate Education Policy Committee, 2013.

Committee Member, Education Policy Committee, 2013.

Director of Undergraduate Studies, Computer Science, 2004–2007.

Committee Member, Committee on Graduate Admissions and Scholarship, 2002–2007.

Committee Member, Computer Science Committee on Undergraduate Studies, 2002–Present.

Committee Member, Engineering Sciences Committee on Undergraduate Studies, 2002–2005.

Committee Member, Computer Science Junior Faculty Search Committee, Spring 2003.

Committee Member, Committee on Higher Degrees, 2002–2003.

Chair, Committee on Higher Degrees for Computer Science and Applied Math, 2011–2014.

Committee Member, FAS Dean's Faculty Resource Committee, 2012–2014.

Committee Member, Harvard Committee on Retention and Maintenance of Research Records, 2012.

Thesis Committee Member for several Ph.D. Students.

Qualifying Exam Committee Member for several Ph.D. Students.

Professional Service

Conference Organization Activities

Program Committee, International Symposium on Computer Architecture, 2024.

Program Committee, IEEE Micro Top Picks 2023.

Program Committee, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2022.

External Program Committee, International Symposium on Microarchitecture, 2020.

Program Committee, IEEE International Symposium on Workload Characterization, 2020.

Program Committee, International Symposium on Computer Architecture, 2020.

Program Committee, International Conference on Architectural Support for Programming Languages and Operating Systems, 2020.

Program Committee, International Symposium on High-Performance Computer Architecture, 2019.

Program Chair, International Symposium on Computer Architecture, 2017.

Program Committee, International Symposium on Computer Architecture, 2016.

Program Committee, International Symposium on High-Performance Computer Architecture, 2016.

Program Committee, International Symposium on Microarchitecture, 2015.

Organizing Committee, Workshop on Negative Outcomes, Post-mortems, and Experiences, 2015.

Program Committee, International Symposium on Computer Architecture, 2015.

Program Committee, International Symposium on High-Performance Computer Architecture, 2015.

Program Committee, International Symposium on Microarchitecture, 2014.

Program Committee, International Symposium on Computer Architecture, 2014.

Organizing and Program Committee, Workshop on Highly-Reliable Power-Efficient Embedded Designs, 2014.

External Program Committee, International Conference on Architectural Support for Programming Languages and Operating Systems, 2014.

Program Committee, Workshop on Irregular Applications Architectures and Algorithm, 2014.

Program Chair, IEEE International Symposium on Workload Characterization, 2013.

Program Committee, International Symposium on Code Generation and Optimization, 2013.

Organizing and Program Committee, First Workshop on Highly-Reliable Power-Efficient Embedded Designs, 2013.

Steering Committee Chair, IEEE International Symposium on Workload Characterization, 2013–Present.

Program Committee, Workshop on Irregular Applications Architectures and Algorithm, 2013.

Program Committee, International Symposium on Microarchitecture, 2012.

Program Chair, International Symposium on High-Performance Computer Archiecture, 2012.

Program Committee, Special Issue of IEEE Micro's Top Picks from Computer Architecture Conferences, 2012.

Program Committee, International Symposium on Computer Architecture, 2012.

General Co-Chair, Workshop on Performance Modeling and Analysis of Workload Optimized Systems, 2012.

Chair, Design Automation Conference (DAC) Special Session :Hot Chips Running Cool - Energy Efficient Near-Threshold Computing and its Barriers, 2012.

Program Committee, Fourth Workshop on Energy-Efficient Design, 2012

Program Committee, Workshop on Irregular Applications Architectures and Algorithm, 2012.

Steering Committee, IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2012–2018.

General Chair, International Symposium on Performance Analysis of Systems and Software, 2011.

Workshops Chair, International Symposium on Computer Architecture, 2011.

Program Committee, International Symposium on Computer Architecture, 2011.

Program Committee, International Symposium on High-Performance Computer Architecture, 2011.

Program Committee, International Conference on Supercomputing, 2011.

Program Committee, International Conference on High-Performance Embedded Architectures and Compilers, 2010.

Program Committee, International Conference on Parallel Architectures and Compilation Techniques, 2010.

Program Committee, International Symposium on Low Power Electronics and Design, 2010.

Program Chair, International Symposium on Performance Analysis of Systems and Software, 2010.

Program Committee, International Symposium on High-Performance Computer Architecture, 2010.

Program Committee, International Symposium on Computer Architecture, 2009.

Workshops/Tutorials Co-Chair, International Symposium on Microarchitecture, 2009.

External Program Committee, International Symposium on Programming Language Design and Implementation, 2009.

Steering Committee, NSF Workshop on Science of Power Management, 2009.

Program Committee, Special Issue of IEEE Micro's Top Picks from Computer Architecture Conferences, 2009.

Program Committee, International Symposium on High-Performance Computer Architecture, 2009.

Program Committee, International Conference on Parallel Architectures and Compilation Techniques, 2009.

Program Committee, International Symposium on Low Power Electronics and Design, 2009.

Program Committee, International Conference on Computer Design, 2009.

Program Committee, International Symposium on Performance Analysis of Systems and Software, 2009.

Vice Program Chair, Computer Architecture Track, International Symposium on Computer Architecture and High-Performance Computing, 2009

Program Committee, International Parallel and Distributed Processing Symposium, 2009.

Program Committee, International Symposium on High-Performance Computer Architecture, 2008.

Program Committee, International Symposium on Low Power Electronics and Design, 2008.

Program Committee, ACM International Conference on Computing Frontiers, 2008.

Program Committee, International Symposium on Performance Analysis of Systems and Software, 2008

Technical Program Committee Co-Chair, Special Issue of IEEE Micro Micro's Top Picks from Computer Architecture Conferences, 2008.

Program Committee, International Symposium on Microarchitecture, 2007.

Program Committee, International Symposium on Low Power Electronics and Design, 2007.

Publication Chair and Program Committee, International Symposium on Performance Analysis of Systems and Software, 2007.

Program Vice-Chair, and Program Committee, Technology-Driven Architectures, ACM International Conference on Computing Frontiers, 2007.

Program Committee, Special Issue of IEEE Micro Micro's Top Picks from Computer Architecture Conferences, 2007.

Program Committee, International Symposium on High-Performance Computer Architecture, 2007.

Program Committee, International Symposium on Performance Analysis of Systems and Software, 2007.

Program Committee, International Conference on Architectural Support for Programming Languages and Operating Systems, 2006.

Track Co-chair (with Michael Gschwind), Processor Architecture Track, International Conference on Computer Design, 2006.

Program Committee, International Symposium on High-Performance Computer Architecture, 2006.

Program Committee, International Symposium on Performance Analysis of Systems and Software, 2006.

Program Committee, International Parallel and Distributed Processing Symposium, 2006.

Program Committee, International Conference on Parallel and Distributed Systems, 2006.

Track Co-chair (with Michael Gschwind), Processor Architecture Track, International Conference on Computer Design, 2005.

Program Committee, International Symposium on Low Power Electronics and Design, 2005.

Program Committee, International Conference on Computer Design, 2004.

Registration and Finance Chair, International Symposium on Microarchitecture, 2004.

Program Committee, International Symposium on Low Power Electronics and Design, 2004.

Program Committee, International Conference on Computer Design, 2003.

Program Committee, International Symposium on High-Performance Computer Architecture, 2003.

Program Committee, International Symposium on Performance Analysis of Systems and Software, 2002.

Program Committee, International Symposium on Performance Analysis of Systems and Software, 2001.

Web and Publicity Co-Chair, International Symposium on Performance Analysis of Systems and Software, 2001.

Journal Editorship Activities

Guest Editor, IEEE Micro Special Issue on Ultra-Low-Power Processors, November/December 2017

Guest Editor, IEEE Micro Special Issue on CPU, GPU, and Hybrid Computing, September/October 2011

Associate Editor, IEEE Micro, 2016–2020.

Associate Editor, ACM Transactions on Architecture and Code Optimization, 2009 – 2018.

Associate Editor, IEEE Computer Architecture Letters, 2010 – 2015.

Journal Review Activities

IEEE Journal of Solid-State Circuits (JSSC)

IEEE Transactions on Very Large Scale Integration Systems (TVLSI)

IEEE Transactions on Computers

IEEE Transactions on Computer-Aided Design

IEEE Transactions on Parallel and Distributed Systems

IEEE Micro

IEEE Computer

IEEE Computer Architecture Letters

IEEE Pervasive Computing

ACM Transactions on Architecture and Code Optimization

ACM Transactions on Design Automation of Electronic Systems

ACM Transactions on Embedded Computer Systems

ACM Transactions on Sensor Networks

ACM Journal of Emerging Technologies in Computing

Journal of Parallel and Distributed Computing.

IET Computers and Digital Techniques

Other Professional Activities

ACM SIGARCH/IEEE TCCA Outstanding Dissertation award committee, 2018, 2019, 2020.

ACM SIGARCH Alan D. Berenbaum Distinguished Service award committee, 2016–2018.

Member, Cavium Industry-Academia Partnership advisory board, 2012–Present.

Co-chair, NSF Workshop on Cross-Layer Power Optimization and Management, 2012.

Executive Committee Member: Association for Computing Machinery (ACM) Special Interest Group on Microarchitecture (SIGMICRO), 2018–2020.

Executive Committee Member and Vice Chair: Association for Computing Machinery (ACM) Special Interest Group on Microarchitecture (SIGMICRO), 2012–2018.

Participated in the DARPA/ISAT Workshop: Advancing Computer Systems without Technology Progress, Chicago, 2012.

Grant Review Activities

One NSF Panel in 2018

One NSF Panel in 2016

One NSF Panel in 2013

One NSF Panel in 2012

One NSF Panel in 2011

One NSF Panel in 2010

Two NSF Panels in 2009

Two NSF Panels in 2008

One NSF Panel in 2006

One NSF Panel in 2005