EVALUATION METHODOLOGY FOR SINGLE ELECTRON ENCODED THRESHOLD LOGIC GATES

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Abstract Single Electron Tunneling (SET) is an emerging technology, with a switching behavior which is completely different from MOS technology. The ability to control the transport of individual electrons within SET circuits creates the conditions for Single Electron Encoded Logic (SEEL). Although it is expected that, when compared with other approaches, SEEL circuits have both reduced delay and reduced energy consumptions, a method for evaluation is required. This paper proposes a methodology to evaluate delay, power consumption, maximum fanin, and maximum fanout for buffered SEEL linear threshold gates. Furthermore, we discuss the implications of the proposed methodology on practical networks of such gates. We estimate that buffered threshold gates operating at room temperature can potentially switch with a delay of 6 ps and have a packing density of 10^9 gates per cm^2.

Keywords: SET, single electron technology, single electron encoded logic, threshold gates.

1. Introduction

During the last six decades we have witnessed spectacular increases in the processing power of logic and arithmetic circuits. Since the seventies the microelectronics industry has followed Moore's "law" [Moore, 1965], doubling processing power every 18 months. This increase in processing power can to a large extend be contributed to advances in algorithms and device technology [Hennessy and Patterson, 1996]. Focussing on device technology, one can observe that the feature size reduction in microelectronic circuits, and the corresponding increase in the number of transistors per cm^2, has been one of the main contributing factors to this dramatic increase.

Currently, circuit technology is primarily based on (C)MOS devices and it is anticipated that CMOS feature sizes will continue to be scaled down in the near future. The 2003 edition of the International Technology Roadmap for

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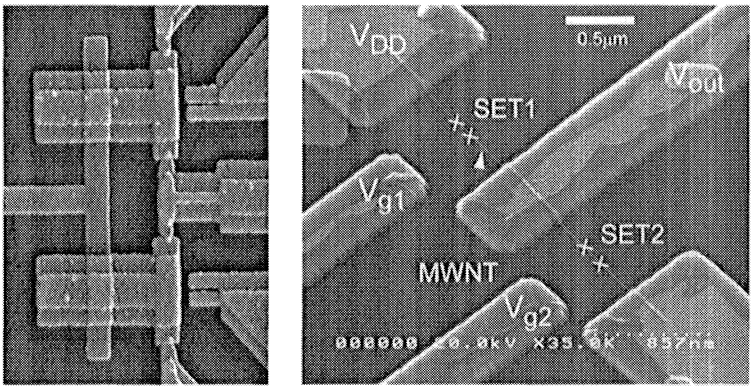
Semiconductors [TRS03, 2003] predicts that in 15 years ultra-thin body (UTB) MOSFETs will reach gate lengths of 10 nm. However, it also predicts that such devices will increasingly operate in a quasi-ballistic mode, i.e., with electrical currents dwindling down to individual electrons. Note that this is already occurring in today's circuits in the form of undesired tunnel currents through thin oxides [Brennan and Brown, 2002, Iwai and Momose, 1998, Momose et al., 1998]. Consequently, the switching behavior of future MOSFET devices will greatly differ from MOSFET behavior in the traditional sense. On the other hand, it is generally accepted that sooner or later MOS based circuits cannot be reduced further in (feature) size due to fundamental physical restrictions [Taur et al., 1997].

Given the anticipated end of the CMOS era, several candidate technologies based on alternative operating principles have been under investigation for the last two decades. These candidate technologies include, amongst others, Single Electron Tunneling (SET), Carbon Nanotubes, Rapid Single Flux Quantum (RSFQ), Resonant Tunneling Diodes (RTD), and Magnetic Spin devices (see [TRN99, 1999] for an overview of some of these emerging technologies). As of yet it is undecided which of these technologies, if any, will supplant (C)MOS. If a candidate technology is to replace (C)MOS in at least some application areas, it must satisfy as many of the following criteria as possible. First, the candidate technology should have greater feature size scaling potential then CMOS, i.e., larger device density. Second, given the anticipated device density the candidate technology should have extremely low power consumption. Note that power consumption is one of the main problems anticipated for (C)MOS in the near future [TRS03, 2003]. Third, it should be able to operate at room temperature as liquid cooling would encumber potential systems with added cost and bulk. Fourth, device switching should occur sufficiently fast, such that when the device is used in conjunction with the appropriate design techniques and architectures to build circuits and systems it can compete or outperform "equivalent" (C)MOS based designs.

As an emerging technology the SET technology [Korotkov, 1999] [Likharev, 1999] offers a number of advantages as follows. First, it offers a greater scaling potential than (C)MOS as the device structure is less complex. Second, SET has the potential to realize circuits that consume much less power than (C)MOS circuits. Third, recent advances in silicon based fabrication technology (see for example [Ono et al., 2000]) indicate that SET has the potential to operate at room temperature. An additional benefit of the SET technology is that SET quantum tunnel junctions, the basic SET circuit element, can be fabricated in many different ways. In order to illustrate the variety in possible implementation technologies, we present in Figure 1 two possible implementations of the SET inverter [Tucker, 1992]. Figure 1(a) depicts an SET inverter fabricated in a conventional lithographic technology on silicon [Heij



(a) Conventional process. (b) Carbon nanotube.

Figure 1. SET inverter implementations.

et al., 2001]. In this case the tunnel junctions resemble conventional capacitors and consist of small gaps between conducting plates. Figure 1(b) on the other hand depicts a carbon nanotube based implementation [Ishibashi et al., 2001] in which case the tunnel junctions consist of small gaps in a multiwall carbon nanotube.

Similar to other future technology candidates, SET devices display a switching behavior that differs from traditional MOS devices. This provides new possibilities and challenges for implementing digital circuits. Currently, there are three design styles in creating SET-based logic circuits. The first approach is to implement the SET equivalent of the MOS transistor (see for example [Tucker, 1992]) an mimic the (C)MOS design style. The main disadvantage of this approach is that the current transport through an "open" transistor still comprises a large number of individual electrons "dripping" through the tunnel junctions. This results in increased delay and power consumption. The second approach is to design SET Boolean logic gates that operate according to the Single Electron Encoded Logic (SEEL) paradigm, i.e., charge transport due to switching activity is limited to a single electron. Given that this results in the transport of fewer electrons, it is expected that SEEL circuits have both reduced delay and reduced energy consumption. Earlier investigations revealed that (buffered) SEEL linear threshold logic gates can be constructed based on the Coulomb blockade of SET tunnel junctions [Lageweg et al., 2001a] and that such gates operate correctly in larger networks [Lageweg et al., 2002]. A third approach is to design high radix logic circuits in which a non-Boolean

value X is encoded as X electron charges and implement electron counting based logic [Cotofana et al., 2003]. Currently electron counting based implementations still require additional amplification, i.e., OP-AMPs, for which a SET tunnel junction based implementation has not yet been found.

Comparing the above three design styles, we conclude that the SEEL based approach appears to be the most promising due to the limited amount of transported charge. Moreover, previous research has demonstrated that networks of SEEL threshold gates can be implemented by only utilizing SET circuit elements [Lageweg et al., 2002]. However, in order to compare this approach with others, a methodology for estimating the delay and power consumption is required. In order to evaluate the SEEL linear threshold gate, as well as to provide a means for evaluating other single electron logic approaches, this paper proposes a methodology to evaluate delay, power consumption, maximum fanin, and maximum fanout for buffered SEEL linear threshold gates.

The remainder of this paper is organized as follows. Section 2 introduces the SET theory. Section 3 describes the generic SET linear threshold gate and the SET buffer, which are combined as a generic SEEL buffered threshold gate. In Section 4 methods for analyzing the delay, the power consumption, the fanin and the fanout of buffered threshold gates operating in a network are proposed. Section 5 applies the proposed methods to evaluate parameter asymptotic bounds for practical SEEL threshold logic networks. Section 6 concludes the paper with some final remarks.

2. Background

The Single Electron Tunneling (SET) technology introduces the quantum tunnel junction as a new circuit element. A tunnel junction consist of two conductors separated by an extremely thin insulating layer. The insulating layer acts as an energy barrier which inhibits charge transport under normal (classical) physics laws. However, according to quantum physics theory, charge transport of individual electrons through this insulating layer can occur if this results in a reduction of the total energy present in the circuit. The transport of charge through a tunnel junction is referred to as *tunneling*, while the transport of a single electron is referred to as a *tunnel event*. Electrons are considered to tunnel through a tunnel junction strictly one after another.

Rather then calculating for each tunnel junction if a hypothetical tunnel event results in a reduction of the circuit's energy, we can calculate the critical voltage V_c, which is the voltage threshold needed across the tunnel junction to make a tunnel event through this tunnel junction possible. For calculating the critical voltage of a junction, we assume that the tunnel junction has a capacitance of C_j and that the remainder of the circuit, as viewed from the tunnel junction's perspective, has an equivalent capacitance of C_e. Given the

approach presented in [Wasshuber, 1998], we calculate V_c for the junction as

$$V_c = \frac{q_e}{2(C_e + C_j)}. \tag{1}$$

In the above equation, as well as in the remainder of this discussion, we refer to the charge of the electron as $q_e = 1.602 \cdot 10^{-19}\ C$. Strictly speaking this is incorrect, as the charge of the electron is of course negative. However, it is more intuitive to consider the electron as a positive constant for the formulas which determine if a tunnel event will take place or not. We will of course correct for this when we discuss the direction in which the tunnel event takes place.

Generally speaking, if we define the voltage across a junction as V_j, a tunnel event will occur through this tunnel junction if and only if $|V_j| \geq V_c$. If tunnel events cannot occur in any of the circuit's tunnel junctions, i.e., $|V_j| < V_c$ for all junctions in the circuit, the circuit is in a *stable state*. For our research we focus on circuits where a limited number of tunnel events may occur, resulting in a stable state. Each stable state determines a new output value resulting from the distribution of charge throughout the circuit.

Given that electron tunneling as described by the orthodox tunneling theory (see for example [Wasshuber, 1998] for a more extensive introduction) is a quantum physical process, the transport of individual electrons can only be described by a stochastic process. This implies that we can at most calculate the chance that an electron has tunneled through a tunnel junction after a time interval t_d. In other words, there will always be a non-zero switching error probability P_{error}. In addition to the switching error probability there are two fundamental phenomena that may cause errors: thermal tunneling and cotunneling. Thermal tunneling events are tunnel events due to thermal agitation. Cotunneling events are two tunnel events that reduce the total amount energy of the system when they occur *simultaneously*, while the individual tunnel events each increase the total amount of energy present in the system. Given a maximum acceptable switching error probability, we must ensure that the thermal error probability as well as the cotunneling error probability are of the same order of magnitude or less.

The thermal error probability can be calculated as follows. For any temperature $T > 0K$ there exists a non-zero probability that a tunnel event will occur through a junction (even if $|V_j| < V_c$). The error probability P_{therm} due to *thermal tunneling* can be described by a simple formula as

$$P_{therm} = e^{-\Delta E / K_b T}, \tag{2}$$

where k_b is Boltzman's constant ($k_b = 1.38 \cdot 10^{-23} J/K$) and ΔE is the change in the energy as a results of the tunnel event. For practical purposes, this implies that, if we intend to add or remove charge to a circuit node by means of

tunnel events, the total capacitance attached to such a circuit node must be less then $900aF$ for $1K$ temperature operation, or less then $3aF$ for $300K$ (room temperature) operation [Goossens, 1998]. This represents a major SET fabrication technology hurdle as even for cryostat temperature operation very small circuit features are required to implement such small capacitors.

For a multi-junction system in which a combination of tunnel events leads to a reduction of the energy present in the entire system there exists a non-zero probability that those tunnel events occur simultaneously (even if $|V_j| < V_c$ for all individual tunnel junction involved). This phenomenon is commonly referred to as *cotunneling* [Averin and Odintsov, 1989, Averin and Nazarov, 1990]. Although a detailed analysis of cotunneling is outside the scope of the present work, we remark that the best approach for reducing the cotunneling error probability appears to be the addition of strip resistors between the SET circuit and the supply voltage lines, as demonstrated in [Lotkhov et al., 1999, Zorin et al., 2000, Lotkhov et al., 2001]. This method can reduce the cotunneling rate without significantly increasing the switching delay. This is due to the fact that the delay added by a resistor is on the RC scale. Thus, assuming for example $R = O(10^6)\ \Omega$ and $C = O(10^{-18})\ F$, we find that the delay added by the resistor is $t_{RC} = O(10^{-12})\ s$. As these such RC values switching delay of tunnel events is typically at least one order of magnitude larger, the additional delay due to the cotunneling suppressing resistors would be negligible. Although the circuits discussed in the remainder of this paper do not contain such resistors, cotunneling suppressing resistors of appropriate value can be appended to the designs in order to reduce the cotunneling error to an acceptable error probability.

The next section introduces the SEEL linear theshold gate, which serves as an example circuit for the type of SEEL circuits which our proposed methodology evaluates in terms of delay, power consumption, fanin and fanout.

3. Single Electron Encoded Threshold Logic Gate

Threshold logic gates are devices which are able to compute any linearly separable Boolean function given by:

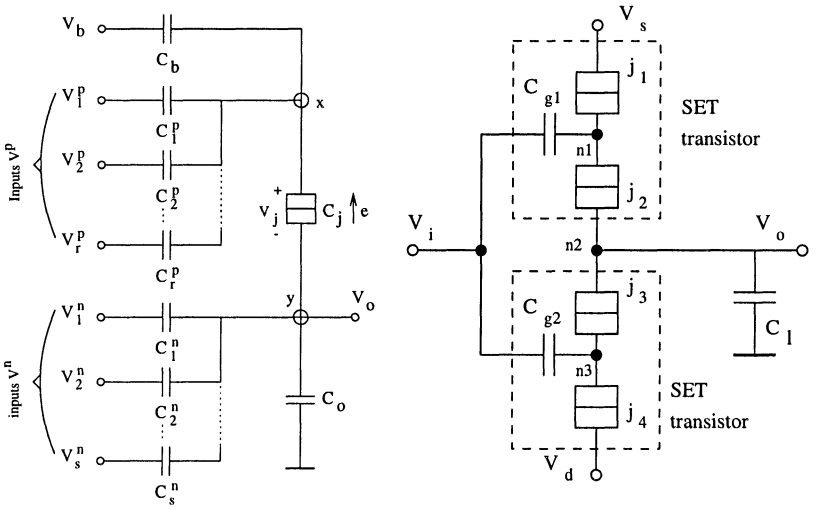
$$Y = sgn\{\mathcal{F}(X)\} = \begin{cases} 0 & \text{if } \mathcal{F}(X) < 0 \\ 1 & \text{if } \mathcal{F}(X) \geq 0 \end{cases} \tag{3}$$

$$\mathcal{F}(X) = \sum_{i=1}^{n} \omega_i x_i - \psi \tag{4}$$

where x_i are the n Boolean inputs and w_i are the corresponding n integer weights. The linear threshold gate performs a comparison between the weighted sum of the inputs $\Sigma_{i=1}^{n} \omega_i x_i$ and the threshold value ψ. If the weighted sum of inputs is *greater than or equal to* the threshold, the gate produces a logic

1. Otherwise the output is a logic 0. Note that threshold logic gate networks are fundamentally more powerful than networks of standard Boolean gates [Muroga, 1971], e.g., TL gate based implementations of Boolean functions potentially require a smaller number of gates and less gate levels.

A generic threshold gate scheme, which is displayed by Figure2(a), has been proposed in [Lageweg et al., 2001a]. The circuit operates as follows. The input voltages V^p (weighted by their input capacitors C^p) are added to V_j, while the input voltages V^n (weighted by their input capacitors C^n) are subtracted from V_j. The critical voltage V_c of the tunnel junction acts as the threshold value. The bias voltage V_b weighted by its input capacitor C_b adjusts the threshold value to the desired value. If the voltage V_j across the junction is less then V_c, no charge transport can occur and the circuit's output remains 'low'. If $|V_j| > V_c$, one electron tunnels through the junction (from node y to node x), resulting in a 'high' output. This scheme can therefore be used as a basis for implementing linear threshold gates with both positive and negative weights.



(a) n-input LTG. (b) Non-Inverting buffer

Figure 2. Linear Threshold Gates (LTG) and buffer.

Such threshold gates however do not operate correctly in networks due to the passive nature of the circuit. It was found in [Lageweg et al., 2001b] that augmenting the output of each threshold gate with a buffer results in correctly

operating threshold gate networks. A buffer requires active components, for which SET transistors (see for example [Chen et al., 1996] for an introduction of the SET transistor) can be utilized. If two SET transistors share a single load capacitor, such that one transistor can remove a single electron from the load capacitor (resulting in high output) while the other can replace it, we arrive at the non-inverting static buffer as displayed in Figure 2(b). The circuit can also be modified, as described in [Lageweg et al., 2002], to become an inverting static buffer. The inverting static buffer can also function as a stand-alone inverter gate. Additionally, threshold gates can also be augmented with two cascaded buffers, such that both the normal and inverted output are available. Both the generic threshold gate and the buffer operate in accordance with the single electron encoded logic (SEEL) paradigm, i.e., charge transport due to switching activity is limited to one electron. Note that the buffer/inverter can be augmented with strip resistors in order to suppress cotunneling. Referring to Figure 2(b), this is achieved by adding strip resistors between junction 1 and V_s and between junction 4 and ground as suggested in [Lotkhov et al., 2001].

In the next section we discuss a methodology to calculate the delay and power consumption of SEEL logic circuits. Focusing on the SEEL threshold gates, we subsequently analyze the maximum fanin and fanout.

4. Delay, Power, Fanin and Fanout

The tunneling of electrons in a circuit containing tunnel junctions is a stochastic process. This means that the delay cannot be analyzed in the traditional sense. Instead, one can calculate the chance that an electron has tunneled through a tunnel junction after a time interval t_d. To evaluate t_d let us first assume that a large number of tunnel events occurs one after another through a single junction at a constant rate of Γ tunnel events per second. Furthermore, assuming that n is the state in which exactly n tunnel events have occurred, and assuming that the tunnel events adhere to a Poisson distribution, the probability $P_n(t_d)$ of being in state n after t_d time can be formulated as

$$P_n(t_d) = \frac{(\Gamma t_d)^n}{n!} e^{-\Gamma t_d}. \tag{5}$$

In the case of SEEL gates, such as the buffered threshold gate discussed in the previous section, in which the state transition diagram only consists of states $n = 0$ (before the tunnel event) and $n = 1$ (after the tunnel event), $P_0(t_d)$ is the probability that the tunnel event has not occurred after t_d seconds. If the tunnel event is the desired behavior of the circuit, then $P_0(t_d)$ or $P_{error} = e^{-\Gamma t_d}$ is the chance of an erroneous output after t_d seconds. Given that an acceptable error probability P_{error}, the time t_d needed to reduce the error probability to

this value can be calculated as

$$t_d = \frac{-ln(P_{error})}{\Gamma}. \tag{6}$$

Assuming $|V_j| > V_c$, the rate at which electrons tunnel through a junction can be described as

$$\Gamma = \frac{-\Delta E}{q_e^2 R_t} \frac{1}{(e^{\Delta E/k_B T} - 1)}, \tag{7}$$

where R_t is the tunnel resistance (typically $R_t = 10^5 \Omega$), $k_B = 1.38 \cdot 10^{-23} J/K$ is Boltzman's constant and ΔE the reduction of the total amount of energy present in the circuit due to a single tunnel event, which can be expressed as

$$\Delta E = -q_e(|V_j| - V_c). \tag{8}$$

The above provide the basic framework for calculating the gate delay and power consumption of SEEL logic gates. Assuming $|\Delta E| >> k_B T$, one can combine Equations (6), (7) and (8) in order to describe the switching delay as a function of the error probability and the junction voltage as

$$t_d = \frac{-ln(P_{error}) q_e R_t}{|V_j| - V_c}. \tag{9}$$

The energy consumed by a single tunnel event occurring in a single tunnel junction can be calculated by taking the absolute value of ΔE. In order to calculate the power consumption of a gate, the energy consumption per tunnel event is multiplied by the switching frequency of the gate's output. The switching frequency in turn depends on the frequency at which the gate's inputs change and is input data dependent as a new combination of inputs may or may not results in a new output value. However, assuming that the gate's output switches at the maximum frequency $f_{max} = 1/t_d$, the theoretical maximum power consumption $P_{max} = \Delta E/t_d$ is

$$P_{max} = \frac{(|V_j| - V_c)^2}{-ln(P_{error}) q_e R_t}. \tag{10}$$

Assuming that gates operate in networks with a logic depth of 15 gates per pipeline stage, and that input data causes switching activity in half the time, we can estimate that the actual power consumption in SEEL circuits is about two orders of magnitude less then P_{max}.

Given that the SEEL threshold gate is intended to be utilized as a network component, in addition to gate delay and power consumption we also require a methodology to calculate the maximum fanin and fanout. When utilizing buffered threshold gates in a network, each gate influences the circuit node

voltages inside neighboring gates (through capacitive division), causing feedback and feed forward effects. There are two fundamental contributors to these effects. First, the bias voltage(s) of a gate influences other gates through capacitive division. Given that bias voltages are DC signals, this results in a fixed contribution, which can be compensated for in the design phase. Therefore, the DC feedback and feed forward effects are ignored in this discussion. Second, the switching behavior of a gate also influences other gates. This effect can be considered as a 'random' disturbance of voltage levels, and therefore it cannot be compensated for through fixed biasing. The amount of 'random' disturbance at which the gates will cease to correctly perform their function therefore limits the fanin and fanout of gates operating in a network.

In the remainder of this paper it is assumed that Boolean logic values (input and output signals) are represented by predefined voltage levels, such that logic $'0' = 0$ Volt and logic $'1' = V_{high}$. If all inputs have the 'ideal' voltage levels of 0 and V_{high}, a buffered threshold gate will operate correctly for any number of inputs. If the inputs are not ideal then the fanin of a gate is limited by the quality of the input signals. The quality of an input signal V_{in} is defined by the parameter d, such that $|V_{in} - V_{ideal}| \leq d \cdot V_{high}$. For example, if $V_{high} = 100$ mV and $d = 0.02$, a logic 0 can be represented by any voltage in the range $[-2\ mV, +2\ mV]$.

In a buffered threshold gate an input is part of a weighted sum. Therefore, the quality of the input signal directly contributes to the sum which limits the discrimination of the gate. In practical threshold gate implementations the threshold is usually set in the middle of two integer values in order to maximize robustness for disturbances of the weighted sum. This implies that the maximum deviation of the weighted sum from its 'ideal' value should be less then 0.5. Consider for example a 3-input buffered threshold gate with $d = 0.2$ and all input weights $\omega_i = 1$. In this case the weighted sum can deviate from the intended value by as much as of $3d = 0.6$, which can result in a wrong threshold evaluation. For our discussion we define $fanin$ as the maximum sum of the absolute values of the input weights, which can be described as

$$fanin < \frac{0.5}{d}. \tag{11}$$

For the fanout calculations the following is assumed (see Figure 2): $C_{\Sigma}^{p} = C_b + \Sigma_{k=1}^{r} C_k^p$, $C_{\Sigma}^{n} = C_o + \Sigma_{l=1}^{s} C_l^n$, C_{max}^{p} is the largest input capacitance of a positively weighted input, C_{max}^{n} is the largest input capacitance of a negatively weighted input, C_{out} is the buffer's output capacitance, $C_{out} >> C_{max}^{p}$, $C_{out} >> C_{max}^{n}$. It is also assumed that $C_{\Sigma}^{p} >> C_j$ and $C_{\Sigma}^{n} >> C_j$ for the threshold gates. If the output of a gate controls another gate via a positively weighted input and the controlled gate switches to a high output value, the total charge on node x of the threshold gate becomes $q_x = -q_e$. This charge reduces

the voltage of node x by $V_x = \frac{-q_e}{C_\Sigma^p}$. Given that $V_{high} = q_e/C_{out}$, V_x can also be described as $V_x = \frac{-C_{out}V_{high}}{C_\Sigma^p}$. The resulting feedback voltage V_{fb}^p on the output of the controlling gate is at most $V_{fb}^p = \frac{-C_{max}^p V_{high}}{C_\Sigma^p}$. Similarly, a negatively weighted input generates at most a feedback voltage $V_{fb}^n = \frac{C_{max}^n V_{high}}{C_{out}}$. If the maximum accepted deviation from ideal voltage levels is d, it is required that the sum of all feedback contributions due to fanout is less then $d \cdot V_{high}$. Therefore the following two constraints apply to fanout

$$p\_fanout < \frac{d \cdot C_\Sigma^p}{C_{max}^p} \; ; \; n\_fanout < \frac{d \cdot C_{out}}{C_{max}^n}, \tag{12}$$

where p_fanout is the fanout to positively weighted inputs and n_fanout is the fanout to negatively weighted inputs.

The next section discusses the implications of the proposed analysis methods on practical networks of buffered threshold gates. Given that we intend our discussion to be technology and application independent, we ignore the effects of interconnects on area, delay and power consumption. Also, given that it is probable that nanotechnology applications will be restricted to locally connected circuits it can be assumed that interconnects will not dominate in the area, delay and power calculations.

5. Discussion

The first practical implication of the proposed methodology, as discussed in the previous section, applies to the limits imposed on the operation temperature T. In order to ensure that the thermal energy $E_{therm} = k_B T$ does not mask the switching energy ΔE related to tunneling events, one must ensure that $\Delta E >> k_B T$. Additionally, Equation (7) implies the same in order to ensure a high tunneling rate. Assuming $\Delta E = 10 k_B T$ and utilizing Equation (8), the operating temperature as a function of $|V_j| - V_c$ is depicted in Figure 3. It can be observed that room temperature operation requires a difference of approximately 250 mV between the junction voltage V_j and the critical voltage V_c.

One of the key metrics for any novel technology is its performance it terms of gate delay. Given an error probability P_{error}, the gate delay solely depends on the tunnel resistance R_t and $|V_j| - V_c$ (see Equation (9)). The tunnel resistance depends on the physical implementation, but $R_t = 100k\Omega$ is commonly used in literature. For the switching error probability we assume $P_{error} = 10^{-12}$ as this is a reasonaly low value which can be further reduced by the application of error correction schemes if so desired. We note that smaller error probabilities can be achieved at the cost of increased delay, as suggested by Equation (9). Using the above parameter values for R_t and

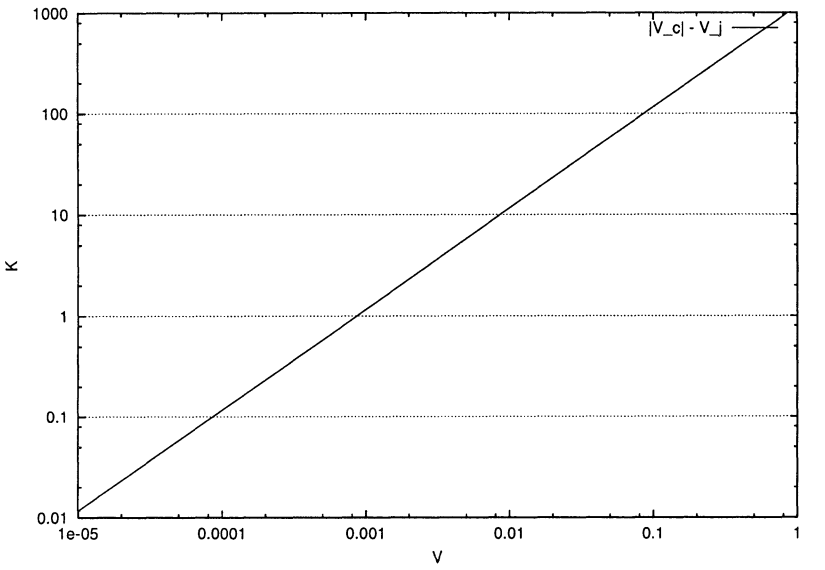


Figure 3. Maximum temperature as function of $|V_j| - V_c$.

P_{error}, the switching delay of a single junction as a function of $|V_j| - V_c$ is depicted in Figure 4. It can be observed that the switching delay is approximately 2 ps if we assume $|V_j| - V_c = 250$ mV, i.e., room temperature operation. Given that this is the delay per tunnel event, and that three tunnel events will sequentially occur in the buffered threshold gate when output switching occurs, we increase the delay estimate by a factor of 3, resulting in an estimated gate delay of 6 ps.

In order to estimate power consumption we assume $|V_j| - V_c = 250$ mV, i.e., room temperature operation, and the calculated gate delay of 6 ps for buffered threshold gates. Given these values, Equation (8) implies that the energy consumption per switching event is $\Delta E = 250$ eV, which implies $\Delta E = 750$ eV if a buffered threshold gate switches its output value (three switching events in total). Larger networks typically operate in pipelines stages, in which series of combinatorial gates are alternated with latches. If we assume 10 gate delays for a pipeline stage, the threshold gates can receive new input data every 60 ps. Assuming that data processing is synchronized by a clock, a system of system threshold gates can potentially operate on a $\frac{1}{60ps}Hz = 17$ GHz clock frequency. Assuming that new input data in 50% of the cases results in the gate switching output value, the buffered threshold gates can potentially switch output value with a frequency of 7.5 GHz. Combining the above, each

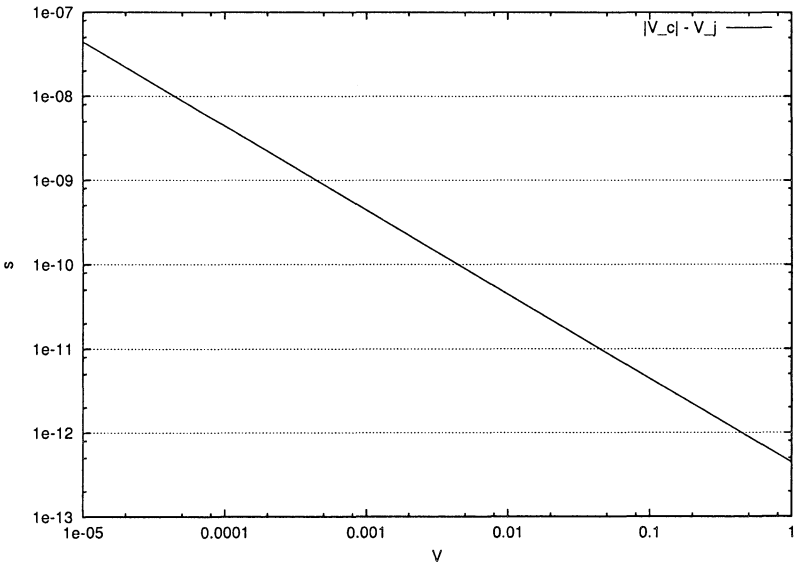


Figure 4. Switching delay as function of $|V_j| - V_c$.

gate consumes 56 nW. If we assume a heat cooling capability of 50 W/cm^2 while maintaining room temperature (100 W/cm^2 cooling capability will be required for mainstream applications by 2007 [TRS03, 2003]), we find a theoretical upper bound of 10^9 buffered threshold gates per cm^2. This is a huge improvement when compared with state-of-the-art CMOS technology that has around 10^6 standard Boolean gates per cm^2.

As discussed in the previous section, $fanin$ (see Equation (11)) is determined by the quality of the input signal d. Figure 5 depicts $fanin$ as a function of d. The maximum fanout to positively weighted inputs p_fanout (see Equation (12)) is determined by the quality d, and the ratio between the input capacitor and C^p_Σ. Figure 6 displays p_fanout as a function of d for various values of $\frac{C^p_\Sigma}{C^p_{max}}$. If for example we target a $fanin = p\_fanout = n\_fanout = 3$, this requires that $d < 0.2$, which results in the following constraints: $\frac{C^p_\Sigma}{C^p_{max}} > 9$ and $\frac{C_{out}}{C^n_{max}} > 9$. In general, increasing the ratios $\frac{C^p_\Sigma}{C^p_{max}}$ and $\frac{C_{out}}{C^n_{max}}$ results in larger fanin and fanout at the cost of larger delay, as increasing these ratios decreases the contribution of input voltages to the voltage V_j across the tunnel junction through which the charge transport occurs.

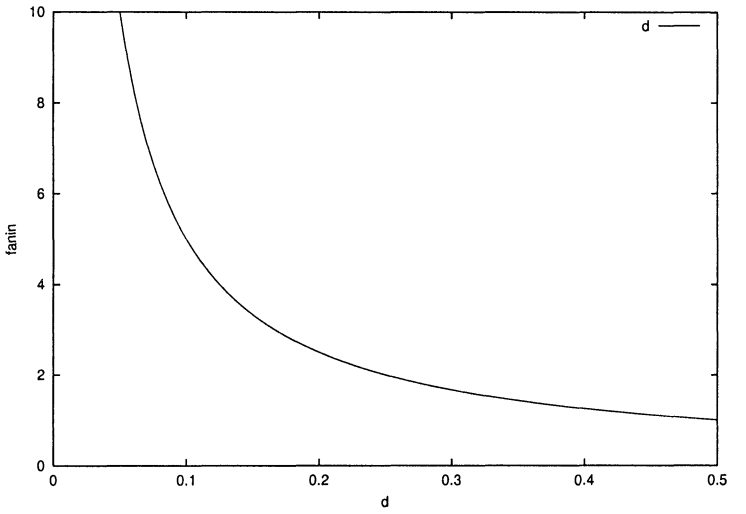


Figure 5. $fanin$ as function of the input signal quality d.

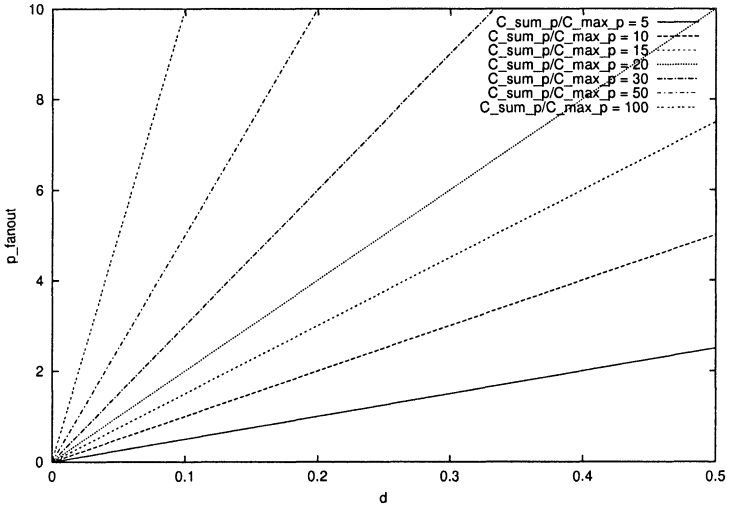


Figure 6. p_fanout as function of d for various $\frac{C_{\Sigma}^{p}}{C_{max}^{p}}$.

6. Conclusions

The SET technology allows for compact implementation of (buffered) SEEL threshold gates with both positive and negative weights. Although it is ex-

pected that, when compared with other approaches, SEEL circuits have both reduced delay and reduced energy consumptions, a method for evaluation is required. In this theoretical investigation we proposed a methodology to evaluate delay and power consumption associated with the transport of a single eletron through a tunnel junction. The proposed methodology is based on the orthodox theory and assumes that the stochatic behavior of electron tunneling adheres to a Poisson distribution. We also proposed methods to calculate the maximum fanin and fanout for such buffered SEEL linear threshold gates. Furthermore, we discussed the implications of the proposed methodology on practical networks of such gates. Our estimation indicates that buffered threshold gates operating at room temperature can potentially switch with a delay of $O(10^{-12})$ seconds and have a packing density of 10^9 gates per cm^2.

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