A Retrofit Current Sensor for Non-Intrusive Power Monitoring at the Circuit Breaker

by

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Abstract

This thesis presents a new sensor for power monitoring that measures current flow in a circuit breaker without permanent modification of the breaker panel or the circuit breaker itself. At the breaker panel, an inductive pickup and low-power amplifier sense current from the breaker face. Two coupled resonators form an inductive link that serves as a communication channel through the steel breaker panel door. A passive, balanced JFET mixer circuit transmits the sensed current signal through the inductive link by impedance modulation. Outside of the breaker panel door, sense circuitry detects the impedance modulation, and a digitally implemented compensator inverts the non-uniform frequency response of the analog sensor circuitry to reconstruct the original current signal. This sensor provides a solution for low-cost, non-intrusive retrofit of any circuit breaker panel for centralized power monitoring.

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Chapter 1

Introduction

1.1 Motivation

Given information about their level of electricity consumption, end-users will alter their usage patterns to generate substantial energy savings, according to a myriad of studies performed over the past several decades [10]. *Indirect feedback* of energy usage, meaning energy usage information that has been processed before reaching the end-user (through billing, for instance), has been shown to generate energy savings in the range of 0-10%, while immediate *direct feedback* from a meter has been shown to generate energy savings in the range of 5-15% [10, 12]. Reducing the power consumed by utility customers by just five percent would "equate to permanently eliminating the fuel and greenhouse gas emissions from 53 million cars" [1]. A 10-15% reduction "would be equivalent to the yearly power output of 16 nuclear power plants or 81.3 million tons of coal" [14].

Feedback that is *disaggregated by end-use*, so that energy information is provided on an appliance or device basis, is even more advantageous because it allows users to better understand *how* energy is used in a building. Research in environmental psychology has shown that "people tend to overestimate the effectiveness of conservation measures that depend on changes in short-term behavior such as turning off the lights when leaving a room," while underestimating long-term solutions such as appliance replacement, retrofitting, or renovation [14]. Feedback disaggregated by

end-use can help clear such misconceptions through the intelligent presentation of appliance-centric energy usage information.

Unfortunately, energy monitoring systems that are disaggregated by end-use can be difficult to install and prohibitively expensive, as they often require sensors attached to the various devices and appliances to be monitored (known as "Distributed Direct Sensing") [10, 14]. As an alternative to this, centralized power monitoring systems have been developed that promise lower sensor counts than other "per-load sensor" systems. References [9, 11, 15, 18, 20, 23–25, 27, 28, 30, 31] describe centralized power monitoring approaches in which loads are identified and then monitored according to their current signatures, which can be detected with a single current sensor at the main circuit breaker panel.

In such centralized power monitoring approaches, closed or "clamp" core sensors wrapped around the utility feed are typically used to provide electrical current information from the circuit breaker panel. However, these sensors are impractical in many retrofit applications. For instance, skilled labor is required to separate line and neutral in order to deploy a wrap-around sensor, and in some industrial environments, electrical service interruption may be intolerable or prohibitively expensive.

This thesis proposes an alternative retrofit current sensor specfically aimed at widespread and accessible power monitoring. This sensor measures the current in the utility feed by sensing the resulting magnetic field at the face of the main (or secondary) circuit breaker in a standard breaker panel where the line and neutral current-carrying elements are already separated. Since direct access to current-carrying elements within the breaker panel is not necessary, skilled labor is not required for installation. Furthermore, the sensor can be interrogated through the steel panel door with no direct panel contact, permitting the door to remain closed in compliance with safety regulations.

The U.S. Department of Energy has identified "sensing and measurement" as one of the "five fundamental technologies" essential for driving the creation of a "Smart Grid" [1]. Consumers will need "simple, accessible. . . , rich, useful information" to help manage their electrical consumption without interference in their lives [1].

The sensor described in this thesis is presented as a potential solution to the financial and technical barriers-to-entry limiting the proliferation of electricity consumption feedback systems disaggregated by end-use. Both vendors and consumers will likely find innumerable ways to mine the energy usage information from such systems if it are made readily available in a useful form.

1.2 Thesis Overview

A block diagram of the retrofit current sensor is shown in Figure 1-1. It consists of the following components:

- An inductive pickup for sensing current from the circuit breaker face.
- An ultra-low-power or passive pickup amplification stage (Pickup Amp).
- An inductive link designed to transmit power to the sensing electronics at the breaker face, and act as a communication channel through the steel door.
- A balanced JFET modulator circuit for transmitting information through the inductive link (JFET Mixer).
- Drive, sensing, and demodulation circuitry that facilitates communication through the inductive link.
- A digital filter that inverts the non-uniform frequency response of the sensor.

The sensor operates as follows. Magnetic flux produced by electrical current in the circuit breaker is sensed and transduced to a voltage by the inductive current-sense pickup on the face of the circuit breaker. That voltage is amplified by an ultra-low power or passive amplification stage larger voltage signal V_{sense} that is proportional to the current sensed in the breaker. This voltage can be measured and utilized directly in applications for which a circuit breaker panel door is not an obstruction, such as in the monitoring of doorless secondary breaker panels or temporary diagnostic applications of the sensor.

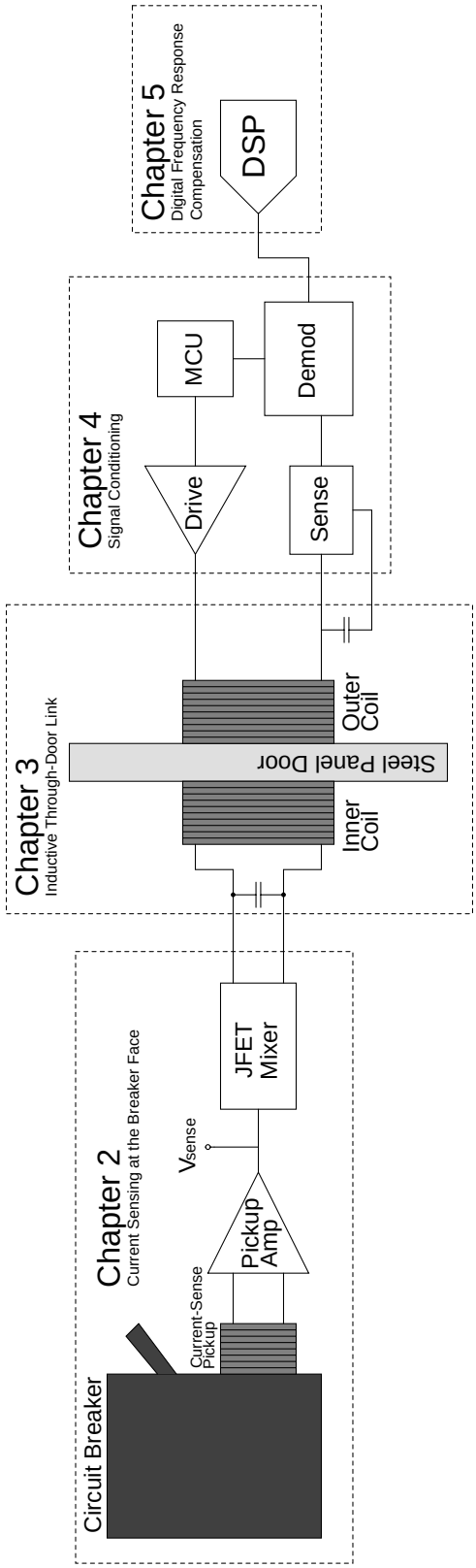


Figure 1-1: Diagram of the retrofit current sensor design.

In most permanent installations, where the panel door must be closed in order to comply with safety code, sensed current information is transferred through an inductive link consisting of two coupled resonators, one on either side of the door. Each resonator consists of a coil secured to the steel door and a discrete resonant capacitor. Through-door communication is achieved by sensing the impedance of the JFET mixer circuit through the inductive link. The link is driven from the outside with a high-frequency oscillating voltage, while the impedance of the JFET mixer varies with the low-frequency current sensed at the breaker faced. The result is an amplitude modulation of the high-frequency drive signal that can be sensed outside the panel door. Demodulation and signal conditioning circuitry downconvert the sensed amplitude-modulated signal to baseband. After a digitally-implemented frequency response compensation filter that inverts all nonuniform magnitude and phase shifts of the current sense circuitry and inductive link, the original current signal sensed at the breaker face is reconstructed outside the panel.

The system components placed directly at the breaker face, including the breaker pickup, pickup amplifier, and mixer are discussed in Chapter 2. Analysis and experimental design of the inductive link is discussed in Chapter 3. The external drive, sense, and demodulation circuitry is discussed in Chapter 4. Design of the digital frequency response compensation filter is discussed in Chapter 5. Chapter 6 provides all the details of our complete experimental setup, and lists measured system specifications. We conclude the thesis in Chapter 7 with a summary of our results and a consideration of future work. Appendicies include all relevant schematics, CAD drawings, source code, and experimental data, as well as application and design notes for the sensor.

1.3 Thesis Contributions

Previous work demonstrated preliminary results from similar sensors in [7, 8]. This work presents improved modelling and a more detailed analysis of all system components. Two new designs are presented for the pickup amplifier stage, including

an ultra-low power instrumentation amplifier that can be used independently of the through-door link in applications where the circuit breaker panel door need not be closed or does not exist. In addition to improved modelling and simulation of the through-door link, this work presents a new configuration of permanent magnets on the panel door that better saturates the steel. The sense and demodulation circuitry has redesigned to reduce the thermal noise floor while using fewer, less expensive discrete parts. A new digital filter is introduced that compensates the sensor to produce a flat frequency response. New experimental results are presented demonstrating a 8-bit resolution, sensing of currents as low as 20 mA, and a total harmonic distortion of less than 0.01%.

Chapter 2

Current Sensing at the Circuit Breaker Face

This chapter describes the current-sensing electronics attached directly to the circuit breaker face. The current-sensing interface performs two functions:

- Detect current passing through a particular circuit breaker.
- Up-modulate the sensed current signal for transmission through breaker panel door.

The breaker current is detected with an inductive current-sense pickup discussed in Section 2.1, and is transmitted through an inductive link out of the circuit breaker panel by a passive JFET modulator discussed in Section 2.2. These two elements are coupled together with an amplification stage designed to add gain to the sensed current signal and drive the modulator. Design of the amplification stage is discussed in Section 2.3.

Because the current-sensing electronics are enclosed behind the door of the circuit breaker panel, the circuits within must be inherently ultra-low power or passive. The active circuits presented in this chapter are sufficiently low power to operate for 5 months on a pair of 11.4mm diameter SR44 silver-oxide coin-cell batteries.

2.1 Current-Sense Pickup

The current sensor is a passive inductive pickup made of a high-permeability ferrite half-toroid. The choice of a inductive sensor is motivated by the fact that active current-sensing mechanisms, such as hall-effect sensors, use prohibitively too much power to be practical for a long-term installation in the circuit breaker panel.

2.1.1 Overview of Inductive Current Sensing

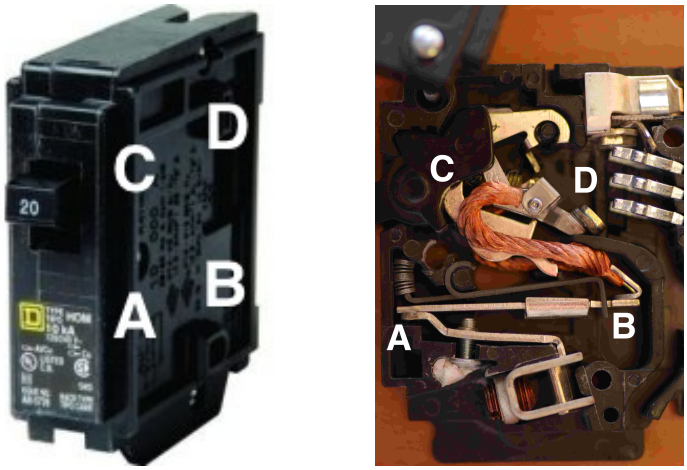
Inductive current sensing is a way of measuring electrical current by sensing the magnetic fields produced by the movement of charge that composes the current. These magnetic fields are described by Ampere's law as closed contours around the current:

$$\oint_C \vec{H} \cdot d\vec{s} = I \tag{2.1}$$

where $\vec{H}$ is the magnetic field intensity and I is the current enclosed within the contour C. Induction occurs via the electrical potentials that exist across the closed contours around these magnetic fields, which are proportional to the time derivative of the magnetic flux density of the field, $\mu\vec{H}$, as expressed by Faraday's law of induction:

$$V = \oint_C \vec{E} \cdot d\vec{s} = -\frac{d}{dt}\int_S \mu\vec{H} \cdot d\vec{a} \tag{2.2}$$

where V is the potential composed of the electric field $\vec{E}$ integrated around the closed contour C, and $\vec{a}$ is the area of the contour. In an inductive current sensor, the changing magnetic flux generated by the electrical current is focused through a contour of conductive material like the magnet wire used in our sensor, so that an electrical potential proportional to the current, given by Equation 2.2, can be measured across the material. In our current sensor, we aim to focus magnetic flux generated by the current inside a circuit breaker through turns of wire in order to generate such an electrical potential that can be amplified and transmitted out of the breaker panel.



(a) Breaker Enclosure (b) Breaker Cross-Section

Figure 2-1: Typical 20A circuit breaker and cross-section.

2.1.2 Circuit Breaker Construction

A typical low-voltage circuit breaker adhering to UL 489 design standards [32] is shown in Figure 2-1a[1]. This sort of circuit breaker is used commonly in the United States in electrical distribution panels in both homes and commercial buildings. A cross-section of such a circuit breaker is shown in Figure 2-1b. The disconnection mechanism inside the breaker consists of a small bimetallic strip (A) connected to an actuator mechanism (B). As current passes through the bi-metallic strip, it bends the actuator downwards, releasing a catch (C) that separates electrical contacts (D).

2.1.3 Placement of Current Sensor

As can be seen in the cross-section, the current path through the bi-metallic strip passes directly adjacent to the face of the circuit breaker, below the switch. Since the net flow of current is predominantly vertical inside the circuit breaker, we expect the magnetic field produced by the current to wrap horizontally around the current-carrying components of the breaker. Since the breaker enclosure is made out of low-permeability molded plastic, we also expect the magnetic fields to pass through

[1]Photo of Square-D® QO-Series® breaker enclosure photo by Schneider Electric. Available at `http://products.schneider-electric.us/products-services/products/circuit-breakers/miniature-circuit-breakers/qob-circuit-breakers/`

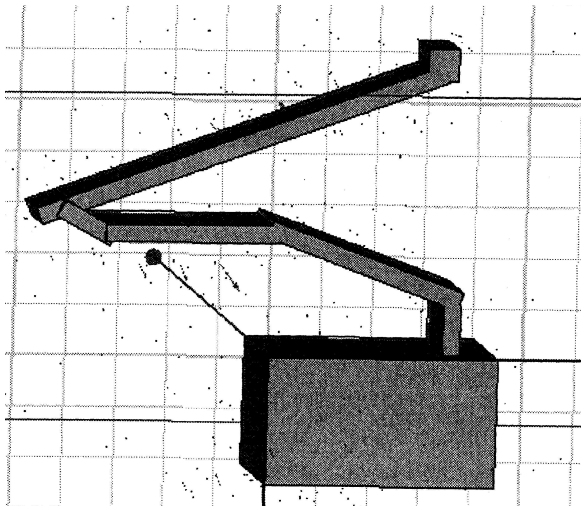


Figure 2-2: Ansoft Maxwell 3D model of circuit breaker [7].

the lower face, making it an appropriate location to place the current-sense pickup.

In [6–8], Ansoft's Maxwell 3D was used to model the magnetic fields generated by the current-carrying components inside this type of circuit breaker. The geometry of the model in Figure 2-2 was designed to match the geometrty of the bi-metallic strip, actuator, and catch mechanism. Simulations of the magnetic fields outside the breaker enclosure demonstrated that they are indeed strongest and most uniform at the lower face of the breaker, confirming it as an ideal location for the current-sense pickup.

Various shapes were considered to yield the maximum possible concentration of magnetic flux in the pickup core. Simulations using Maxwell 3D indicated that fields outside the lower face of the breaker approximate the circular shape of fields generated by a simple linear current-carrying wire, suggesting that a high-permeability half-toroid of similar shape would focus the most magnetic flux. Simulations using Finite Element Magnetics Modeling software (FEMM)[2] verified that such a toroid placed on the breaker face was suitable. A typical FEMM simulation is depicted in Figure 2-3. In both Maxwell 3D and FEMM simulations, the plastic enclosure of the circuit breaker was modeled as air.

[2]FEMM is a suite of programs for solving low frequency electromagnetic problems on two-dimensional planar and axisymmetric domains. It was written by David Meeker and is available free of charge at `http://www.femm.info/wiki/HomePage`.

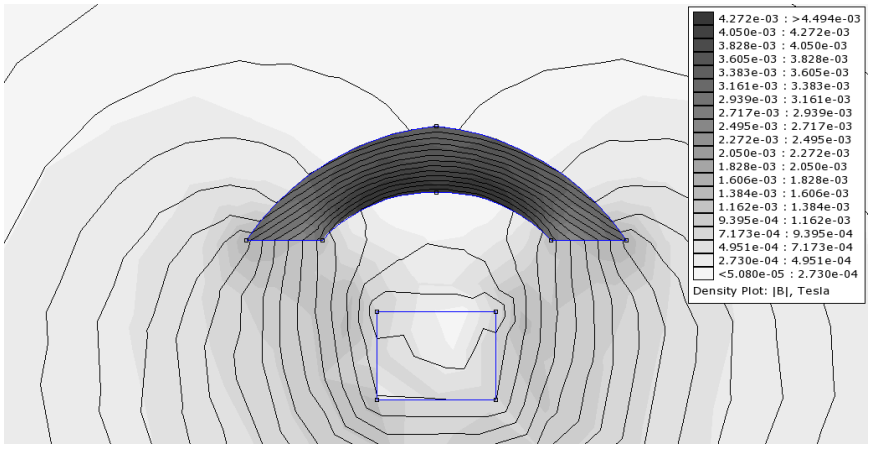


Figure 2-3: FEMM simulation of breaker and attached toroid.

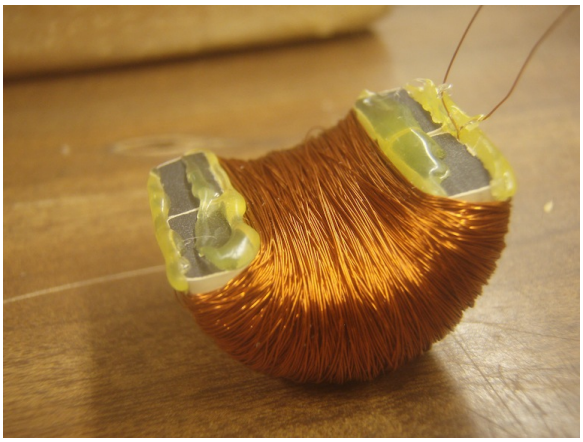


Figure 2-4: Inductive current-sense pickup.

2.1.4 Current Sensor Construction and Modeling

Construction

The current-sense pickup is designed to maximize magnetic flux concentrated in the core, by making both the relative permeability and the cross-sectional area of the core as large as possible. The magnetic yoke is formed from a Ferroxcube TX-25/15/10-3E6 core with an initial relative permeability of 12,000 [13]. The toroidal core is cut into two halves and then joined for increased cross-sectional area. The magnetic flux concentrated by the core is transduced to a voltage signal by many turns of fine-gauge magnet wire, as shown in Figure 2-4. The high number of turns is first motivated by the need for sufficient voltage to drive the JFET mixer described in Section 2.2 after

an amplification stage, but also because the signal-to-noise ratio of the sensed signal increases as the square root of the turns count. This order of growth originates from the fact that white noise generated by parasitic resistances in the pickup windings goes as the square root of the resistance, which is linearly proportional to the turn count, while the voltage simply goes linearly with the turn count, to the extent that the breaker acts as a flux source:

$$V_{sense} = \frac{d}{dt}\int_S \mu\vec{H}\cdot d\vec{a} \approx \frac{d}{dt}\mu H N A_C \tag{2.3}$$

assuming that the magnetic field intensity $\vec{H}$ is uniform throughout the core, where N is the number of turns of magnet wire, and A_C is the average cross-sectional area of those turns. The root-mean-squared (RMS) voltage noise of the parasitic resistance of the windings, which goes only as the square root of the parasitic winding resistance, is given by,

$$\sqrt{\overline{v_n^2}} = \sqrt{4kTR}\ \mathrm{V}/\sqrt{\mathrm{Hz}} \tag{2.4}$$

where R is the parasitic resistance, k is the Boltzmann constant, and T is the temperature of the wire in Kelvin.

Modelling and Validation

We can model the breaker and attached pickup as a current source connected to a simple 1:N transformer with magnetizing inductance L_m, leakage inductance L_l, and parasitic series resistance R_S. A schematic of this model is shown in Figure 2-5. A current source is chosen to represent the signal from the breaker current because of the inherent high-impedance of the power circuit - that is, the voltage drop across the load in the power circuit is large relative to the change in voltage across the circuit breaker caused by attaching the sensor. Because the transformer primary is driven with a current source in our model, a primary-side leakage inductance would have no effect on the observed voltage at the secondary, so only the secondary-side leakage inductance L_l is included.

To validate this model under open-circuit conditions, several pickups were wound

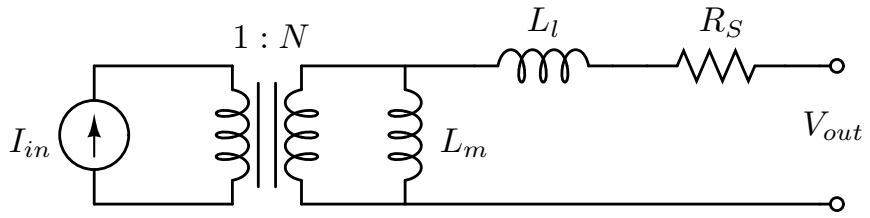


Figure 2-5: Circuit model for inductive current-sense pickup.

Turns Count	R_{DC} (Ω)	mΩ/Turn	L (mH)	A_l (nH/Turn^2)	mV_{pp}	μV/Turn
250	11.8	47	3.2	51.2	3.5	14
500	24.5	49	14.1	56.4	9.5	19
750	37.5	50	30.0	53.3	14.3	19
1000	51.0	51	51.0	54.0	20.0	20
2000	118.0	59	210	52.5	38.0	19

Table 2.1: Measured properties of wound pickups, by turn count. Voltage across the pickup is measured in an open-circuit configuration, while the pickup is placed on a breaker carrying 5 A RMS. Inductance is measured at 60 Hz.

with 35AWG magnet wire at varying turn counts. The inductance and series resistance at of each pickup at 60 Hz was measured with an HP4192A Impedance Analyzer, and the peak-to-peak open-circuit voltage of each pickup was measured when placed on a breaker carrying a 5A RMS 60 Hz test current. These measurements are listed in Table 2.1. They demonstrate that the open-circuit pickup voltage goes linearly with turns count, as the model suggests. The measurements also show that the net inductance goes as N^2, and the series resistance goes slightly faster than linearly with N because the average turn circumference slowly grows with the turn count.

To validate the model under loaded conditions, a pickup with $N = 2000$, $L = 210$mH and $R_S = 118\Omega$ was loaded with various load resistors and placed on a circuit breaker carrying a 5 A RMS current. For each load resistor, the output voltage of the pickup was measured as a function of frequency. The transfer function from sensed current to the output voltage pickup can be shown to be

$$\frac{v_O}{i_I}(s) = \frac{sL_mR_L}{N(R_L + R_S + sL)} \tag{2.5}$$

according to our model in Figure 2-5, where $L = L_l + L_m$ is the net pickup inductance

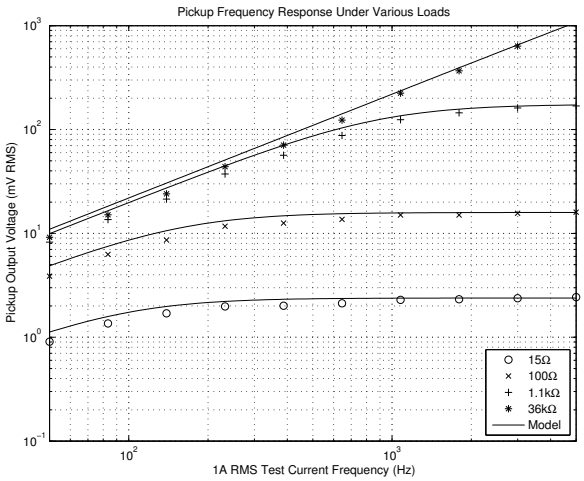


Figure 2-6: Experimental results for validation of model current-sense pickup. Results predicted by model are shown as solid lines.

and R_L is a load resistor attached across the output terminals of the pickup.

Equation (2.5) implies that for low frequencies, we expect the magnitude of the output voltage to increase at 20dB per decade, but as frequency increases and the denominator begins to be dominated by the leakage inductance term, the response will flatten out to:

$$\frac{v_O}{i_I}(\omega \gg (R_L + R_S)/L) \approx \frac{L_m R_L}{NL} \tag{2.6}$$

The measurements of the loaded pickup are plotted in Figure 2-6 and match the shape of the frequency response predicted by Equation 2.5. We can use the settling points of the loaded frequency response data curves to approximate the magnetizing inductance:

$$L_m \approx N\frac{L}{R_L}\left|\frac{v_O}{i_I}(\omega \gg (R_L + R_S)/L)\right| \tag{2.7}$$

We use this approximation to fit our model to the data. Applying Equation 2.7 to the 5 kHz datapoint for the 100 Ω load, we find that $L_m \approx 70\,\text{mH}$. That gives us $L_l = L - L_m \approx 150\,\text{mH}$. Using these parameter estimates, we plot the model of Equation (2.5) alongside the data in Figure 2-6. It closely matches the measured data. MATLAB® code for plotting this data and the associated model is given in Appendix E.2.1.

Tamura MET-01 Properties			
Terminal	R_S	L_l	L_m
Primary	300 Ω	5 mH	500 mH
Secondary	10 kΩ	10 H	100 H

Table 2.2: Measured properties of the Tamura MET-01 1:14.1 audio transformer. Measurements were performed at 60 Hz.

Turn Count and Wire Gauge Selection

Using the model in Figure 2-5, we can determine the appropriate turn count and wire gauge necessary to maximize the pickup voltage for a given load presented by the amplification stage. In Section 2.3, we present two designs for the amplification stage: a passive transformer-based design, and an active instrumentation amplifier-based design.

In the case of the instrumentation amplifier, there is negligible loading on the pickup because the input terminals of the instrumentation amplifier, an Analog Devices AD627A, have an ultra-high input impedance equivalent to $20G\Omega$ in parallel with 2pF [4]. Furthermore, since the amplifier is an active device, it has input voltage noise, which is in fact far higher than any level of thermal noise that could reasonably be produced by parasitic resistances in the pickup windings. This implies that our signal-to-noise ratio increases linearly with N in this circuit, and since the instrumentation amplifier can operate over a wide range of gains, we must simply select a sufficient number of turns to reach a SNR that does not limit the performance of our system. Given the pickup volts/turn ratios given in Table 2.1, and given the typical AD627 input voltage noise of $38\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ [4], the sensor will be able to measure milliamp signals with 320 turns or more in this configuration. The wire gauge must selected to allow sufficient space on the pickup for the number of turns desired, but otherwise does not affect sensor performance.

The transformer load, on the other hand, has fixed, finite inductive and resistive components, and will attenuate the induced voltage on the pickup if either the leakage inductance or the parasitic resistance of the pickup windings become too large. The transformer load can be modeled as shown in the schematic in Figure 2-7, with

leakage inductances and series resistances on the primary and secondary sides, and a magnetizing inductance between the two. Here we refer to the primary as the "low turns" winding of the transformer, and the secondary as the "high turns" winding, shown connected to v_{IN} and v_{OUT} respectively in Figure 2-7.

A simulation was designed to determine the appropriate turn count and wire gauge for a pickup with a transformer load. The simulation populates transformer model in Figure 2-7 with component values measured on a Tamura MET-01 1:14.1 audio transformer, given in Table 2.2. The values for the pickup model elements in Figure 2-5 are extrapolated from an average of the resistance-per-turn and inductance-per-turn-squared data in Table 2.1, so that for any given simulated turns ratio:

$$R_S = N \cdot 51\,\mathrm{m\Omega}$$
$$L_l = N^2 \cdot 53.5\,\mathrm{nH/N^2}$$

Using these models, the simulation plots the transformer secondary voltage at 60 Hz for a 5A RMS current when the transformer primary is connected to the current-sense pickup. The results, shown in Figure 2-9, are parameterized by the number of MET-01 transformers connected to the pickup in the parallel-series configuration shown in Figure 2-8, and by various configurations of the pickup windings, with gauges ranging from 25 to 40 AWG and turns counts ranging up to the maximum possible for a particular gauge.

The plots demonstrate that with a small number of transformers connected to the pickup, the effect of greater attenuation from increased pickup windings does not offset the corresponding increase in induced voltage until the wire gauge is as small as 40 AWG. The plots furthermore show that for this circuit topology, 1500-2000 turns of 35 AWG wire yields the highest output voltage for a small number of transformers. For this reason the 2000 turn, 35 AWG pickup in the bottom row of Table 2.1 was selected for our experimental setup, which is discussed in deatil in Chapter 6. MATLAB® code for this simulation is given in Appendix E.2.2.

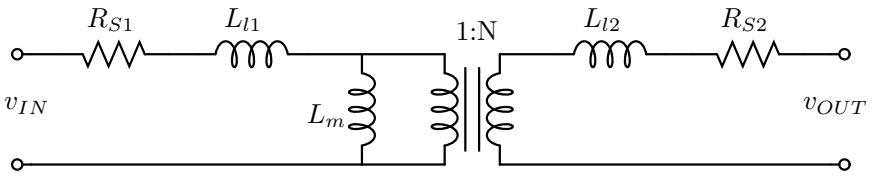


Figure 2-7: Circuit model for Tamura MET-01 Audio Transformer.

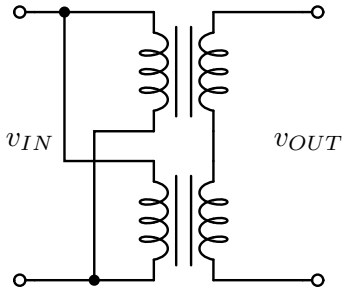


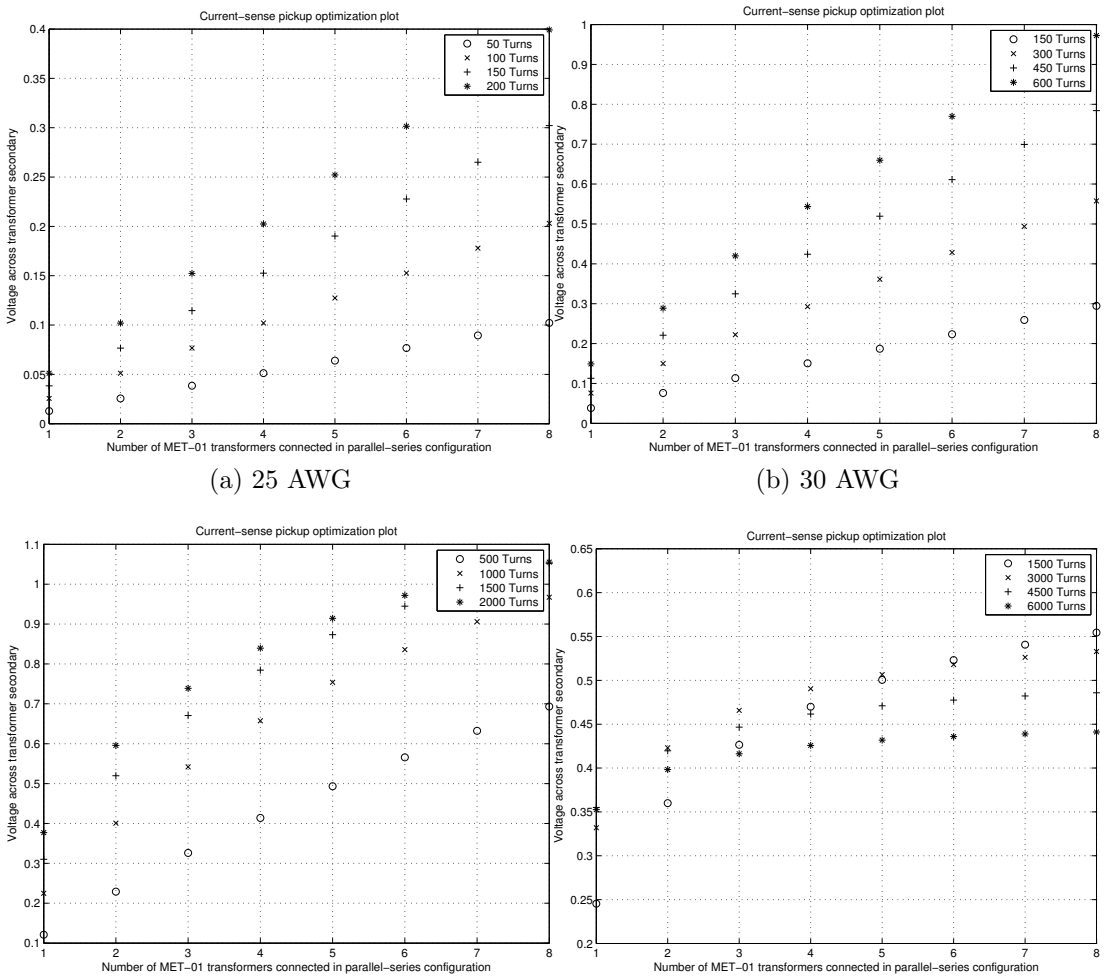
Figure 2-8: Parallel-series configuration of multiple transformers.

2.1.5 Sensor Frequency Response and Compensation

The frequency response of the current-sense pickup is inductive. That is, the output voltage of the pickup increases linearly with frequency for a current of constant amplitude, as demonstrated with a 2000-turn pickup in Figure 2-6. This comes directly from Faraday's law of induction 2.2: if we assume that the magnitude of the magnetic field intensity $|\vec{H}|$ is uniform throughout the pickup core, and takes the form of a sine wave with frequency ω and an amplitude of 1, then the induced voltage will be:

$$\omega \mu N A_C \cos(\omega t) \tag{2.8}$$

This sort of frequency response is helpful because it produces more of the frequencies we are interested in for NILM post-processing: the higher harmonics of the fundamental 60 Hz current. However, the response is also problematic because the voltage induced on the uncompensated pickup will be dominated by signals of even higher frequencies than those in our band of interest. As an example, Figure 2-10 shows high-frequency zero-crossing transients detected by an open-circuited uncompensated current-sense pickup that are almost imperceptible in the original current signal. Unless these high-frequency signals are attenuated, they will saturate the JFET mixer



(a) 25 AWG

(b) 30 AWG

(c) 35 AWG

(d) 40 AWG

Figure 2-9: Pickup-transformer inter-stage loading simulation.

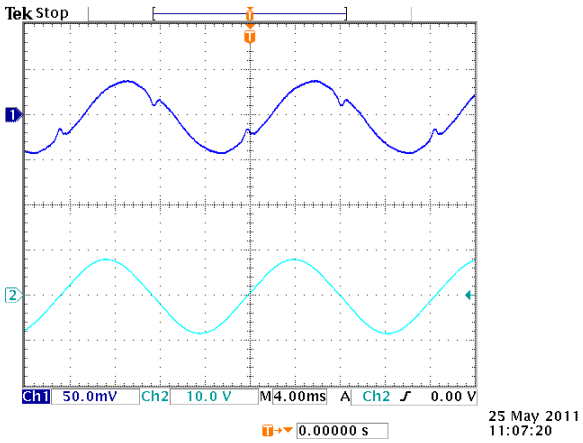
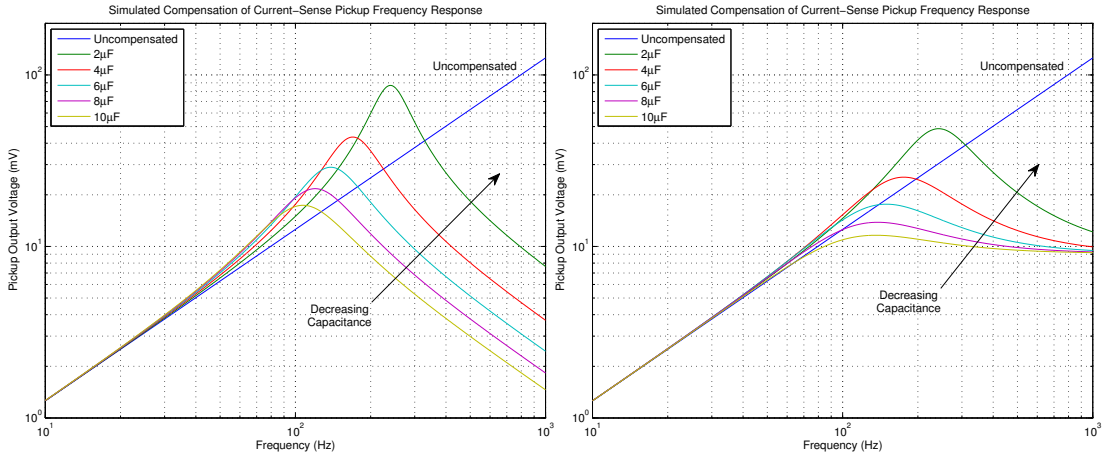


Figure 2-10: Pickup responding to high-frequency zero-crossing transients. Light blue: voltage across 2Ω load resistor carrying test current. Dark blue: secondary voltage of 1:14.1 transformer connecter to pickup.

and reduce the linearity of the system.

We compensate the inductive frequency response of the pickup by placing a capacitor in parallel with its terminals. The capacitor is selected to resonate with the pickup inductance at a frequency within our band of interest, so that the response begins to roll off as frequencies continue to increase. Figure 2-11 shows an LTSPICE simulation of this effect with various capacitor values. The simulation was run with data measured on the 2000-turn pickup in Table 2.1. The simulated plots show the frequency response of the open-circuited pickup, parameterized by the resonant capacitor value. As the capacitance is decreased, the resonant point moves higher in frequency and the quality factor of the resonator is increased, raising the response at 60 Hz as well as at the resonant point. In our experimental setup, a 10 μF capacitor was used to compensate the inductive frequency response of the 2000-turn pickup.

If desired, the frequency response can be "flattened" by adding a resistor in series with the capacitor, lowering the Q for any given resonant frequency, as shown in Figure 2-11b. If the transformer-based amplification stage is used, another resonant capacitor can be added to the transformer secondary to further shape the frequency response by resonating with the magnetizing inductance of the transformer.



(a) Capacitor (b) Capacitor with 100Ω series resistor

Figure 2-11: Simulation of frequency response compensation of current-sense pickup using a parallel resonant capacitor.

2.2 JFET Mixer

The four-quadrant balanced passive JFET modulator (mixer), shown in Figure 2-12, is designed to transmit information from the current-sense pickup through the inductive link and out of the breaker panel. The circuit consists of two JFET devices for modulation control and two resistors for current limiting at the gate junctions of the JFETs, but it does not require a DC power supply. The passive topology is motivated by the fact that the power constraints inside the breaker panel prohibit any kind of circuit that could actively drive the through-door coils. Instead, the modulator presents a varying impedance to the coil, which is actively driven from outside the breaker panel. The two-JFET mixer circuit is particularly advantageous for this application because it requires a minimal amount of circuitry behind the breaker door and lends itself to a low-cost solution.

In this section, we first discuss the operation of the mixer circuit from an intuitive, qualitative perspective. We subsequently proceed to employ models of the JFET device for both hand analysis and SPICE simulation in order to gain a more quantitative understanding of the circuit.

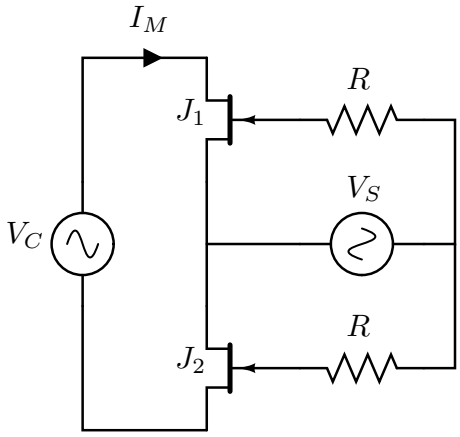


Figure 2-12: Schematic of passive, balanced, adaptive referencing, two-JFET modulator circuit.

2.2.1 Intuitive Description of Mixer Operation

During operation, both JFET devices are nominally operating in their linear region, so the mixer can be modeled as a time-varying resistive load on the carrier voltage source V_C in Figure 2-12, that corresponds to the voltage on the coil on the inner side of the breaker panel door. This load varies with control signal V_S, applied to the JFET gates and leads to a corresponding modulation of the mixer current I_M. For this description of the mixer operation, we assume that V_S is small and any voltage across the gate resistors is negligible.

The JFET is a normally-on device that requires a negative gate-to-source voltage, V_{GS} to turn it off. It may be modeled as a symmetric device, so that the drain and source are interchangable and determined by which leg of the JFET has the lower potential. On positive half-cycles of the carrier waveform ($V_C > 0$), the source of each device is the lower leg, and the drain is the upper leg. The gate-source voltage of the lower device is the positive-valued drain-source voltage of the device itself added to V_S. If the 60 Hz signal, V_S, is sufficiently small, the lower device maintins a strictly positive gate-source voltage for most of the positive half-cycle of the carrier signal. Thus the lower device can be taken to be "fully on" during that time, well-modeled by a small resistance. Meanwhile, the upper device has a gate-to-source voltage that is simply V_S. Again, if the 60 Hz signal, V_S, is sufficiently small, the upper device

maintains a gate-source voltage that *may not be* strictly postive so that its incremental resistance, which dominates the mixer circuit during the half-cycle, varies according to the 60 Hz signal measured from the current-sense pickup at the breaker face. In general, the gate-source voltage for the lower device contains a positive DC offset compared to that of the upper device even if it is not strictly positive.

The roles of the two devices reverse when the polarity of the carrier signal reverses. The result is a modulation of the carrier signal current by the 60 Hz signal. The JFET mixer is adaptively-referencing because during both positive and negative half-cycles of V_C, one device is fully-on, referencing the source of the other device to the low-potential end of the mixer circuit.

2.2.2 Analysis of Mixer Operation

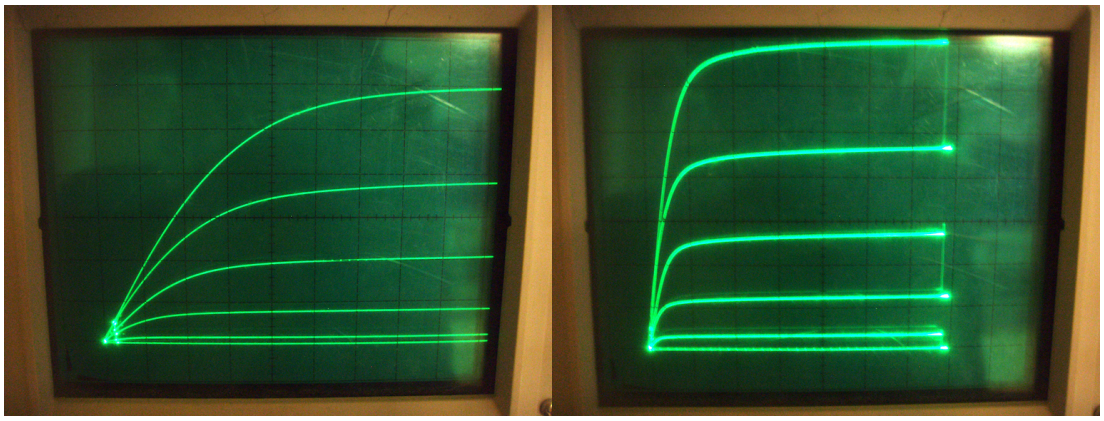
JFET Modeling

The n-channel junction field effect transistor (JFET) is a three-terminal voltage-controlled device. Like its more common counterpart, the MOSFET, current flows through a semiconductor channel between the "source" and "drain" terminals. The JFET is a normally-on device, so with zero bias between the "gate" and "source" terminals, V_{GS}, there is a drain-to-source current I_{DS}. As V_{GS} is decreased, the channel is "pinched" so that I_{DS} is reduced until V_{GS} reaches a "pinch-off" voltage V_P, at which point no current flows between the drain and source.

A typical I-V plot of JFET characteristics is shown in Figure 2-13. Like a MOSFET, the JFET operation characteristic is divided into a linear region where I_{DS} is roughly linearly dependent on V_{DS}, and a saturation region where I_{DS} has only a weak dependence on V_{DS}. The characteristic equations of the JFET are:

$$I_{DS} = \frac{2I_{DSS}}{V_P^2}(V_{GS} - V_P - \frac{V_{DS}}{2})V_{DS} \quad \text{Linear Region, } V_{DS} < V_{DS_{SAT}} \tag{2.9}$$

$$I_{DS} = I_{DSS}(1 - \frac{V_{GS}}{V_P})^2 \quad \text{Saturation Region, } V_{DS} > V_{DS_{SAT}} \tag{2.10}$$



(a) 0.2V/Div Horizontal (b) 1.0V/Div Horizontal

Figure 2-13: Typical PN4117A I-V curves, demonstrating (a) linear and (b) saturated operation. Vertical scale is 10μA/Div

where the transition between the linear and saturation regions occurs at:

$$V_{DS_{SAT}} = V_{GS} - V_P \tag{2.11}$$

Mixer Analysis

The voltage relations governing the operation of the mixer, derived directly from the JFET model presented above, are:

$$V_{GS1} = Vs \tag{2.12}$$

$$V_{GS2} = V_{DS2} + V_S \tag{2.13}$$

$$V_{DS1} + V_{DS2} = V_C \tag{2.14}$$

Where V_C has been abbreviated as V_C, V_S as V_S, and I_M as I_D. The drain currents of the JFETs, $I_{D1} = I_{D2} = I_M$, depend on the operating regions of the devices. We can easily determine the operating region of the lower JFET, J_2, by combining equations 2.13 and 2.11 to show that:

$$V_{DS2_{SAT}} = V_{DS2} + V_S - V_P \tag{2.15}$$

Since the saturation voltage of J_2 depends directly on its own drain-to-source voltage, it can only saturate if the voltage from the pickup amplifier becomes negative enough to exceed the pinch-off voltage of the transistor. Doing so would push J_1 into cutoff and ruin the linearity of the mixer. We do not expect to drive the JFET gates at levels beyond the pinch-off voltage, so it is assumed that for our operating range, J_2 never saturates.

The saturation voltage of J_1, on the other hand, is simply $V_{DS1_{SAT}} = V_S - V_P$, and does not depend on the drain-to-source voltage of the transistor, which may enter saturation for sufficiently high V_C. If we assume operation in the linear region, as desired, the equations for the mixer current I_M are:

$$I_D = \frac{2I_{DSS}}{V_P^2}(V_{GS1} - V_P - \frac{V_{DS1}}{2})V_{DS1} \tag{2.16}$$

$$I_D = \frac{2I_{DSS}}{V_P^2}(V_{GS2} - V_P - \frac{V_{DS2}}{2})V_{DS2} \tag{2.17}$$

When we combine these with equations with Equations (2.12)-(2.14), it can be shown that when operating in the linear region, the drain-to-source voltage of J_1 is given by:

$$V_{DS1} = \frac{V_C - 2V_P + V_S - \sqrt{-V_C^2 + (2V_P - 2V_S)^2}}{2} \tag{2.18}$$

Equating this expression to $V_{DS1_{SAT}}$ shows us that the saturation threshold is a linear innequaulity of V_C and V_S:

$$V_{C_{SAT}} > \sqrt{(}2)(V_P - V_S) \tag{2.19}$$

which is plotted in Figure 2-14. The equation and corresponding plot confirm that for sufficiently small V_C and V_S, both J_1 and J_2 will consistently operate in their linear regions over the entire operation region of the mixer. Given this condition, the mixer

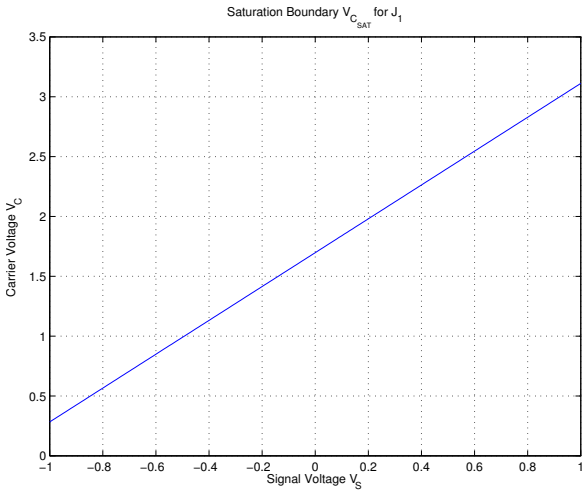


Figure 2-14: Saturation boundary for J_1, $V_{C_{SAT}}$, assuming positive V_C.

current can be shown to be:

$$I_M = \frac{I_{DSS} V_C \sqrt{-V_C^2 + (2V_P - 2V_S)^2}}{2V_P^2} \tag{2.20}$$

which is confirmed by simulation in the following section.

One last aspect of the modulator circuit that we have not addressed is the gate resistors. Assuming that the JFET gates are consistently high impedance, these resistances should have no effect on the mixer behavior. However, for large levels of V_S, the drain-source drop across the lower JFET, V_{DS2} may become positive enough as to activate the parasitic diode at the PN junction from the gate to the source of the device. Because the mixer impedance is already dominated by J_1 during this stage of the operation cycle, the "turn-on" of this diode does little to change the circuit behavior as viewed from the perspective of the attached door coil. However, when the active instrumentation amplifier gain stage is employed, this current path, which passes through the amplifier, will draw needless amounts of power from the batteries powering the circuit. A pair of 100kΩ resistors will limit this current so that is negligible compared to the drain current of J_2.

2.2.3 Modeling and Simulation

The above description of mixer operation was validated in simulation using Linear Technology's LTSPICE circuit simulation software.

Device Modeling for Simulation

We selected PN4117 JFET devices for the mixer because their high incremental resistance works well with the impedance modulation scheme we use to transmit current information through the coils. The impedance modulation scheme we use and the device selection for the mixer are discussed further in Chapter 3.

To simulate the mixer circuit, we use Linear Technology's LTSPICE software, which has an generic model for a different packaging of the same JFET made by Fairchild, the 2N4117. We modify this model with parameters measured from the JFET I-V curve shown in Figure 2-13, which was taken on a sample from our batch of transistors. We measure the pinchoff voltage V_P, the drain saturation current at $V_{GS} = 0$: I_{DSS}, the JFET transconductance parameter $\beta = I_{DSS}/V_P^2$, and λ, which is the parameter that determines output conductance. From the measured values from the curves shown in Figure 2-13, we modify the generic model as follows:

```
.model 2N4117  NJF(Beta=33.07u Betatce=-.5 Rd=1 Rs=1 Lambda=13m
   Vto=-1.2 Vtotc=-2.5m Is=5.261f Isr=51.03f N=1 Nr=2 Xti=3
   Alpha=797.9n Vk=90.45 Cgd=3.94p M=.4335 Pb=1 Fc=.5 Cgs=4.93p
   Kf=45.61E-18 Af=1 mfg=Fairchild)
.model PN4117A NJF(Beta=40u Betatce=-.5 Rd=1 Rs=1 Lambda=10m
   Vto=-1.2 Vtotc=-2.5m Is=5.261f Isr=51.03f N=1 Nr=2 Xti=3
   Alpha=797.9n Vk=90.45 Cgd=3.94p M=.4335 Pb=1 Fc=.5 Cgs=4.93p
   Kf=45.61E-18 Af=1 mfg=Fairchild)
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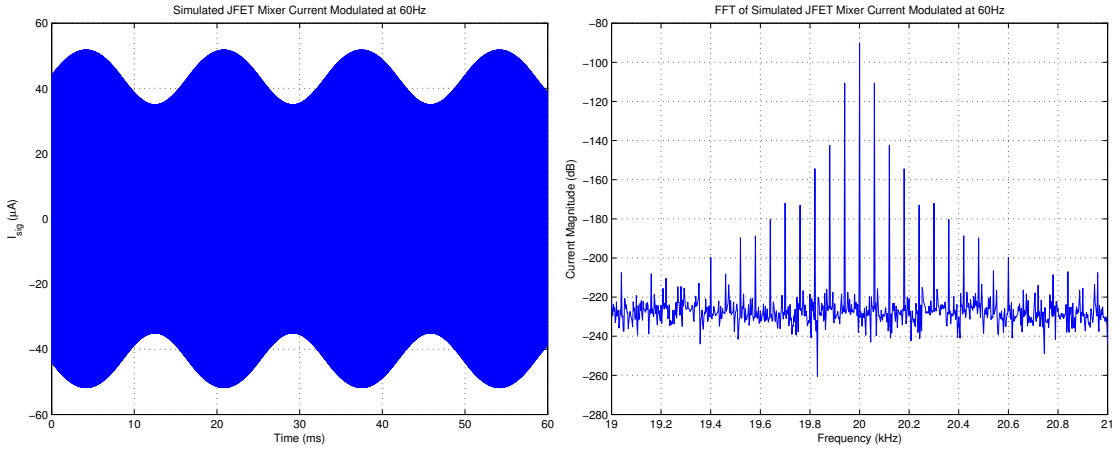


(a) Time-Domain Modulation Behavior (b) Fast Fourier Transform

Figure 2-15: LTSPICE transient simulation of the JFET mixer, demonstrating modulation behavior and distortion.

Simulation

The simulated circuit is identical to Figure 2-12, with $R = 100\text{k}\Omega$ and the custom PN4117A model described above used for JFET devices J_1 and J_2. Modulation behavior is confirmed by a 40ms transient simulation, where V_C is a 20kHz 1V peak sine wave, V_S is a 60 Hz 200mV peak sine wave. The 60 Hz amplitude modulation of the 20kHz carrier current is shown in Figure 2-15a, which plots the mixer current I_M over time. The result in Equation 2.20 as well the ohmic characteristic of the mixer at low levels of V_C and V_S is confirmed by a DC sweep, shown in Figure 2-16. This DC sweep plots the I-V characteristic of the entire mixer across the terminals of the inner coil, parameterized by various values of V_S. This plot demonstrates that for low carrier levels ($V_C \lesssim 1\text{V}$ peak) and low gate drive levels ($V_S \lesssim 250\text{mV}$ peak), the mixer behavior is approximately ohmic, and we achieve linear impedance modulation. Figure 2-15b shows a fast fourier transform (FFT) of the modulated current in Figure 2-15a that allows us to quantitatively evaluate linearity in terms of the total harmonic distortion (THD) of the original 60 Hz modulating signal. The THD is given by the ratio of the sum of the powers of the unwanted harmonics of 60 Hz to the power of

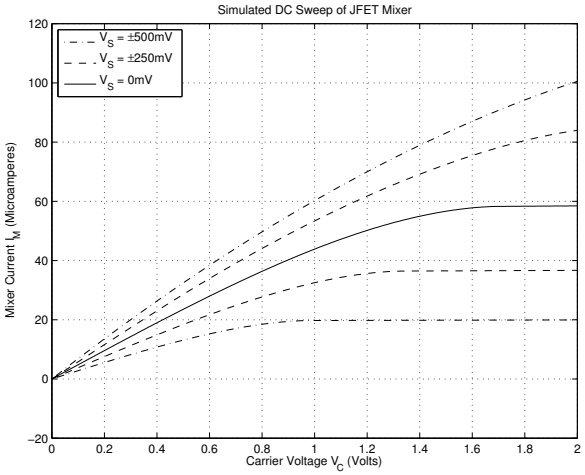


Figure 2-16: LTSPICE DC simulation of the JFET mixer.

the fundamental 60 Hz harmonic:

$$\text{THD} = \frac{\sum_{n=2}^{\infty} P_{n\cdot 60\text{Hz}}}{P_{60\text{Hz}}} \tag{2.21}$$

Which translates to voltage units, as given in the FFT, as:

$$\text{THD} = \frac{\sum_{n=2}^{\infty} V_{n\cdot 60\text{Hz}}^2}{V_{60\text{Hz}}^2} \tag{2.22}$$

Operating under the conditions shown, which represent typical maximum operating levels for our system, the simulated total harmonic distortion is 0.075%.

2.3 Pickup Amplification

The pickup amplifier is an amplification stage designed to gain to current-sense pickup voltage to a level sufficient to drive the JFET mixer. As shown in Table 2.1, the pickups we designed only produce millivolts for every ampere of current sensed, so a gain of 10 to 100 is necessary to drive the mixer, depending on the current level in the breaker. In this section we discuss two designs for the amplification stage: a passive transformer-based design and an active instrumentation amplifier-based design. Both circuits have advantages and disadvantages.

Using a transformer eliminates the need for wirelessly transmitted power or bat-

teries inside the door. The circuit is simple and small. However, it is difficult to design a transformer with turns ratios of 1:10 or more that both meets the size requirements for placement inside the breaker panel and does not inductively load the current-sense pickup at 60 Hz. Furthermore, dynamically adjusting the gain of a transformer-based amplification stage is difficult.

An instrumentation amplifier, by comparison, has high-impedance input terminals that do not load the pickup, and the gain can easily be adjusted with a single resistor. The downside of the instrumentation amplifier is its power requirement, which necesitates either a serparate power transmission coil on the door, or batteries which must be replaced by the user.

2.3.1 Passive Amplification

The highest turns-ratio, low-frequency transformers commerically available are audio transformers. Specifically, the Tamura MET-01 and Triad SP-4 audio transformers have the highest turns ratio available for their size: 14.1:1 with roughly 500mH of magnetizing inductance on the secondary. These are used for impedance matching in audio circuits, but we can insert them "backwards" into our circuit, by connecting the secondary to the current sense pickup and the primary in place of V_S in Figure 2-12, and achieve nearly a gain of 10.

Section 2.1.4 showed that by adding transformers in parallel, we can increase the net output voltage driving the JFET mixer despite attenuation from greater loading on the pickup. In particular, Figure 2-9 shows that by connecting four transformers in parallel to a pickup wound with 1500 turns of 35 AWG magnet wire, as in Figure 2-8, we can nearly double the output voltage. We can marginally improve this to *exactly* double the output voltage by instead connecting the four transformers to the pickup as two parallel pairs of series-connected transformers, and to the mixer as four series-connected transformers, as shown in Figure 2-17. The effect of this is that the load presented to the pickup is equivalent to that of a single transformer, but the output voltage is doubled. This strategy can be extended to arbitrary numbers of transformers, but beyond four, the physical space requirements start to become

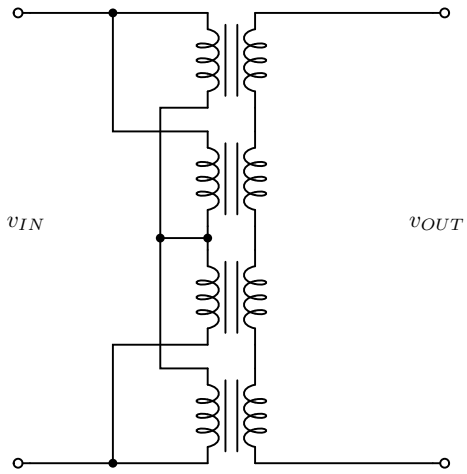


Figure 2-17: Series-parallel-series configuration of multiple transformers.

unreasonable.

2.3.2 Active Amplification

A schematic for our active amplification stage design is shown in Figure 2-18. The active device is an instrumentation amplifier powered by two batteries, center-tapped to produce a split rail. The gain of the amplifier is set by a single resistor, R_G, that can be varied in order to adjust the range of the sensor. The pickup, represented by the inductor in the schematic, is connected directly to the input terminals of the instrumentation amplifier in parallel with a frequency response compensation capacitor C_R.

In inductively coupled instrumentation amplifier inputs, the input transistors of the amplifier are usually biased by connecting a center-tap on the winding to the reference node of the amplifier, producing matched impedances between the input terminals and reference node. For our application, however, we can expect the gain of the amplifier to be low enough $G < 100$ that we can bias the inputs with large resistors without seeing any substantial DC offset or noise at the amplifier output. Resistors R_B are identical 18 kΩ 5% biasing resistors shunted from each input terminal to the reference terminal.

The instrumentation amplifier used in our experimental setup is an Analog Devices

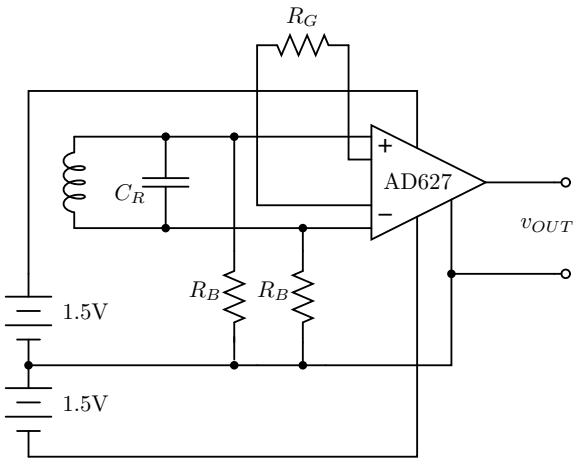


Figure 2-18: AD627-based active pickup amplification circuit. The coil symbol represents the current-sense pickup.

AD627 micropower instrumentation amplifier. The AD627 was selected for its low quiescent supply current of 60μA and split-rail design.

Physical space constraints require batteries of the small form-factor "coin-cell" variety. The most common high-capacity low-leakage coin cell, the 20mm diameter CR2032, has an average capacity of 225mAh at 3 volts for lithium maganese dioxide chemistry. Our application requires even less than 3V, but requires a split rail, so we can reduce the battery size (but not increase capacity) by moving to a 11.6mm diameter SR44 1.5V cell with 200mAh capacity using a silver-oxide chemistry. At this energy capacity, we can expect a nearly five-month lifespan at the 60 μA current draw of the AD627.

Chapter 3

Inductive Through-Door Link

This chapter reviews the transmission of information between the sensing electronics described in the previous chapter and the signal conditioning circuitry outside the circuit breaker panel, discussed in Chapter 4. The inductive through-door link serves as a near-field wireless communication channel for this information.

The link consists of two coupled LC resonators, each constructed of a coiled winding and a discrete capacitor. The windings, W_1 and W_2, are placed at the same point on the outer and inner sides of the panel door, respectively, as shown in Figure 3-1. The difficulty of this configuration is that the high permeability of the steel door limits the coupling between the two coils by diverting the magnetic flux generated by one coil through the steel and away from the adjacent coil, leading to large leakages. We reduce this effect by saturating the magnetic domains in the steel

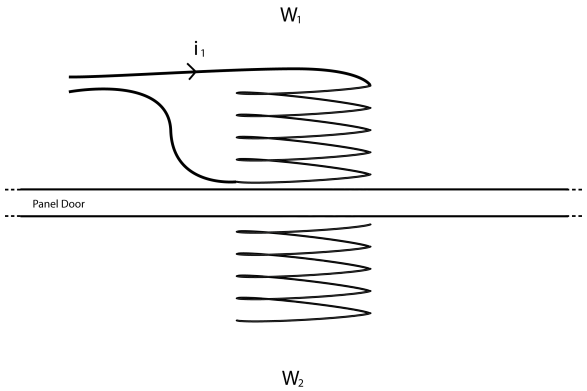


Figure 3-1: Cartoon of windings on either side of panel door.

with permanent magnets that are placed on either side of the door in the centers of the coils. Saturation reduces the relative permeability of the steel, limiting the amount of magnetic flux diverted through the door. Figure 3-2 separately depicts coupling fields between the windings and leakage fields.

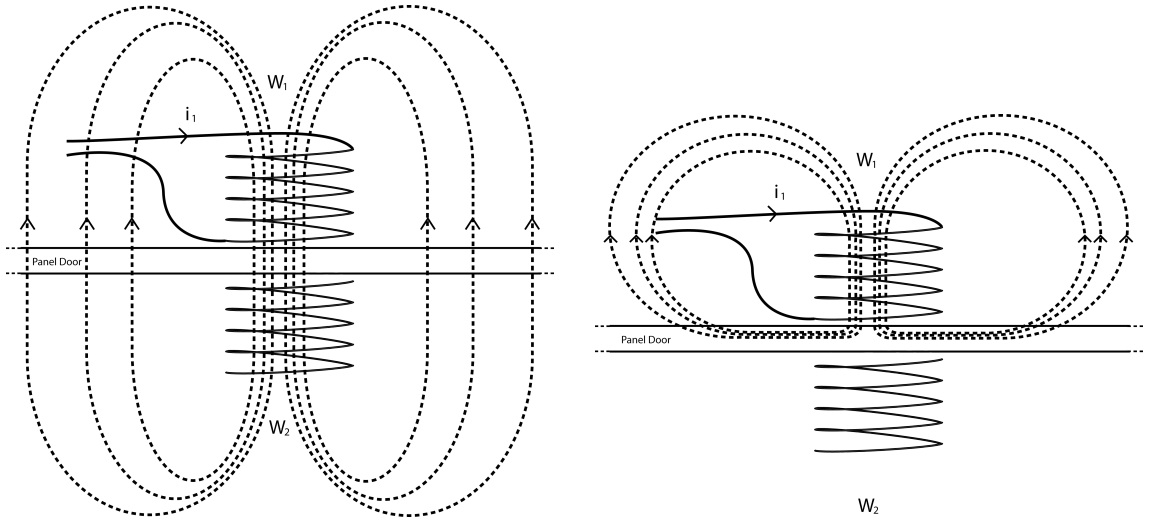
To sense changes in the impedance of the JFET mixer present at the terminals of inner coil, the outer coil is driven with a voltage source oscillating at the resonant frequency of the two LC resonators, which is selected to minimize both the relative permeability of the door and resistive losses due to eddy currents in the steel. The impedance of the JFET mixer, modulated linearly with the sensed current, is reflected across the coupled resonators, and alters the input impedance to the outer-door resonator as measured at the drive circuitry. Changes in this impedance translate to proportional changes in the outer coil current, which is measured at the front-end of the signal conditioning circuitry as the voltage across the capacitor of the outer resonator.

This chapter reviews the fundamentals of coupled resonators in Section 3.1. Section 3.2 discusses how they can be used with an impedance modulation scheme for data transmission. Section 3.3 discusses the use of permanent magnets to saturate the magnetic domains in the steel door of the circuit breaker panel in order to increase coupling between the resonators. Finally, Section 3.4 reviews experimental design of the resonator coils.

3.1 Coupled Resonators

3.1.1 Mutually Coupled Inductors

The inductive through-door link consists of two resonators made with two coils, W_1 and W_2, as shown in Figure 3-1. When the outer coil W_1 is driven with a current i_1, a magnetic field is generated in the closed contours around the current-carrying windings, according to Ampere's law:



(a) Coupling (b) Leakage

Figure 3-2: Drawings of magnetic coupling fields and leakage fields between windings W_1 and W_2. In reality, both fields exist simultaneously.

$$\oint_{C_{H1}} \vec{H_1} \cdot d\vec{s} = i_1 \tag{3.1}$$

where $\vec{H_1}$ is the magnetic field intensity along the closed contour C_{H1} around coil W_1. As shown in Figure 3-2a, some of the magnetic flux from this field will pass through the inner coil, W_2:

$$\Phi_{21} = \int_{S_{W2}} \mu \vec{H_1} \cdot d\vec{a}_2 \tag{3.2}$$

where $\mu\vec{H_1}$ is the flux density of the magnetic field, which is integrated over the surface enclosed by the windings of the inner coil. Thus Φ_{21}, the flux through W_2 due to the field generated by the current in W_1, is proportional to the current i_1 by a constant of proportionality M_{21} that depends on the coil geometries.

$$\Phi_{21} = M_{21} i_1 \tag{3.3}$$

If current i_1 is time-changing, the proportional time-changing flux Φ_{21} will induce a voltage on W_2 according to Faraday's Law:

$$v_{21} = \oint_{C_{E2}} \vec{E_2} \cdot d\vec{s} = -M_{21} \frac{d}{dt} \Phi_{21} \tag{3.4}$$

We call M_{21} the *mutual inductance* from W_1 to W_2 because it is proportional to the voltage induced on W_2 due to the time-changing magnetic flux from W_1.

Similarly, the magnetic flux generated by the current in W_1 induces a voltage on W_1 itself. While only some of this flux couples to W_2, all of it must pass through W_1, since the net flux through any closed surface around the coil is necessarily zero according to Gauss's law:

$$\oint_{S_{W1}} \mu \vec{H_1} \cdot d\vec{a_1} = 0 \tag{3.5}$$

Re-applying equations (3.1)-(3.4), we can see that the voltage that is "self-induced" on W_1 will also be proportional to the time derivative of I_1, this time by another (larger) constant called the *self-inductance* of the coil, L_1:

$$v_{11} = -L_1 \frac{d}{dt} \Phi_1 \tag{3.6}$$

The self-inductance of each coil is dependent on its own particular geometry. However, it can be shown that the mutual inductance from W_1 to W_2 is equal to the mutual inductance from W_2 to W_1 by using a reciprocity theorem derived from Ampere's law and Stokes' theorem [29]:

$$M_{21} = M_{12} = M \tag{3.7}$$

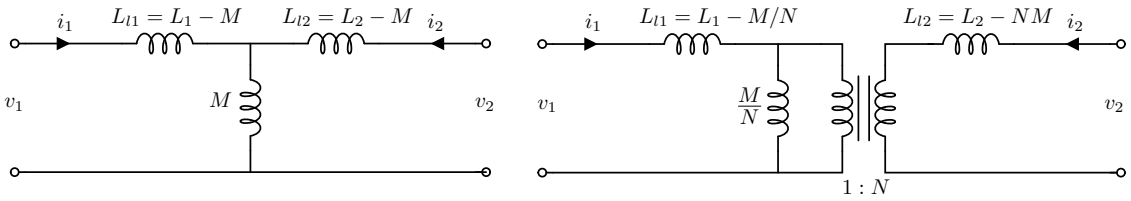
Given these self- and mutual inductance parameters, we can write a system of equations to represent the inductive coupling between the two coils:

$$v_1 = L_1 i_1 + M i_2 \tag{3.8}$$

$$v_2 = L_2 i_2 + M i_1 \tag{3.9}$$

Leakages

As shown in Figure 3-2b, a fraction of the flux generated by the current in W_1 is shunted through the steel door and does not couple to W_2. This is known as the *leakage* flux, $\Phi_{l1} = \Phi_1 - \Phi_{21}$. We can use this concept of leakage to represent the behavior of the coil from a circuit perspective, splitting the total inductance L of a



(a) Basic Model (b) Model with Ideal Transformer

Figure 3-3: Leakage circuit models for coupled inductors.

coil into into leakage and mutual components, L_l and M:

$$L = L_l + M \tag{3.10}$$

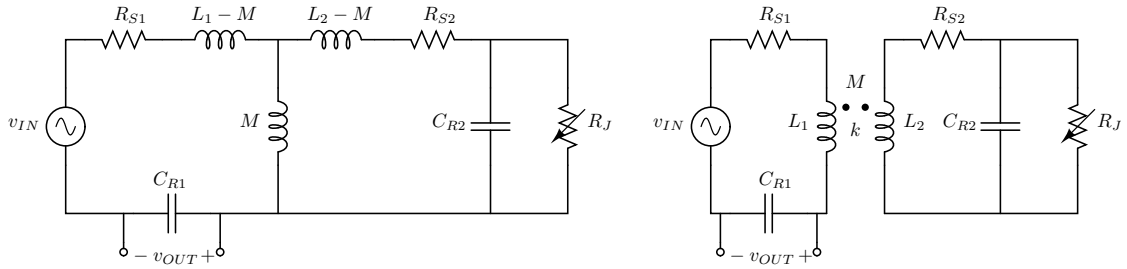
where L_l is the "leakage inductance". By substituting this expression into the system of equations (3.8) and (3.9), we can develop a circuit model for the coupled coils, shown in Figure 3-3a. When necessary, this circuit model can be extended to a transformer model with a turns ratio $1 : N$ by dividing or multiplying the mutual inductance by N depending if it is referenced to the primary or secondary side of the transformer, respectively, as shown in Figure 3-3b [16].

The Coupling Coefficient

The leakage inductances in the schematics in Figure 3-3 help describe the coupling between the coils, but the additional circuit elements also make the system more complicated algebraicly. To simplify the algebra, the relationship between the mutual flux and the leakage flux can be summarized with a single *coupling coefficient* k, given by

$$k = \frac{M}{\sqrt{L_1 L_2}} = \sqrt{\frac{L_{l1} L_{l2}}{L_1 L_2} - \frac{L_{l1}}{L_1} - \frac{L_{l2}}{L_2}} \tag{3.11}$$

where k is always a value between 0 and 1, inclusive. A k of 1 represents perfect coupling, and a k of 0 represents no coupling. This constant greatly simplifies the analysis of the input impedance to the coils in Section 3.2. The coupling coefficient is advantageous for modeling our system in particular, because coupling between the through-door coils is very low, and leakage inductances are difficult to measure.



(a) Leakage Model (b) Coupled Inductor Model

Figure 3-4: Equivalent circuit models for coupled resonators.

3.1.2 Coupled Resonator Modelling

Schematics of the coupled resonators that make up the through-door link are shown in Figure 3-4 using equivalent leakage and coupling coefficient circuit models. L_1 and L_2 are the inductances of the windings of the outer and inner coils respectively. The coils have a mutual inductance M with a coupling coefficient k, and leakage inductances L_{l1} and L_{l2}. Resistances R_{S1} and R_{S2} represent the parasitic series resistances of the windings. Capacitances C_{R1} and C_{R2} are the discrete resonant capacitors attached to the windings. R_J is the load presented by the JFET modulator on the inner coil. In this model we ignore any losses from hysteresis or eddy currents in the steel door, as well as effective series resistances (ESR) of capacitors C_1 and C_2, for simplicity.

After combining resistive terms, the outer circuit reduces to a simple RLC resonator, but the inner circuit is more complex because of the parallel combination of C_{R2} with R_J that is loading the coil. It can be shown, however, that any parallel combination of impedances can transformed to an equivalent series circuit or vice-versa, as follows [19]:

$$R_P = R_S(Q^2 + 1) \tag{3.12}$$

$$X_P = X_S \left(\frac{Q^2 + 1}{Q^2} \right) \tag{3.13}$$

where R_P, R_S, and X_P, X_S represent parallel and series resistances and reactances,

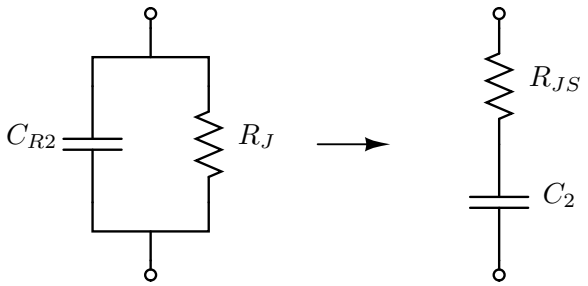


Figure 3-5: Parallel-to-series transformation of resonant capacitor and JFET modulator load on the inner resonant coil.

respectively. The quality factor Q of the circuit is given by

$$Q = \frac{X_S}{R_S} = \frac{R_P}{X_P} \tag{3.14}$$

and is constant for both the parallel and series configurations, as they are equivalent. However, since the transformation is dependent on Q, which itself depends on operating frequency ω, this equivalence can only be taken to hold over a very narrow range of frequencies. Fortunately, we can expect to always be operating the resonators within a small bandwidth about a single carrier frequency ω_o that is equal to the resonant frequency of both resonators, so the parallel-series equivalence is a reasonable approximation here.

Using these transformations, we can simplify the load connected to the inner coil to a series RC circuit, as shown in Figure 3-5:

$$R_{JS} = \frac{R_{C2}}{Q_C^2 + 1} \tag{3.15}$$

$$C_2 = C_{R2}\left(\frac{Q_C^2}{Q_C^2 + 1}\right), \tag{3.16}$$

where Q_C is the quality factor of the discrete capacitor C_{R2} in parallel with R_J.

$$Q_C = \frac{R_J}{\omega C_{R2}}. \tag{3.17}$$

At this point all remaining series resistances can be combined to give us a final circuit consisting of two coupled simple RLC resonators, as shown in Figure 3-6,

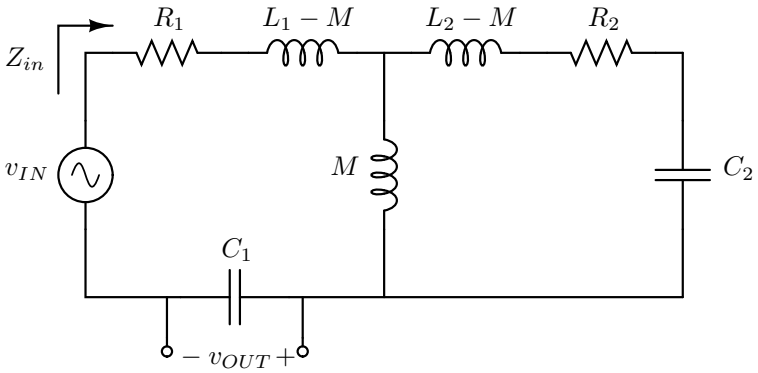


Figure 3-6: Simplified model of coupled resonators.

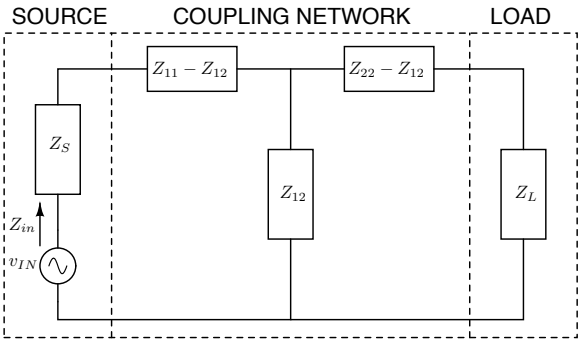


Figure 3-7: Generic model of coupled resonators [22].

where

$$R_1 = R_{S1}, \tag{3.18}$$

$$R_2 = R_{S2} + \frac{R_J}{(\frac{R_J}{\omega C_{R2}})^2 + 1}, \tag{3.19}$$

$$C_1 = C_{R1} \tag{3.20}$$

$$C_2 = C_{R2}\left(1 + \left(\frac{\omega C_{R2}}{R_J}\right)^2\right). \tag{3.21}$$

We can generalize the circuit in Figure 3-6 to the generic model for coupled resonators presented in [22], shown here in Figure 3-7. This model generalizes the circuit components in our simplified model to input impedances (Z_{11} and Z_{22}), a *transfer*

impedance Z_{12}, a load impedance Z_L, and a source impedance Z_S. For our model,

$$Z_{11} = j\omega L_1 + R_1 \tag{3.22}$$

$$Z_{22} = j\omega L_2 + R_2 \tag{3.23}$$

$$Z_{12} = j\omega M, \tag{3.24}$$

and our source and load impedances are

$$Z_S = 1/j\omega C_1 \tag{3.25}$$

$$Z_L = 1/j\omega C_2. \tag{3.26}$$

As with our simplified circuit model, we do not account for losses from radiation, eddy currents in the steel door, or capacitance to the steel door, for simplicity. However, such effects are compatible with this general model and can be readily included.

3.2 Impedance Modulation

Impedance modulation is commonly performed by driving a source resonator with an oscillating voltage, then switching a load impedance between discrete states at a coupled transmitting resonator. The receiver senses the change of load impedance as a change in the input impedance as seen from the drive circuitry at the source resonator.

Here impedance modulation is accomplished with a JFET modulator that changes its incremental impedance continuously with the sensed current signal from the circuit breaker, as described in Chapter 2, instead of switching between discrete states.

3.2.1 Theoretical Analysis

To begin the analysis of impedance modulation in our circuit, we can use the generalized model in Figure 3-7 to derive the expression for the driving impedance Z_{in} at

the outer coil of a pair of coupled resonators.

$$\begin{aligned} Z_{in} &= Z_S + Z_{11} - Z_{12} + (Z_{12} \parallel (Z_{22} - Z_{12} + Z_L)) \\ &= Z_S + Z_{11} - Z_{12} + \frac{Z_{12}(Z_{22} - Z_{12} + Z_L)}{Z_{22} + Z_L} \\ &= Z_S + Z_{11} - \frac{Z_{12}^2}{Z_{22} + Z_L} \end{aligned} \tag{3.27}$$

Arriving at this expression, we can decompose the impedance terms into lumped circuit element values from the definitions in equations (3.18)-(3.21):

$$Z_{in} = \frac{1}{j\omega C_1} + R_1 + j\omega L_1 + \frac{\omega^2 M^2}{j\omega L_2 + R_2 + \frac{1}{j\omega C_2}} \tag{3.28}$$

This expression can be greatly simplified if we assume the system is driven near the resonant frequency of both resonators. That is, if

$$\omega = \omega_o = \frac{1}{\sqrt{L_1 C_1}} = \frac{1}{\sqrt{L_2 C_2}}, \tag{3.29}$$

then the reactive components L_1, C_1, L_2, and C_2 cancel, and we are left with

$$Z_{in} = R_1 + \frac{\omega_o^2 M^2}{R_2}. \tag{3.30}$$

Directly expressing ω_o in terms of circuit elements, this becomes

$$\begin{aligned} Z_{in} &= R_1 + \frac{M^2}{R_2} \frac{1}{\sqrt{L_1 C_1 L_2 C_2}} \\ &= R_1 + \frac{k^2}{R_2} \sqrt{\frac{L_1 L_2}{C_1 C_2}}, \end{aligned}$$

recalling that $k = M/\sqrt{L_1 L_2}$. Finally, we can express Z_{in} in terms of the quality factors of the resonators, $Q_1 = \sqrt{L_1/C_1}/R_1$ and $Q_2 = \sqrt{L_2/C_2}/R_2$, as in [22]:

$$\boxed{Z_{in} = R_1(1 + k^2 Q_1 Q_2)} \tag{3.31}$$

As the JFET mixer modulates its impedance, it will alter the quality factor Q_2 of the inner resonator, since the incremental impedance of the mixer is part of the composite term R_2. Expressing Z_{in} this way, we can see that its modulation depth - the amount that Z_{in} is modulated around its nominal level - is proportional to the quality factors of the resonators and the strength of the coupling between them. This is important because the modulation of Z_{in} is exactly what must be maximized. It is the signal that carries the information about the current sensed at the breaker face, and it is precisely what the voltage measurement across C_1 is designed to detect. Equation 3.31 implies that if we can increase the quality factors and coupling of our resonators, we will increase the signal level at the front-end of our sense circuitry. This is a critical observation.

We can go a step further and directly express the magnitude of the transfer function from the driving point of the outer coil to our sense circuitry input across the resonant capacitor C_1. We start by taking the input current by dividing v_{IN} by our expression for Z_{in}, and then we multiply by the sense impedance Z_S to get the voltage across it:

$$\begin{aligned} \frac{v_{OUT}}{v_{IN}} &= \frac{1}{j\omega_o C_1}\frac{1}{Z_{in}} \\ &= \frac{1}{j\omega_o C_1 R_1(1+k^2Q_1Q_2)} \end{aligned} \tag{3.32}$$

taking the magnitude,

$$\left|\frac{v_{OUT}}{v_{IN}}\right| = \frac{1}{\omega_o C_1 R_1 + k^2\omega_o\sqrt{L_1C_1}\sqrt{\frac{L_2}{C_2}}\frac{1}{R_2}} \tag{3.33}$$

and simplifying,

$$\left|\frac{v_{OUT}}{v_{IN}}\right| = \frac{1}{\omega_o C_1 R_1 + k^2 \frac{1}{R_2}\sqrt{\frac{L_2}{C_2}}}$$
$$\left|\frac{v_{OUT}}{v_{IN}}\right| = \frac{1}{\frac{1}{Q_1} + k^2 Q_2} \tag{3.34}$$

Like Equation (3.31), the transfer function implies that increased resonator Q and coupling will increase the impact that the changing impedance of the JFET modulator will have on v_{OUT}. However, we can see the relationship more clearly by deriving our quantity of interest directly: the change in v_{OUT} with respect to changes in the resistive impedance on the inner coil:

$$\begin{aligned}\frac{d\left|\frac{v_{OUT}}{v_{IN}}\right|}{dR_2} &= k^2\sqrt{\frac{L_2}{C_2}}\frac{1}{R_2^2}\frac{1}{\left(\omega_o C_1 R_1 + k^2\frac{1}{R_2}\sqrt{\frac{L_2}{C_2}}\right)^2} \\ &= \frac{k^2}{\sqrt{\frac{C_2}{L_2}}\left(k^4\frac{L_2}{C_2} + 2k^2\sqrt{\frac{L_2}{C_2}}\omega_o C_1 R_1 R_2 + \omega_o^2 C_1^2 R_1^2 R_2^2\right)}\end{aligned}$$

simplifying,

$$= \frac{k^2}{R_2\left(k^4 Q_2 + \frac{2k^2}{Q_1} + \frac{1}{Q_1^2 Q_2}\right)}. \tag{3.35}$$

This expression is effectively the impedance modulation "gain". In our design, we can use it to maximize the change in $|v_{IN}/v_{OUT}|$ over a range of R_2 corresponding to a linear range of the JFET mixer impedance, R_J. To put that more concretely, the expression to maximize is:

$$\frac{d\left|\frac{v_{OUT}}{v_{IN}}\right|}{dR_2}\Delta R_2$$

where ΔR_2 is our modulation range about a nominal resistance R_2.

This expression is more complex than (3.31) and (3.34), showing the subtler dependence of the modulation depth on R_2 and N. However, if we assume that $k \ll 1$, as is the case in our system where the coils are separated by a steel panel, then the

denominator is dominated by $1/(Q_1^2 Q_2)$ and the expression simplifies to

$$\frac{d\left|\frac{v_{OUT}}{v_{IN}}\right|}{dR_2} \approx R_2 k^2 Q_1^2 Q_2. \tag{3.36}$$

Applying this approximation to Equation (3.2.1), we can get a figure of merit for the design of our resonators:

$$\boxed{\frac{d\left|\frac{v_{OUT}}{v_{IN}}\right|}{dR_2}\Delta R_2 \approx \frac{\Delta R_2}{R_2} k^2 Q_1^2 Q_2} \tag{3.37}$$

This is very satisfying, since like Equation 3.31, it suggests that the most important quantities to maximize are the coupling and quality factors of the resonators.

Accounting for Non-Unity Turns Ratio

Up until this point we have assumed that the turns ratio N between the coils is unity, for convenience. An arbitrary turns ratio can be accounted for by referring circuit elements to the primary (outer) side of ideal transformer in the model shown in Figure 3-3b. However, the equations for the important quantities in this chapter (Z_{in}, $|v_{OUT}/v_{IN}|$, and out figure of merit) are notable because they do not depend on N. Resistance R_1 in Equation (3.31) is not affected because it does not need to be reflected. Factors of N^2 resulting from reflecting resistance R_2 in Equation (3.37) cancel. Composite terms k and Q are also independent of N:

$$k = \frac{M/N}{\sqrt{L_1 L_2/N^2}} = \frac{M}{\sqrt{L_1 L_2}} \tag{3.38}$$

$$Q_2 = \frac{1}{R_2/N}\sqrt{\frac{L_2}{N^2 C_2}} = \frac{1}{R}\sqrt{\frac{L_2}{C_2}}. \tag{3.39}$$

In fact, only Equation (3.35) depends on N, although the dependence is inconsequential for our results. To generalize it to account for an arbitrary turns ratio, it can be multiplied by N^2.

3.2.2 Design Implications

The main design choices for the resonators of the through-door link consist of selecting

- R_J, the incremental impedance of the JFET modulator,
- N, the outer to inner turns ratio,
- The absolute turn counts and wire gauge, which govern L_1, L_2, C_1, C_2, and their associated parasitics.

We want to choose these parameters in such a way that the impedance modulation depth is maximized; specifically, that we maximize the figure of merit in (3.37).

JFET Device Selection

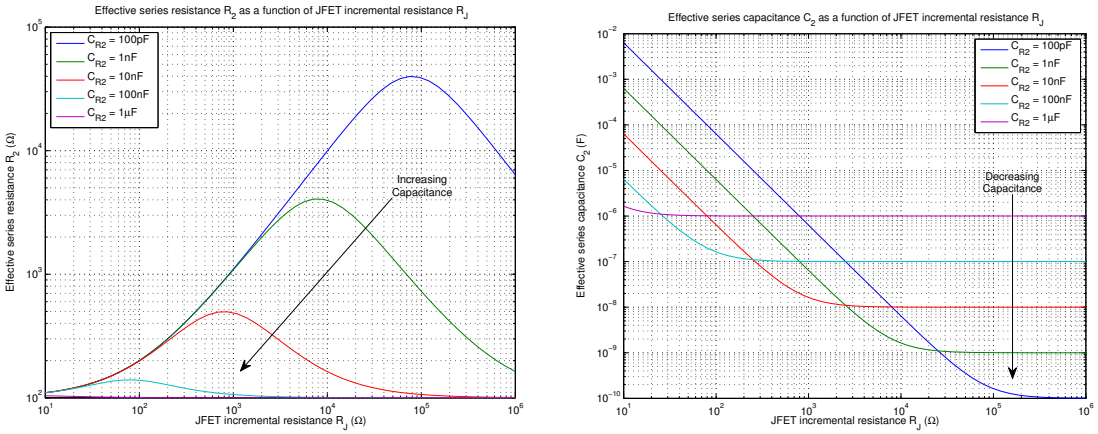
Resistances R_2 and ΔR_2 are influenced by our choice of JFET devices in the modulator. R_2 is a composite term consisting of the of inductor parasitics R_{S2} and the parallel-to-series transformed incremental impedance of the JFET modulator circuit, R_{JS}. We recall from Equations (3.19) and (3.21) that this transformation is

$$\begin{aligned} R_2 &= R_{S2} + R_{JS} = R_{S2} + \frac{R_J}{Q_{C2}^2 + 1} \\ C_2 &= C_{R2}(1 + Q_{C2}^2), \end{aligned}$$

where Q_C is the quality factor of the parallel combination of the resonant capacitor C_{R2} and JFET incremental resistance R_J:

$$Q_{C2} = \frac{R_J}{\omega C_{R2}}.$$

Ideally, we would like R_2 to be dominated by R_{JS}, the series equivalent of the modulator resistance R_J, since R_J is the modulated impedance we are trying to sense at the primary. Examining the expressions for R_2 and C_2, we can see that when R_J is large, the quality factor Q_{C2} is large ($Q_{C2} \gg 1$). As a result, $C_2 \approx C_{R2}$, and $R_{JS} \approx R_J/Q_{C2}^2$. This means that for very large R_J, its series equivalent R_{JS} will be



(a) R_2 as a function of R_J (b) C_2 as a function of R_J

Figure 3-8: Plots of R_2 and C_2 as a function of R_J. R_{S2} is taken to be $100\,\Omega$.

small, so that inductor parasitics dominate R_2. On the other hand, for very small R_J, where $Q_{C2} \lesssim 1$, capacitance C_2 will vary significantly with R_J, invalidating our earlier approximation that $\omega_o = (L_2 C_2)^{-\frac{1}{2}}$. Therefore, the ideal JFET device would have an incremental resistance that is large so that $Q_{C2} > 1$ but small enough that R_{JS} is comparable to or greater than R_{L2}.

Figure 3-8 shows plots of R_2 and C_2 as functions of R_J, parameterized by C_{R2}. For both plots, R_{S2} was taken to be $100\,\Omega$. The plots demonstrate the JFET selection criteria for specific component values. Plot 3-8a shows how R_2 begins to become dominated by R_J increases. Plot 3-8b shows how C_2 is not constant for values of R_J below which $Q_{C2} \lesssim 1$. To maximize $\Delta R_2/R_2$, JFET devices should be chosen so that R_2 nominally lies on the downward sloping edge of the curve corresponding to the resonant capacitor used. MATLAB® code for generating these plots is given in Appendix E.2.4.

Turn Counts, and Wire Gauge

Equations (3.31) and (3.34) imply that our total modulation depth depends heavily on the quality factors of the through-door link resonators. For this analysis, we assume that the resistance of the resonators is dominated by inductor parasitics and not capacitor ESR. Therefore, we define the resonator quality factor as $Q_n = \omega L_n / R_n$, where L_n and R_n are the inductance and winding resistance of coil W_n. These coil

parameters are given by:

$$L_n = A_l N_n^2 \tag{3.40}$$

$$R_n = \frac{l}{\sigma A_c} \tag{3.41}$$

Where l is wire length, A_c wire cross-sectional area, σ is the conductance of the wire material, and A_l is an constant dependent on the coil geometry. N_n refers to the turn count for the particular winding W_n, *not* the absolute turns ratio N. Skin effect is ignored, as it only applies for large wire diameter at the carrier frequencies used in our system, which are discussed in Section 3.3.2.

Assume that winding circumference of the coils is roughly constant, so that $l \propto N_n$. For any given gauge of wire (A_C constant), and the inductance L_n goes as the turns squared, while R_n only goes linearly with turns, so that

$$\boxed{Q_n \propto N_n}.$$

This indicates that for any given wire gauge, we should use the maximum number of turns possible within the physical space constraints in order to maximize Q_n. If we take this fact as given - that we wind the maximum number of turns possible for a given gauge - then as we allow the cross-sectional area of the wire to vary, the number of turns we can fit is inversely proportional to the cross-sectional area of the wire,

$$N_n \propto A_C^{-1}$$

and under our assumption that $l \propto N_n$,

$$l \propto A_C^{-1}$$

therefore,

$$R_n \propto A_C^2$$

$$L_n \propto A_C^{-2}$$

Since $Q_n = \omega L_n / R_n$,

$$\boxed{Q_n \not\propto A_C}.$$

The end result of this is that to maximize Q_n, the turn count should be maximized over the physical space available for a given wire gauge, but the absolute wire gauge itself is for the most part inconsequential, and may be reserved as a variable for controlling the turns ratio. That said, this only applies within our approximation that capacitor ESR and skin effect are negligible, so it does not apply to coils with very large wire diameter or low turn counts.

Turns Ratio

The turns ratio N was shown to be of no consequence to the design equations derived in Section 3.2.1. It may be used as a variable to control the voltage with which the JFET modulator circuit is driven.

3.3 Penetration of the Steel Door

As discussed in the previous section, the modulation depth of the driving point impedance of the outer coil in the through-door link is proportional to the square of the coupling coefficient between the coils. Any incremental improvement in the coupling means better performance from our system. In traditional ferrite-core transformers, coupling coefficients of $k > 0.9$ are not uncommon. However, because high-permeability steel separates the coils, coupling is very poor, with k well below 0.1. We address this issue in two ways: first, by saturating the magnetic domains of the steel using high-grade permanent magnets, thereby reducing its permeability; second, by selecting a carrier frequency at which the permeability of the steel is reduced.

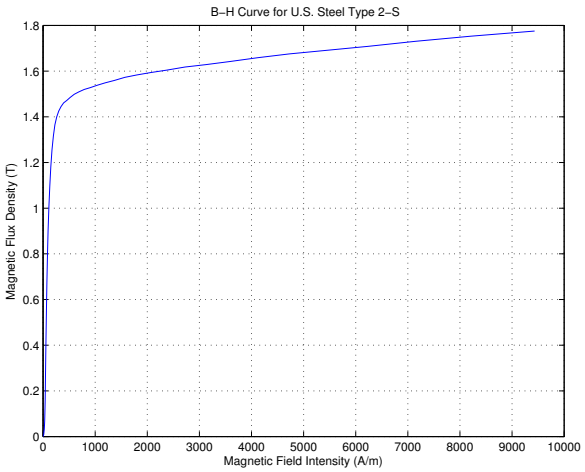


Figure 3-9: B-H Curve for U.S. Steel Type 2-S.

3.3.1 Magnetic Saturation of The Door

Saturation of steel occurs when an increased magnetic field intensity H cannot magnetize the material further. As the magnetic field intensity increases past this point, the relative permeability of the material μ drops far below its initial level μ_i, approaching the permeability of free space μ_o, so that the magnetic flux density $B = \mu H$ is nearly constant. A BH curve for the sort of steel typically used in circuit breaker panels is plotted in Figure 3-9, and shows that the steel begins to saturate around a magnetic flux density of 1.5 Tesla and a magnetic field intensity of 100 A/m. In our design, we want to configure permanent magnets on the door panel in such a way that the magnetic field in the area of the door between the coils exceeds this point on the figure.

Permanent Magnet Configuration

Previous work on this sensor has presented experiments in which permanent magnets were positioned as shown in Figure 3-10, where block magnets with a checkered pole pattern are placed at the center of the windings of each resonator on either side of the door [6–8]. The checkered pattern is intended to produce tight, short flux loops through the steel at the edges between adjacent magnets. In this previous work, the magnets are arranged so that opposite poles on either side of the door face one

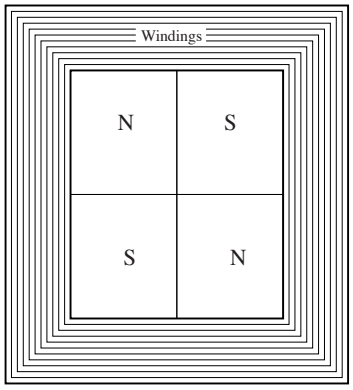
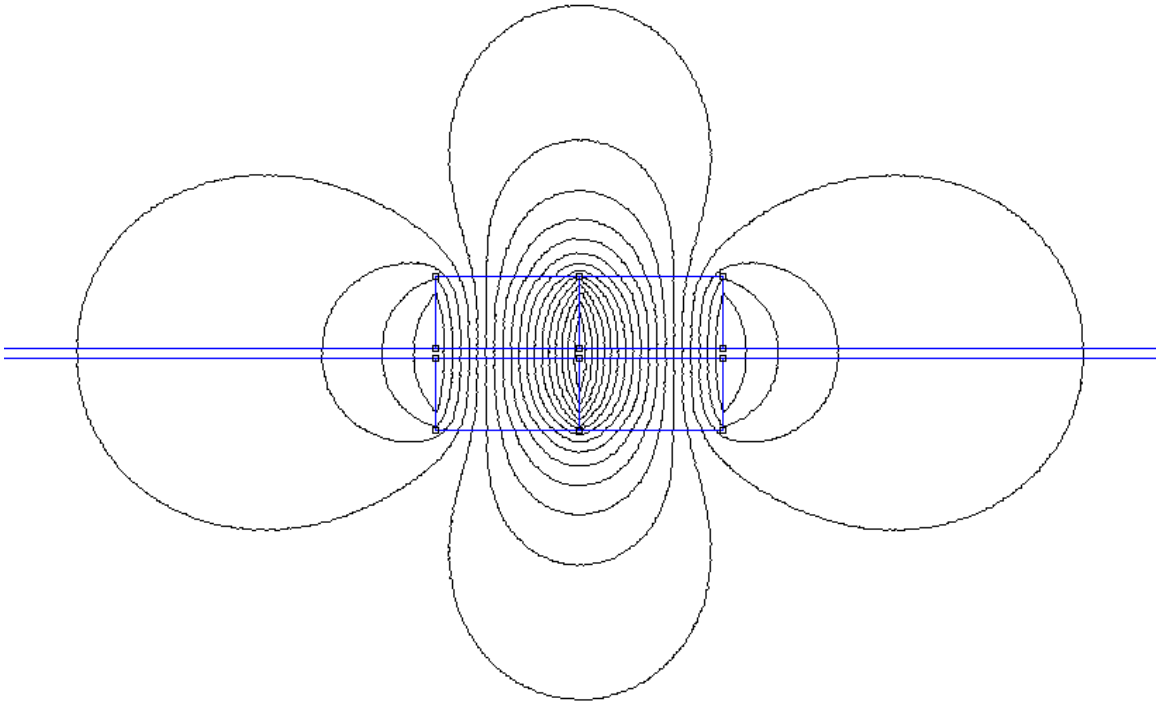


Figure 3-10: Checkered-pole alignment of permanent magnet in winding core.

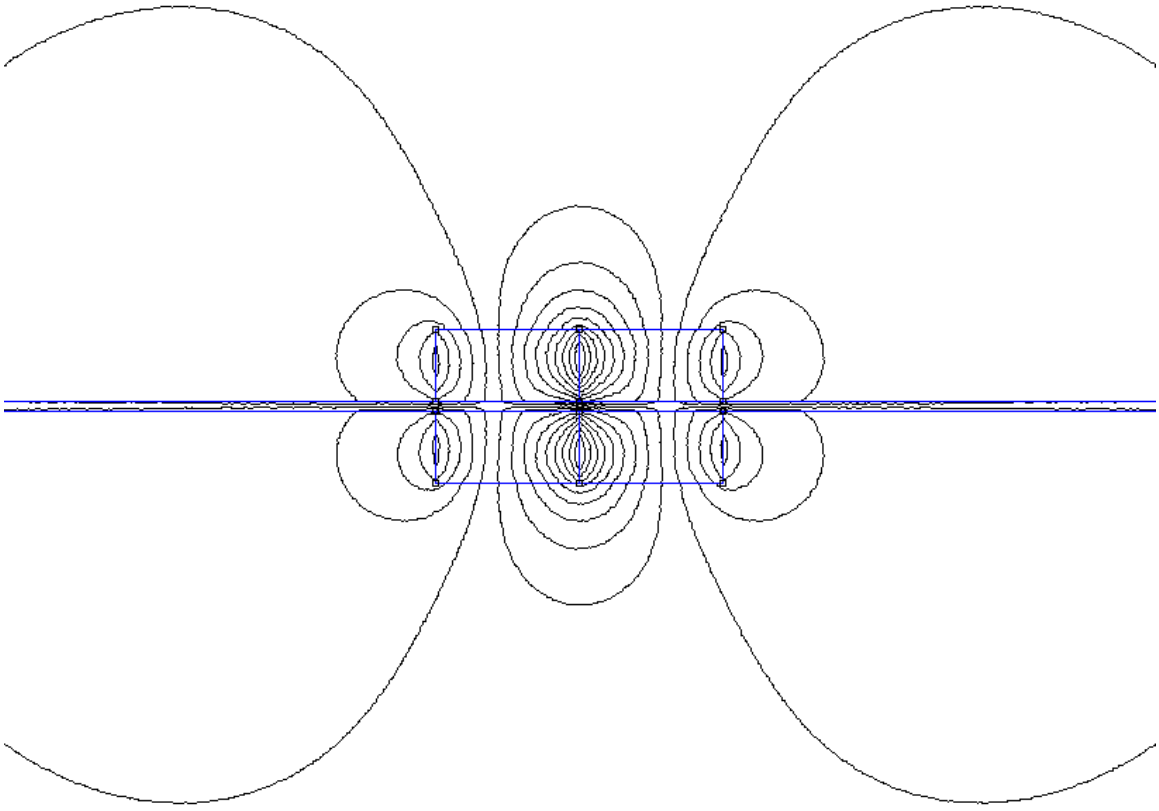
another. We find that we can dramatically increase the level of flux density in the steel if one set of magnets is rotated by ninety degrees so that instead of opposite poles facing one another through the door, like poles face each other. Since the fields from the like poles oppose one another, flux paths are forced to wrap through the steel laterally instead of passing directly through to the other side of the panel. Since the lengths of these flux paths are much smaller than those that completely pass through the door, the magnetic field intensity is increased.

This effect is demonstrated in a set of Finite Element Method Magnetics (FEMM) simulations, shown in Figures 3-11 and 3-12. The simulated problem consists of a set of four 52 MGOe Neodymium block magnets, magnetized through a 1/4" thickness, measuring 1/2" in length. Two magnets are placed with their polarization directions in antiparallel on each side of a 0.035"-thick plate of U.S. Steel Type 2-S. The steel extends out to the end of a simulation boundary set by a 4″x4″ box. All other space in the simulation is modeled as air. The mesh size for the simulation is set to 0.01 inches. The dimensions of the magnetic elements in this simulation are designed to reflect those of our experimental setup as accurately as possible, while the simulation boundary is set to conservatively encompass our area of interest surrounding the magnets.

Simulation results are given for both attracting and opposing pole configurations. Figure 3-11 shows the magnetic field lines, while Figure 3-12 shows the magnetic flux density gradients. The simulation demonstrates that in the configuration where

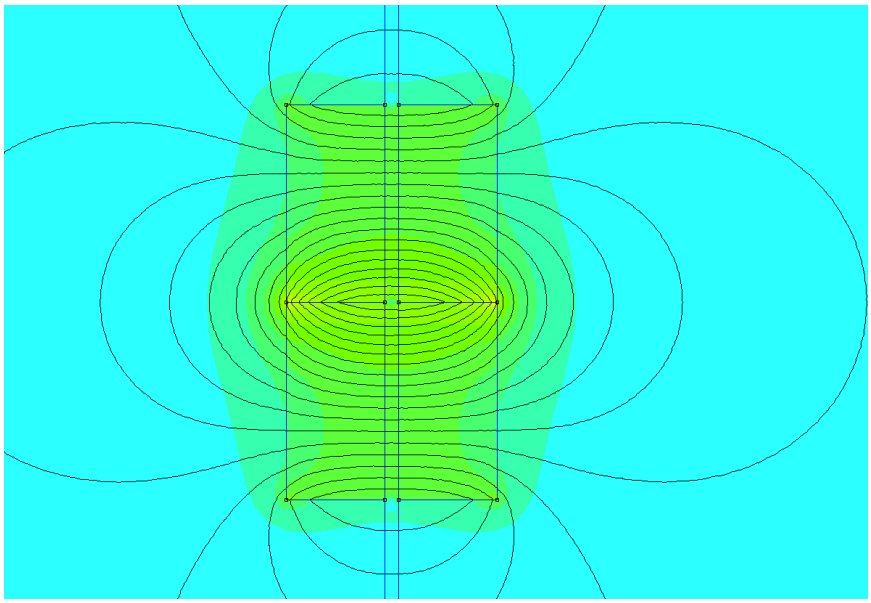


(a) Poles Attracting

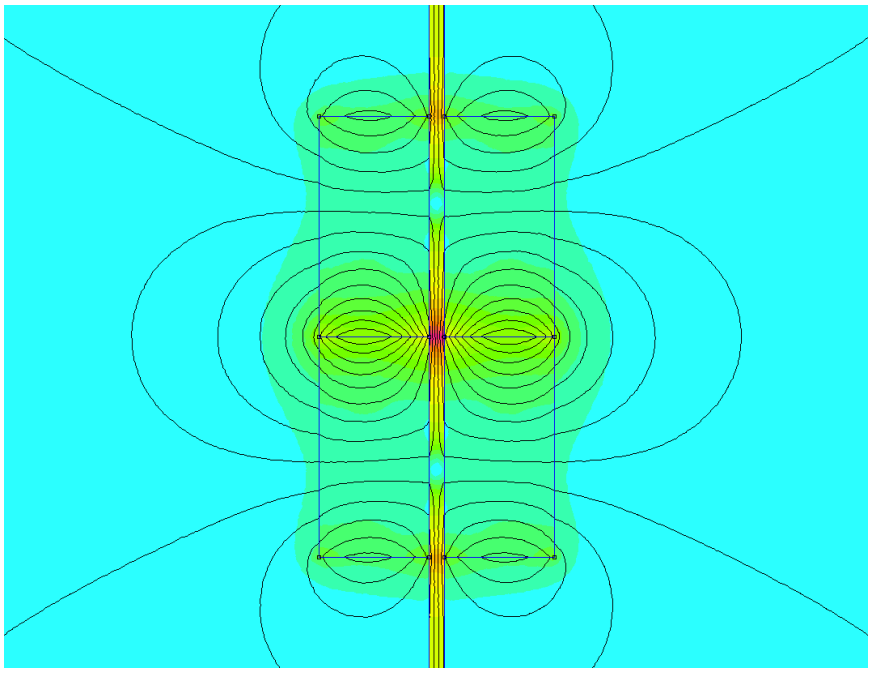


(b) Poles Opposing

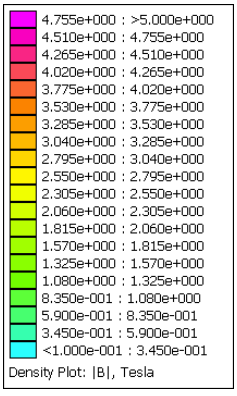
Figure 3-11: FEMM simulation of magnetic field lines of permanent magnets on steel.



(a) Poles Attracting

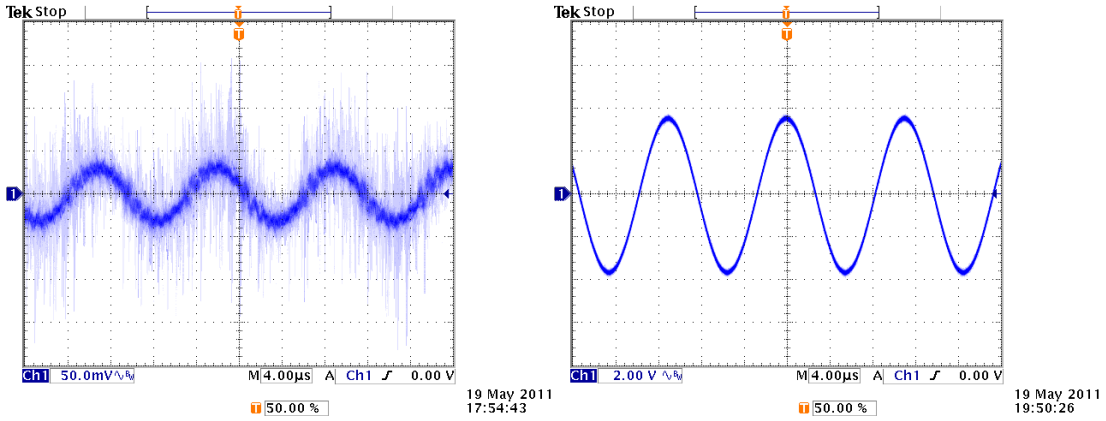


(b) Poles Opposing



(c) Color Legend

Figure 3-12: FEMM simulation of magnetic flux densities of permanent magnets on steel.



(a) Poles Attracting (b) Poles Opposing

Figure 3-13: Open-circuit voltage on inner test coil during experiment testing the effectiveness of attracting- and opposing-pole permanent magnet configurations.

Coil	L	R	Q
Outer	27.8 μH	6.8 Ω	0.57
Inner	42.8 mH	8.2 kΩ	2.58

Table 3.1: Properties of coils used in magnet pole-configuration experiments, plotted in Figure 3-13. Measurements were taken at 100kHz.

magnetic poles oppose one another through the steel, the flux paths are indeed shorter, and flux densities in the steel exceed well past 1.5 T over almost the entire area below and around the magnets. In the original configuration, on the other hand, flux densities in the steel approach but usually do not exceed 1.5 T, and flux paths loop through the other side of the door before returning through it again to the opposite pole of the generator magnet.

To experimentally confirm of this effect, two test coils with parameters given in Table 3.1 were fitted with 26 MGOe grade Samarium-Cobalt block magnets of a size matching our simulation, in the configuration shown in Figure 3-10. The outer coil was driven with a 90 kHz, 10 V peak-to-peak square wave, while the open-circuit voltage of the inner coil was measured with an oscilloscope. The steel door separating the coils was earthed to prevent capacitive coupling between them. The measurements, shown in Figure 3-13, demonstrate an approximate one hundred times improvement in the voltage transfer between the two coils from a "straight" alignment of the magnets to

Coil		Air Core	26 MGOe SmCo	35 MGOe NdFeB Unplated	42 MGOe NdFeB Nickel-Plated
15 Turns 20 AWG	L	25.91 μH	25.66 μH	25.76 μH	25.53 μH
	R	201.1 mΩ	250.0 mΩ	240.6 mΩ	273.2 mΩ
	Q	16.19	12.90	13.45	11.74
1000 Turns 35 AWG	L	97.93 mH	97.09 mH	97.54 mH	96.60 mH
	R	267 Ω	449 Ω	413 Ω	540 Ω
	Q	46.1	27.2	29.7	22.5

Table 3.2: Measured parameters of test coils used in magnet plating experiment.

a "twisted" alignment where like poles face each other through the steel.

Later experiments demonstrated that for best transmission through the door, higher-grade magnets and a lower carrier frequency produce a superior through-door transfer, as we will discuss in Sections 3.3.1 and 3.3.2. The final experimental setup, detailed in Chapter 6, uses 52 MGOe magnets and a 21 kHz carrier, with test coils of higher quality factor. However, the result found here using a 90 kHz carrier, weaker magnets, lower-Q test coils is applicable and important to our design nonetheless.

Magnet Selection

The magnetization strength, or "grade" of a permanent magnet is measured in megagauss-oersteds (MGOe). The highest grade commericially available magnets are made of a Neodymium alloy (NdFeB) and can be purchased up to a magnetization of 52 MGOe. However, this material is very brittle and prone to corrosion, so high-grade Neodymium magnets are usually only available with a nickel or zinc coating, which is roughly fifteen times as conductive as the iron in the steel alloy of the breaker panel door. Out of concern for eddy current losses in the resonators from this conductive coating, Samarium Cobalt (SmCo) magnets of grade 26 MGOe, which are commonly available unplated, were used in previous work [6–8].

To evaluate the effect of eddy currents in various permanent magnet materials, a set of test coils was wound with interchangable cores. These coils were wound separately from test coils used in our experimental setup and were used only for this experiment. The inductance, series resistance, and quality factor of each coil was

measured for an air core and various permanent magnet cores, and the results are listed in Table 3.2. The results demonstrate that all the magnet materials tested have roughly the same amount of impact on the quality factors of the coils. Series resistance measured increases substantially between air cores and magnet cores, but the fractional differences between magnet materials are very small. Furthermore, as we will see with the experimental resonators designed in Section 3.4, the additional losses we measure in the nickel-plated neodymium core are very small compared to the effect of eddy current losses in the steel door itself. These results justify the use of higher-grade neodymium magnets in our experimental setup (Chapter 6) despite the marginally higher losses from their plating material.

3.3.2 Frequency Selection

The choice of carrier frequency for the inductive link requires the consideration of two kinds of shielding by the steel door. At high frequency, the permeability of the steel diminishes, thereby decreasing the shielding effect due to ferrormagnetism in the steel [5]. However, the shielding effect due to eddy currents induced in the steel intensifies as frequency increases. In [5], which characterized alloy 1018 low-carbon steel, a magnetic relaxation was observed at approximately 5 kHz. Using the experimental setup in Section 3.3.1 used to test the permanent magnet pole configurations, a global maximum in the voltage transfer function between the two test coils was experimentally confirmed at about 5 kHz. For typical operation in our experimental setup, we increase our choice of carrier frequency of 20kHz to avoid the audio band.

3.4 Experimental Resonator Design

A set of test coils were designed for experimental evaluation according to the design guidelines discussed in Section 3.2.2.

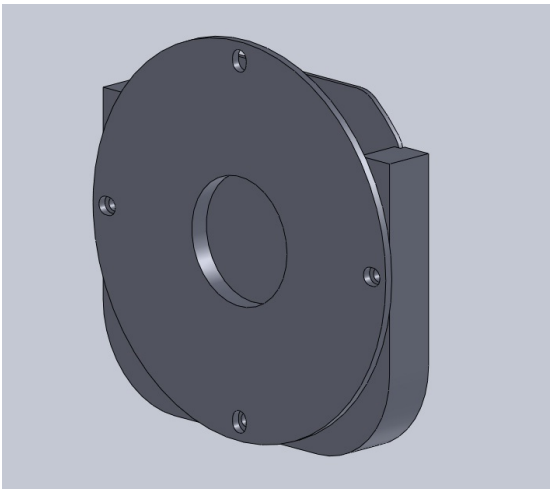
3.4.1 Mechanical Design

The mechanical coil structure consists of a delrin bobbin, clip, and magnet holder machined according to procedures included in Appendix B.2.3. Drawings of these components are shown in Figure 3-14. Since the k of a pair of coils goes roughly as d^{-3}, where d is the distance separating the coils [22], the bobbins are designed with a very thin bottom edge of delrin separating the windings from the steel. The bobbin is made 3/8" wide to allow space for many turns of wire if desired. The core of the bobbin consists of a modular magnet holder designed to hold a 1"x1"x1/4" permanent magnet for saturation of the steel door. The edges of this magnet holder are also made very thin so that the windings can be placed as close to the magnet core as possible such that the induced magnetic flux passes through the saturated region of steel directly beneath and around the magnets.

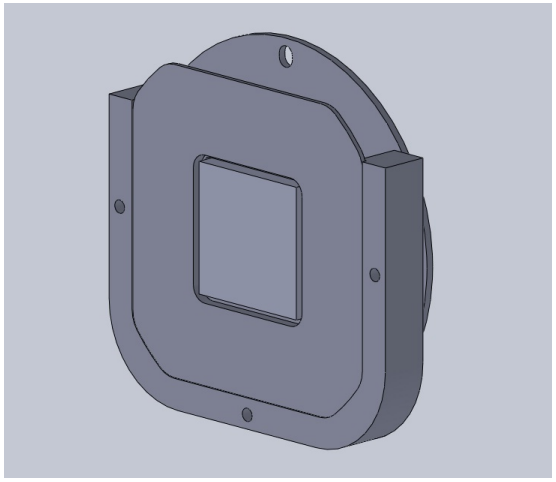
Very high grade magnets, such as the 52 MGOe NdFeB magnets we use, saturate the steel to such an extent that they physically repel one another when placed in a configuration with opposing poles facing each other through the steel. Such a configuration is not inherently physically stable and must be secured mechanically. The delrin clip secures the bobbin and magnet holder in place, as shown in Figure 3-14c. The clip is secured to the door using epoxy or glue, and the bobbin can slide in our out of the fixed clip, secured there with three 6-32 nylon machine screws.

3.4.2 Measured Properties

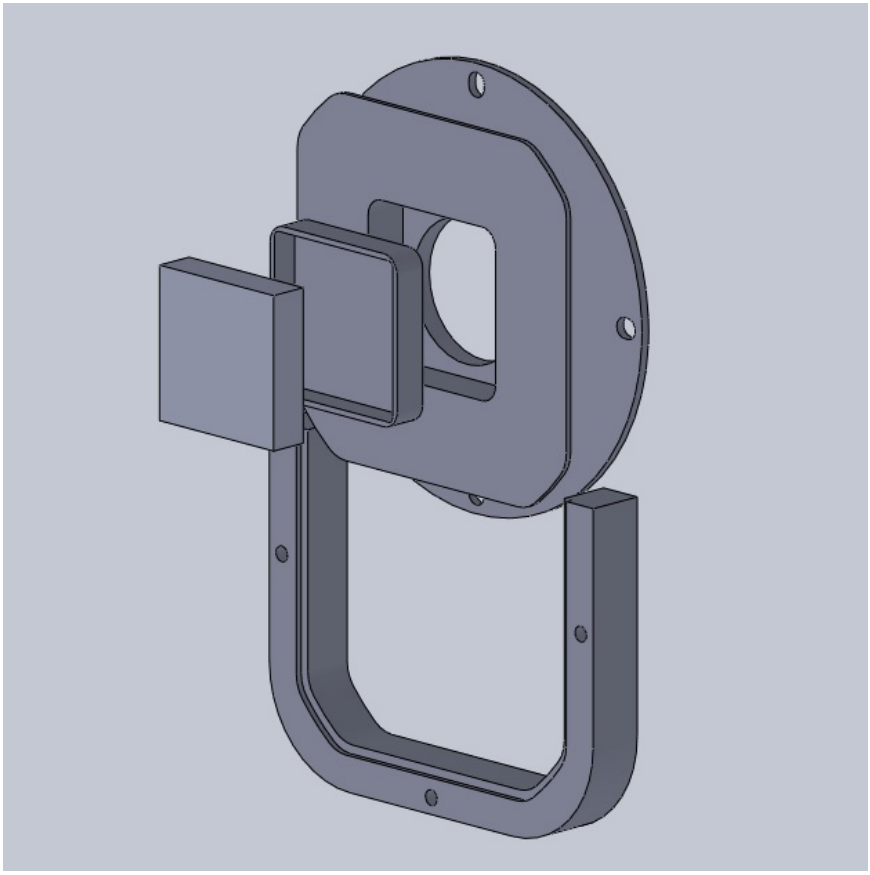
Coils were wound on this mechanical structure with wire gauges ranging from 20 AWG to 35 AWG. At 25 AWG and above, all coils were wound to the capacity of the mechanical structure described in the previous section. Measured parameters for these coils are listed in Table 3.3. It's worth noting how radically the quality factor of each coil decreases as it is placed on the door. While the quality factors of coils in air range from 13.57 to 82.80, they all reduce to about 4 on the door, indicating that the eddy current losses in the door dominate the parasitics. This is particularly notable since it makes the difference in losses due to magnet platings even less significant in our



(a) Front View



(b) Back View



(c) Exploded View

Figure 3-14: Diagrams of coil bobbin, clip, and magnet holder.

	Air Core			Mounted on Panel		
Coil	L	R	Q	L	R	Q
15 / 20 AWG	16.59 μH	153.7 mΩ	13.57	13.75 μH	440.6 mΩ	3.92
30 / 20 AWG	69.20 μH	367.7 mΩ	23.65	56.03 μH	1.657 Ω	4.24
350 / 25 AWG	7.62 mH	16.81 Ω	57.00	5.97 mH	187.3 Ω	4.00
1000 / 30 AWG	59.76 mH	90.75 Ω	82.80	46.54 mH	1.414 kΩ	4.13
3000 / 35 AWG	732.4 mH	2.46 kΩ	37.35	493.8 mH	19.00 kΩ	3.26

Table 3.3: Measured parameters of experimental test coils.

design. For our experimental setup, discussed in Chapter 6, the 30-turn 20 AWG and 1000-turn 35 AWG coils were selected for the outer and inner resonators, respectively, because they have the highest quality factors. Their parameters when mounted on the door with the magnet configuration described in Section 3.3.1 are listed in Table 6.3 in Chapter 6.

Chapter 4

Signal Conditioning

The purpose of the signal conditioning circuitry is to recover the original 60 Hz current signal sensed at the breaker face. The circuit executes four functions:

- Drive the through-door link with a carrier waveform.
- Sense and amplify the impedance-modulated carrier.
- Demodulate the modulating signal to baseband.
- Digitize the demodulated signal for compensation and analysis.

This circuitry demodulates an amplitude modulated signal. Challenges arise from the ultra-low modulation depth of the sensed signal at the front-end, which has only microvolts of modulation on top of volts of carrier due to the low coupling between the resonators of the through-door link. Furthermore, the circuit must be designed to minimize part count and physical size so that it may be mounted on or near the circuit breaker panel.

This chapter begins with an overview of the signal processing chain, followed by more detailed descriptions of the individual blocks that make up the circuit. Measurements of circuit performances as well as complete tables of component selections for our experimental setup are listed in Chapter 6.

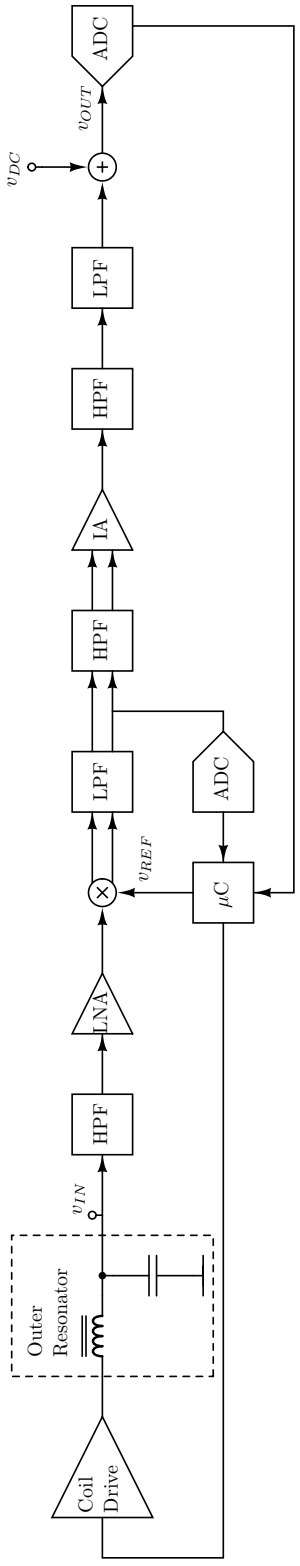


Figure 4-1: Block diagram of signal processing chain.

4.1 Overview

A block diagram of the signal processing chain is shown in Figure 4-1. The front-end of the chain is connected to the voltage across the resonant capacitor of the outer resonator of the through-door link. This voltage takes the form of a carrier-frequency waveform, amplitude modulated with the changing driving-point impedance of the resonators. The signal is immediately high-pass filtered to remove any DC offset so that gain may be applied without saturating the amplifiers. Following the high-pass filter is a low-noise amplifier designed to gain the signal away from the noise floor so as to maintain a high signal-to-noise ratio as active circuits further down the signal chain contribute additional noise. The gain of this stage is set to the maximum possible without saturating the amplifier.

Following the low-noise amplifier is a passive balanced downconverting square-wave mixer with differential-mode outputs that multiplies the amplified, amplitude-modulated signal with an in-phase carrier signal generated by a microcontroller unit (MCU). The output of the mixer is a differential signal consisting of the desired baseband signal, an image signal at twice the carrier frequency, and other higher-frequency images resulting from multiplication by the odd harmonics of the carrier. This is passed through a fully-differential band-pass filter made from series-connected fully-differential low-pass and high-pass filters. The purpose of the band-pass filter is to remove unwanted residual signals from downconversion so that more gain can be applied to the baseband signal. The low-pass filter removes the image signal and any other high-frequency residual signals from the mixer, while the high-pass filter strips the DC content left from demodulation of the unsurpressed carrier.

The phase of the carrier reference signal supplied to the mixer by the MCU is calibrated by feeding back the DC voltage at the output of the differential low-pass filter to the MCU via an internal analog-to-digital converter (ADC). This DC voltage is used as a metric for the phase offset between the sensed AM signal and the local carrier reference generated by the MCU. A hill-climbing algorithm is used to adjust the phase of the carrier reference so that the DC level at the output of the low-pass

filter is maximized. This calibration algorithm is discussed in more detail in Section 4.4.

An instrumentation amplifier connected to the output of the band-pass filter adds substantial gain to demodulated signal so that general-purpose amplifiers can be used for the rest of the signal chain without concern for noise. The instrumentation amplifier also converts the differential signal from the band-pass filter to a single-ended one. The rest of the signal chain is a series of filters implemented with general-purpose op-amps that are designed to limit the signal to our desired bandwidth in order to minimize noise and remove any remaining image-frequency content or offset. The final output signal is passed to an internal 10-bit ADC in the MCU for digital compensation and analysis.

Component value selections in our experimental setup for all the circuits described here are listed exhaustively in Section 6.1.3. Complete schematics of our experimental implementation of these circuits are given in Appendix C.

4.2 Coil Drive

The coil drive circuit is designed to drive the outer resonator of the through-door link at a carrier frequency set to its resonant frequency. The circuit is implemented as half-bridge of two IRF530A power MOSFETs, shown in Figure 4-2. The MCU generates two gate drive signals at the carrier frequency that are 180° out of phase with one another, with an adjustable "dead time" between pulses to avoid shoot-through. The gates of the two power MOSFETs are driven by International Rectifier IR2125 gate driver ICs, through 10 Ω resistors to limit ringing. The DC power supply for the half-bridge circuit is separate from that of the analog signal-processing and gate driver circuitry, so that it may be independently adjusted to produce a desired voltage amplitude across the JFET modulator connected to the inner-door resonator.

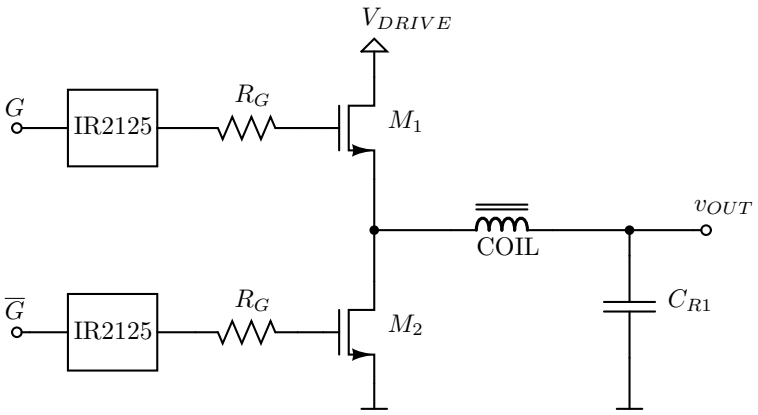


Figure 4-2: Schematic of coil drive circuit.

4.3 Low-Noise Front End

The input signal to our circuit has only microvolts of modulation on top of volts of carrier waveform. At this level, our signal of interest (the modulation) is very suceptible to thermal noise introduced by resistors and active devices in the signal path. The purpose of the low-noise front-end is to provide as much gain to the input signal as possible while adding as little noise as possible. Amplifying the signal at the front end significantly reduces the degradation of the signal-to-noise ratio by other devices in the signal chain because their noise contributions are constant and additive, regardless of the signal level. Adding gain at the front-end with a low-noise amplifier allows noise performance to be traded for other desirable characteristics (i.e. power consumption, cost) in the devices that make up the subsequent stages in the signal chain.

The front-end amplifier circuit is shown in Figure 4-3a. It is a simple non-inverting op-amp gain stage made with a Linear Technology LT1028 ultra-low noise op-amp. The input from the resonator is coupled to the non-inverting input terminal of the op-amp with an RC high-pass filter consisting of C_B and R_B. The gain is set by the resistor divider of R_{F1} and R_{F2}. In practice, the gain is set as high as is possible without saturating the amplifier. The absolute values of the gain resistors R_{F1} and R_{F2} are selected to minimize noise.

4.3.1 Noise Analysis of the Front-End Amplifier

The noise contribution of an op-amp can be modeled as a combination of an effective input noise voltage e_n and input noise currents i_n alongside a noiseless op-amp [19]. The input voltage noise is modeled as a series voltage source at one of the two input terminals to the op-amp, while the input current noise is modeled as shunt current sources to ground at each of the input terminals. Series mean-squared voltage noise density from a resistor is given by:

$$\overline{v_{nR}^2} = 4kTR \quad \mathrm{V}^2/\mathrm{Hz}. \tag{4.1}$$

Dividing by the resistance R gets the equivalent parallel noise current density:

$$\overline{i_{nR}^2} = \frac{4kT}{R} \quad \mathrm{A}^2/\mathrm{Hz} \tag{4.2}$$

where k is Boltzmann's constant and T is the circuit temperature in Kelvin.

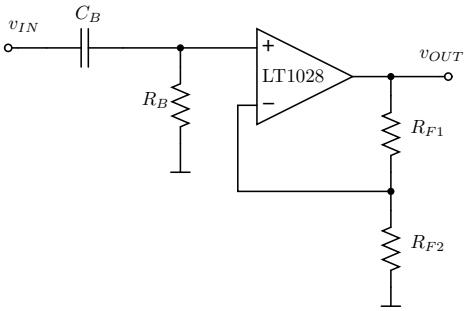
A circuit model of the front-end amplifier with all these equivalent noise sources is shown in Figure 4-3b. Since all these noise sources are linear and independent, we can calculate the total output noise of the stage by superposition, summing the squared magnitudes of the transfer functions from the individual noise sources to the output:

$$\overline{v_{no}^2} = \sum_{\forall x} |\alpha_x(s)|^2 \, \overline{v_{nx}^2} \tag{4.3}$$

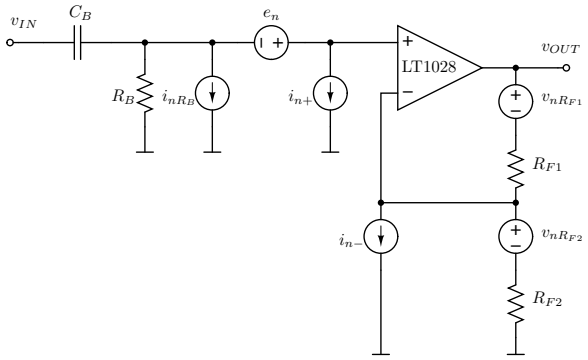
where α_x is the transfer function from noise source v_{nx} to the output. The total mean-squared output voltage is then given by integrating over the bandwidth of the circuit. If we are operating over a narrow bandwidth, as in our case where our signal of interest is in a small band around a high carrier frequency, we can approximate that the magnitudes of the transfer functions are constant over the band,

$$|\alpha_x(s)|^2 \approx \alpha_x^2, \tag{4.4}$$

and simply multiply by the circuit bandwidth Δf to get the total mean-squared



(a) Schematic



(b) Noise Model

Figure 4-3: Schematic of low-noise front-end amplifier with and without noise sources.

voltage noise at the output.

Analyzing the circuit in Figure 4-3b, we begin by assuming that C_B is very large, such that its nominal impedance at the carrier frequency is very low, shunting away noise from R_B as well as the op-amp current noise at its non-inverting input:

$$\alpha_{R_B} \approx 0 \tag{4.5}$$

$$\alpha_{i_+} \approx 0. \tag{4.6}$$

The input noise current at the inverting terminal is converted to an input voltage by the parallel combination of R_{F1} and R_{F2}, then amplified by the gain of the op-amp circuit, G,

$$\alpha_{i_-} = \frac{GR_{F1}R_{F2}}{R_{F1} + R_{F2}}. \tag{4.7}$$

Finally, the voltage noise from R_{F1} goes straight to the amplifier output, while the

noise from R_{F2} goes directly to the input, so that

$$\alpha_{R_{F1}} = 1 \tag{4.8}$$

$$\alpha_{R_{F2}} = G \tag{4.9}$$

The net mean-squared output voltage noise density is then

$$\overline{v_{no}^2} = (4kT)^2(R_{F1}^2 + G^2R_{F2}^2) + G^2e_n^2 + G^2i_n^2\left(\frac{R_{F1}R_{F2}}{R_{F1}+R_{F2}}\right)^2 \quad \text{V}^2/\text{Hz}. \tag{4.10}$$

The noise *contribution* of the amplifier is often expressed in terms of an equivalent noise voltage at the input, known as the output noise *referred-to-input* (RTI). We arrive at this by dividing the mean-squared output voltage noise density by G^2:

$$\overline{v_{n_{RTI}}^2} = \left(\frac{4kTR_{F1}}{G}\right)^2 + (4kTR_{F2})^2 + e_n^2 + i_n^2\left(\frac{R_{F1}R_{F2}}{R_{F1}+R_{F2}}\right)^2 \quad \text{V}^2/\text{Hz}. \tag{4.11}$$

This is the expession that we want to minimize, and it suggests three things. First, increasing the gain will lower the total noise contribution by reducing the effective contribution from R_{F1}, since its noise goes directly to the amplifier output. This is no different from the principle we discussed earlier that front-end gain reduces the effective noise contribution of subsequent stages. Second, we can reduce the contribution from resistor noise and op-amp current noise by decreasing the size of resistors R_{F1} and R_{F2}. Lastly, the minimum noise contribution of the stage is set by e_n, which can not be reduced.

The design implication of this is that the gain should be set to be as large as possible without saturating the amplifier. This sets the relative values of gain resistors R_{F1} and R_{F2}. Their absolute values should reduced until either we reach the output current limitations of the op-amp or e_n begins to to dominate the total noise RTI.

4.4 Downconverting Mixer

The amplitude-modulated waveform at the output of the front-end gain stage can be represented as:

$$R(t) = A\cos(\omega_c t + \phi_1) + m(t)B\cos(\omega_c t + \phi_1). \tag{4.12}$$

This expression assumes that any high-frequency harmonics of the carrier frequency from the coil drive are perfectly filtered out by the resonator of the through-door link. The first term in the expression represents unsurpressed carrier content, while the second represents the carrier modulated by a modulation function $m(t)$ corresponding to the current sensed at the breaker face. ϕ_1 is the phase of the incoming carrier signal.

The purpose of the downconverting mixer is to extract $m(t)$ from this waveform. This can be accomplished by multiplying $R(t)$ with a reference signal at the carrier frequency:

$$A\cos(\omega_c t + \phi_1)\cos(\omega_c t + \phi_2) + m(t)B\cos(\omega_c t + \phi_1)\cos(\omega_c t + \phi_2). \tag{4.13}$$

where ϕ_2 is the phase of the reference signal. Using the product-to-sum identity

$$\cos u \cos v = \frac{1}{2}\left(\cos(u - v) + \cos(u + v)\right), \tag{4.14}$$

this simplifies to

$$\frac{A + Bm(t)}{2}(\cos(\phi_1 - \phi_2) + \cos(2\omega_c t + \phi_1 + \phi_2)), \tag{4.15}$$

which contains the desired baseband signal $m(t)$, attenuated by the cosine of the phase difference between the incoming modulated signal and the local oscillator. The other two products of demodulation are a DC offset proportional to the cosine of the same phase difference, and an image signal at twice the carrier frequency.

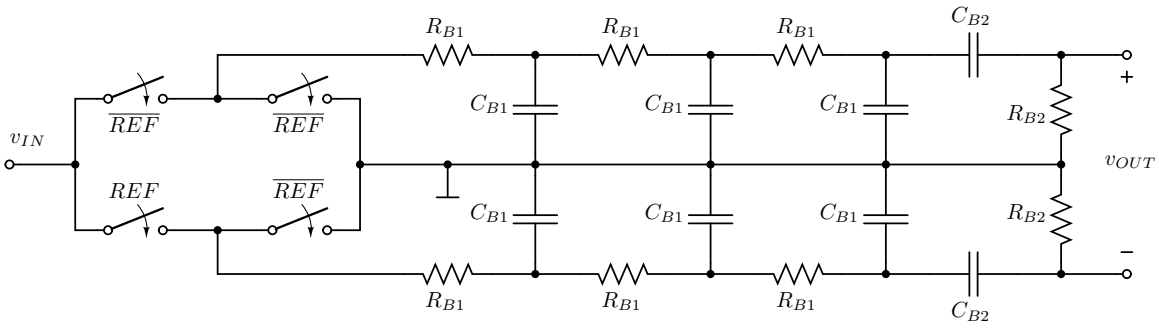


Figure 4-4: Schematic of full-bridge mixer and band-pass filter.

4.4.1 Mixer Topology

Our mixer is a passive, balanced, differential-mode output square-wave multiplier. A schematic of the mixer and subsequent band-pass filter is shown in Figure 4-4. The mixer is implemented with a full-bridge of analog switches, driven by two square waves G_1 and G_2 that are at the carrier frequency and 180° out of phase. In this way, the full bridge effectively multiplies the modulated signal with a carrier-frequency square wave with a peak amplitude of 1. Thus, in addition to multiplying the modulated signal by $\cos(\omega_c t + \phi_2)$ as in (4.13), the square-wave multiplier also multiplies by odd harmonics of ω_c, according to the fourier series of a square wave:

$$\frac{4}{\pi} \sum_{n=1,3,5,\ldots}^{\infty} \frac{1}{n} \sin(n\omega_c t) \tag{4.16}$$

Multiplication by these higher harmonics will result in additional image signals at high frequency, but these will all be filtered out in the subsequent band-pass filter along with the 40 kHz image from multiplication with the carrier fundamental.

The band-pass filter is a 3rd-order fully differential *RC* low-pass ladder connected to the mixer output, followed by an unbuffered *RC* high-pass filter. The purpose of the low-pass ladder is to severely attenuate high-frequency image signals at twice the carrier frequency and above, while the high-pass component simply removes the DC offset resulting from the downmodulated unsurpressed carrier.

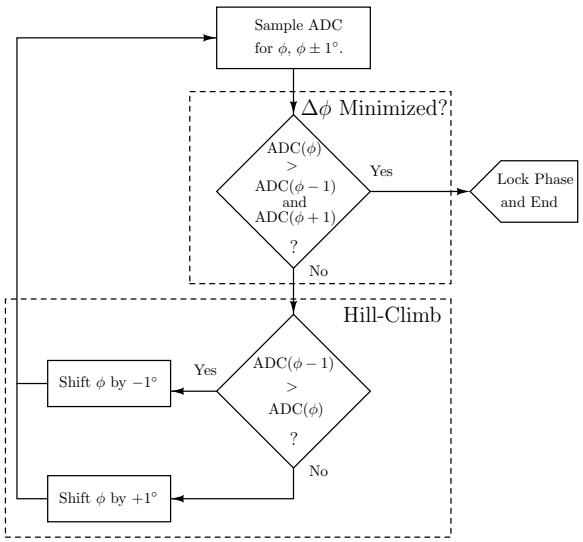


Figure 4-5: Flow chart for phase calibration algorithm.

4.4.2 Digital Phase Calibration

According to expression (4.15), the amplitude of the modulating signal $m(t)$ after downconversion is proportional to the cosine of the phase difference between the sensed signal and the carrier reference signal. Our circuit implements a quasi-phase-locked loop (PLL) to adjust the phase of the mixer gate drive signals to match that of the input signal. This is accomplished by monitoring the DC level at the output of the low-pass RC ladder, which, as expression (4.15) demonstrates, is also proportional to the cosine of the phase offset we want to minimize. This DC level is fed into an internal ADC in the microcontroller, which adjusts the mixer drive phase using a hill-climbing algorithm, with the DC offset as a heuristic, until the DC level is maximized. A block diagram of this algorithm is shown in Figure 4-5.

4.5 Filter Chain

Following the band-pass filter, the demodulated signal converted to a single-ended signal by an Analog Devices AD620 instrumentation amplifier. The instrumentation amplifier also adds a substantial amount of gain so that inexpensive, relatively noisy op-amps can be used throughout the rest of the signal chain. These op-amps im-

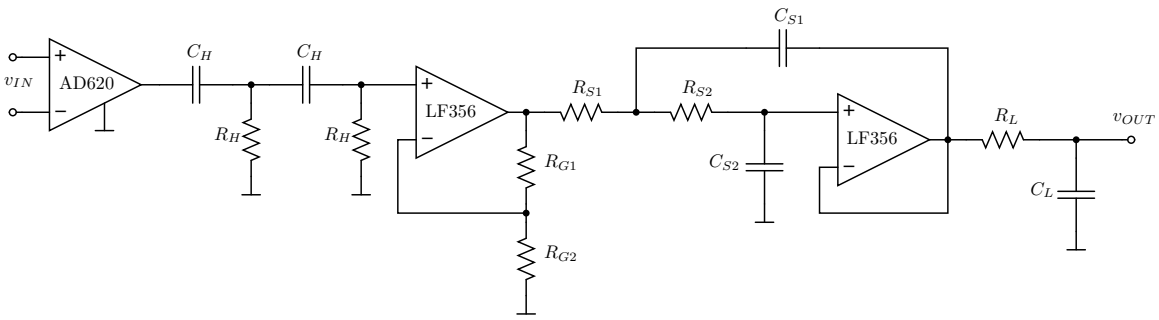


Figure 4-6: Schematic of filter chain.

plement a series of filters to remove any remaining unwanted residual signals from downconversion, as well as reduce the noise bandwidth to only our bandwidth of interest, which includes 60Hz and its first ten harmonics. A schematic of the instrumentation amplifier and filter chain is shown in Figure 4-6.

Immediately following the instrumentation amplifier is a second-order *RC* high-pass filter that removes any offset from mismatched bias currents at the instrumentation amplifier input. The high-pass filter also limits the low breakpoint of the system bandwidth to 50 Hz. The high-pass filter is buffered by an op-amp (IC_1) that can add gain if desired. The op-amp drives a second-order Sallen-Key active low-pass filter, built with an op-amp that drives another first-order *RC* low-pass filter. The two low-pass filters are designed to limit the high-breakpoint of the system bandwidth to 600 Hz. All op-amps in the filter chain are general purpose LF356 ICs from Linear Technology.

4.5.1 Analog To Digital Conversion

The last stage of the signal chain is a level-shifter that conditions the demodulated, filtered signal for analog-to-digital conversion. A schematic of the level-shifter is shown in Figure 4-7. The input is another LF356 op-amp buffer that can add gain if desired. It drives a series resistor R_O and DC blocking capacitor C_{DC}. The DC level at the circuit output is set halfway between the digital voltage rail (3.3 V) and ground, which are the reference voltages for the analog-to-digital converter. A pair of diodes shunted to the the power rail and ground prevent overvoltages which could damage the

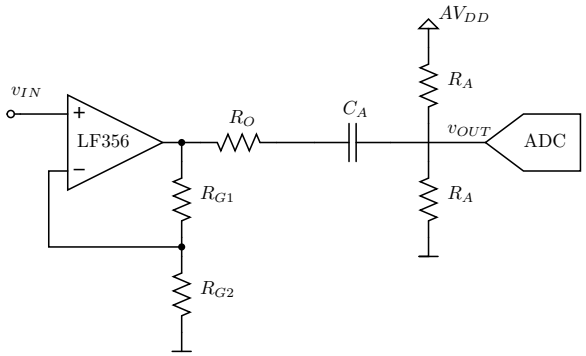


Figure 4-7: Schematic of level shifter circuit.

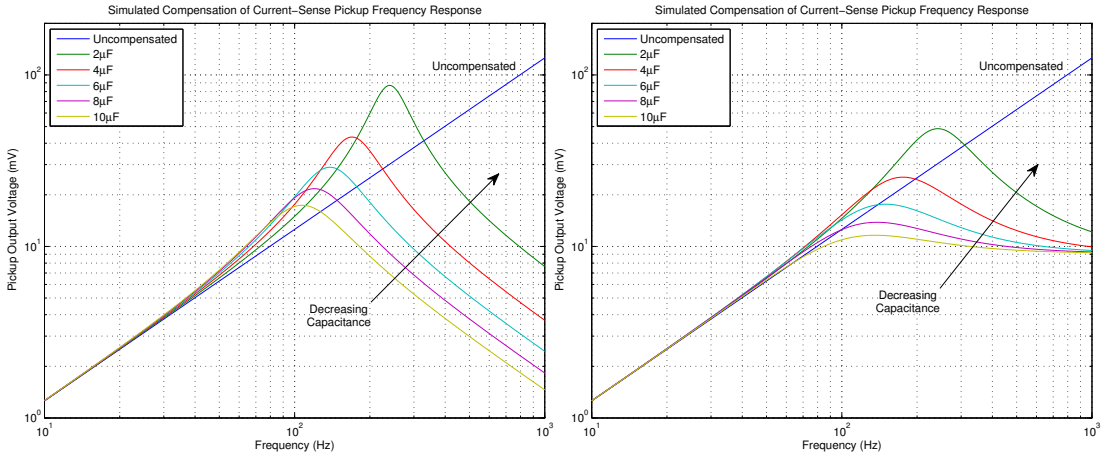
ADC. The resistors are chosen to set the output resistance of the filter chain to about $1\,\mathrm{k}\Omega$, as suggested by the manual for the microcontroller, a dsPIC33FJ256MC710. The blocking capacitor C_{DC} is chosen so that the system bandwidth is preserved.

Chapter 5

Digital Frequency Response Compensation

Chapter 2 discussed the inductive frequency response of the current-sense pickup, and the need to compensate it with a parallel capacitor so that unwanted high-frequency signals are rejected from the sensor. A simulation of the frequency response of the pickup from Chapter 2 is reprinted here in Figure 5-1. The simulation demonstrates that with or without a compensation capacitor, the reactive nature of the current-sense pickup produces a frequency response that is non-uniform. This characteristic, along with additional frequency-dependent phase shifts contributed by the baseband filter chain discussed in Section 4.5, deforms the sensed current signal so that it may not resemble the original current when viewed at the output of the analog signal chain. However, these deformations are linear and can be inverted. This chapter discusses how to accomplish compensation of the non-uniform frequency response of the analog sensor circuitry through digital processing.

In Section 5.1 we characterize the magnitude and phase response of the analog sensor circuitry, and discuss how the characterization can be used to design digital compensation software. Section 5.2 describes the implementation and testing of MATLAB®-based compensator for steady-state periodic signals.



(a) Capacitor compensation (b) Capacitor/resistor compensation

Figure 5-1: An LTSPICE simulation shows how the inductive current-sense pickup has a non-uniform frequency response, regardless of how it is compensated (re-printed from Figure 2-11).

5.1 Compensator Design

In the design of the compensation scheme presented here, it is assumed that the signals processed are periodic and only have frequency content at or near the harmonics of 60 Hz. This assumption is true for nearly all steady-state current signals we can expect to see in the circuit breaker. Under this assumption, the design of a compensator is greatly simplified because it is only necessary to compensate for the phase shifts and magnitude scaling at these specific frequencies. While fitting an inverse filter precisely to the entire frequency response characteristic of the sensor is difficult and can produce a complex, high-order system; manipulating a single frequency is relatively straightforward.

The compensator presented here is simple, and works as follows. An array of digital band-pass filters isolate each individual harmonic of 60 Hz. The scaling and phase shifts contributed by the sensor electronics are inverted for each harmonic independently. Once adjusted, the harmonics are recombined to produce the reconstructed current signal. The precise scaling and shifts that the compensator applies are determined by experimentally characterizing frequency response of the sensor electronics.

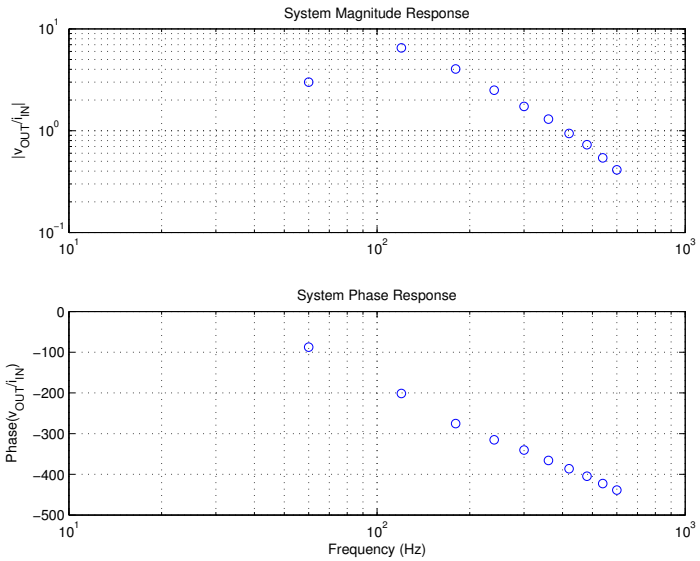


Figure 5-2: Frequency response of the experimental sensor prototype, measured at harmonics of 60 Hz.

5.1.1 System Characterization

The analog sensor system was characterized by running a series of sinusoidal single-frequency test currents through the circuit breaker in the experimental setup described in Chapter 6. For each frequency, the input test current i_{IN} was measured as the voltage v_{R_L} across a resistive test load R_L, and compared to the sensor output v_{OUT}. The measured frequency response is plotted in Figure 5-2 from datapoints corresponding to the first ten harmonics of 60 Hz. The magnitude of the system transfer function H_k at frequency f_k, the k_{th} harmonic of 60 Hz, is calculated as:

$$|H_k| = \frac{v_{OUT_k}}{i_{IN_k}} = \frac{v_{OUT_k} R_L}{v_{R_L}} \tag{5.1}$$

and the phase in degrees ϕ_k is calculated by measuring the time delays t_{dk} between the positive-slope zero crossings of i_{IN} and v_{OUT}:

$$\phi_k = \angle H_k = -f_k t_{dk} \cdot 360^\circ \tag{5.2}$$

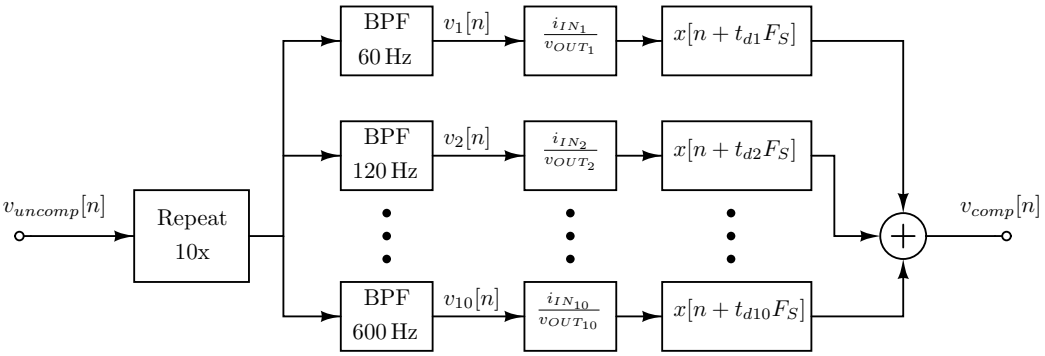


Figure 5-3: Block diagram of the digital frequency response compensation algorithm.

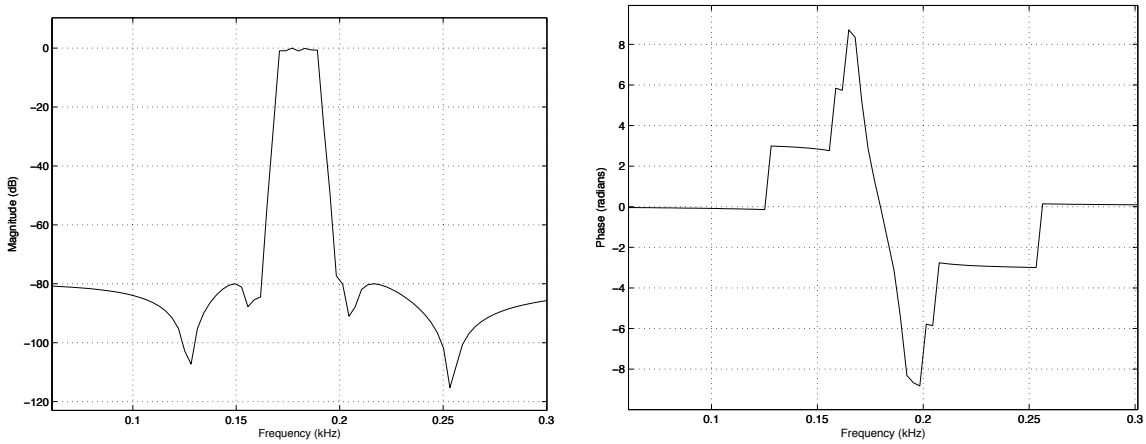
5.1.2 Compensation Algorithm

A block diagram of the overall compensation algorithm is shown in Figure 5-3. The input to the compensator, which is taken from the output of the sensor electronics, is a finite vector of data samples. The vector is be assumed to represent an integer number of cycles of a periodic waveform that extends infinitely in time. The first stage of the algorithm copies and repeats the input vector several times to extend its duration, so that the step response transient produced by the application of the band-pass filters has time to decay. The extended input data vector is then passed through each of the ten band-pass filters in parallel, producing ten filtered vectors of identical length, each containing the time-domain data of one of the 60 Hz harmonics of signal.

The next stage scales each band-passed vector by the inverse of the magnitude data acquired from the sensor characterization by multiplying by i_{IN_k}/v_{OUT_k}. Negative phase shift is applied by simply reversing the time delay measured in the characterization with a circular shift of the data. Once the gains and shifts have been applied, the reconstructed signal v_{comp} is formed by summing all the vectors of compensated harmonic data. Put succinctly:

$$v_{comp}[n] = \sum_{k=1}^{10} \frac{i_{IN_k}}{v_{OUT_k}} v_k[n + t_{dk}F_S] \tag{5.3}$$

where F_S is the sampling rate at which the data was collected from the output of the sensor.



(a) Magnitude Response (b) Phase Response

Figure 5-4: Magnitude and phase response of an example band-pass filter used in digital compensation of the sensor frequency response.

5.2 MATLAB® Implementation and Validation

An example of the digital frequency response compensator is implemented in MATLAB®, using data sampled from an oscilloscope at 50 kHz. The code for the compensator is listed in at the end of this chapter in Section 5.3. The bandpass filters in the implemenation are 12th-order digital eliptical filters with 20 Hz bandwidths centered around the harmonics. Stop-bands are located at -80 dB, 10 Hz from either breakpoint. Each filter is designed so that there is no phase shift immediately at the harmonic frequency. A magnitude and phase characteristic is shown for a 180 Hz band-pass filter in Figure 5-4.

To validate the compensator implementation, an ATX power supply was used to produce a test current with higher harmonic content using the experimental setup described in Chapter 6. More details on the electrical configuration of the power supply can be found in Section 6.2. The data from the output of the sensor was collected from an oscilloscope at a sample rate of 50 kHz. Figure 5-5 plots the time-domain waveforms of the ATX test current as measured with a current probe at the load, the analog output voltage of the signal conditioning circuitry, and the output of the compensator. The visible differences between the digitally compensated waveform and the original current waveform are attributable to band-limiting by the 50 Hz to

610 Hz bandwidth of the sensor. To demonstrate this, in the same figure, the original current sensed at the load is shown after being digitally band-limited to the bandwidth of the sensor. After band-limiting, the current measured at the load appears nearly identical in both magnitude and phase to the reconstructed current signal after digital processing. Figure 5-6 shows fast fourier transforms of the waveforms in Figure 5-5.

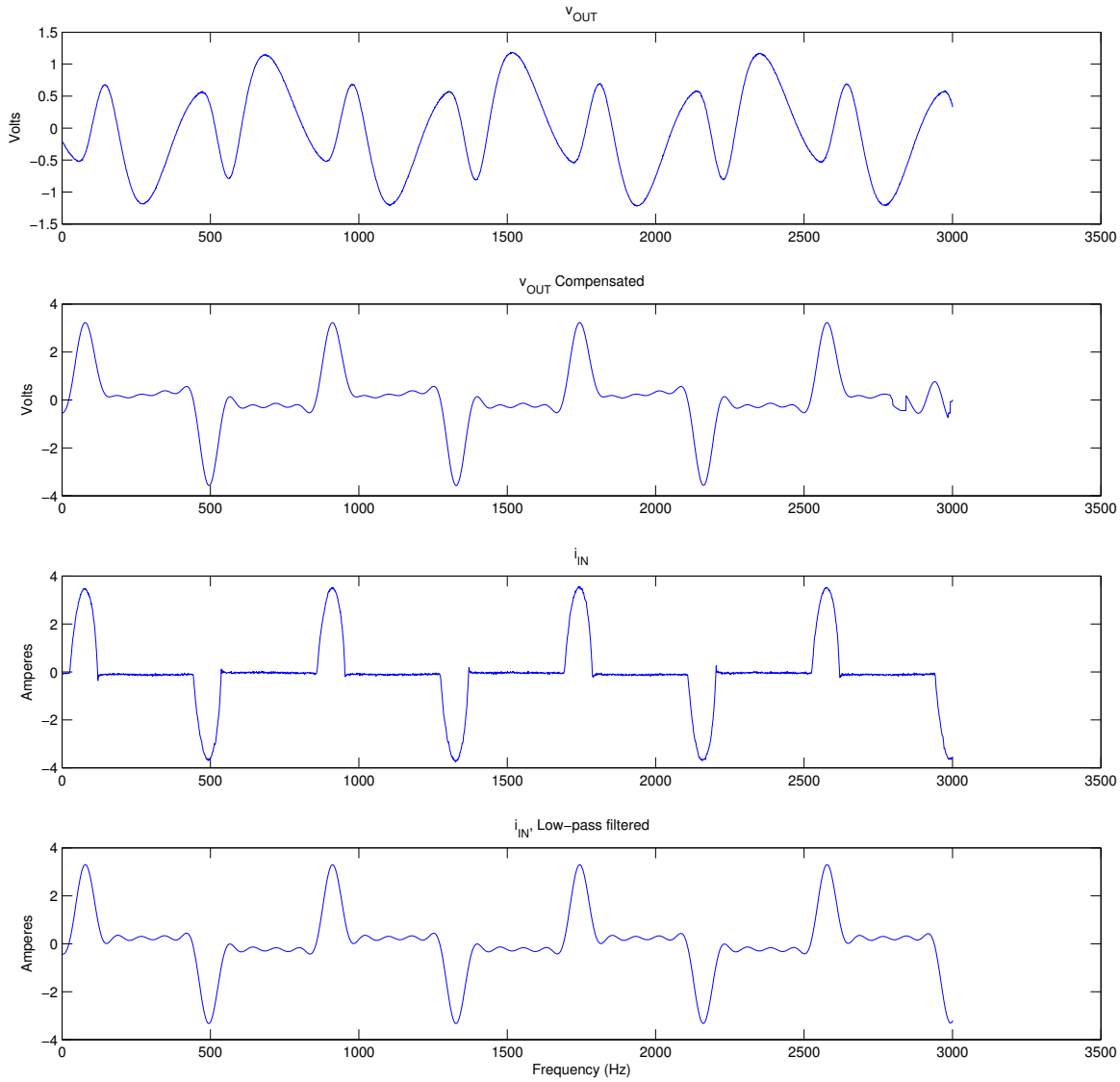


Figure 5-5: Reconstruction and digital frequency-response compensation of a test current with multiple harmonic components.

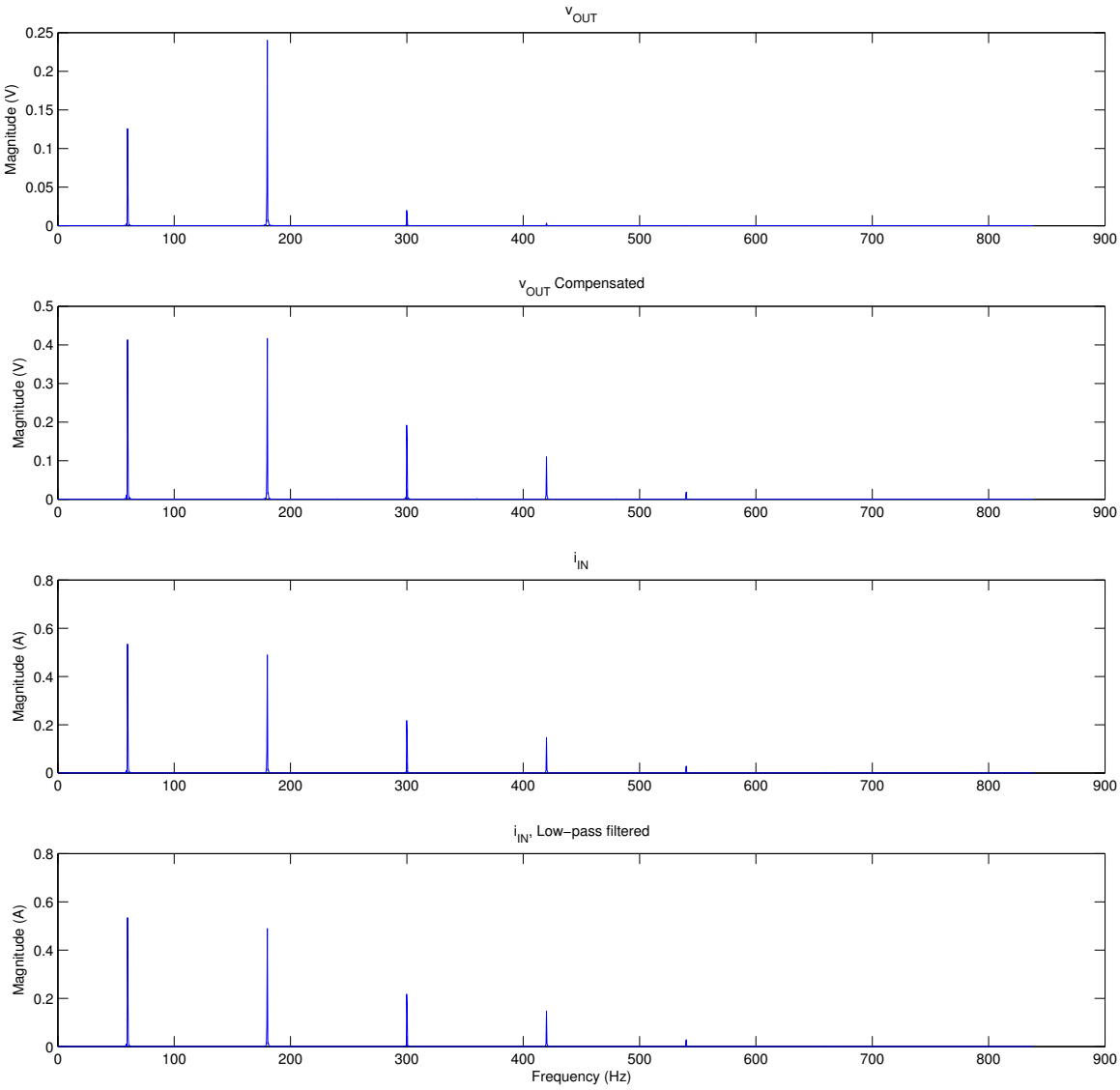


Figure 5-6: Fast fourier transforms demonstrating reconstruction and digital frequency-response compensation of a test current with multiple harmonic components.

5.3 Compensator Source Code

```
%%% Current Sensor Frequency/Phase Compensation %%%
%% Load Workspace
% Load Waveform Data:
load('fcomp_data.mat');

% Load Filters:
load('filters.mat');

%% Measured Freq/Phase Response
% Enumerate Harmonics of 60Hz:
freq = 60:60:600;
% Pk-Pk voltage across 2-ohm load resistor:
vRL = ones(1,length(freq));
% Conver to current by dividing by load resistance:
iIN = vRL / 2;
% Pk-Pk voltage at sensor output:
vOUT = [1.5 3.25 2.02 1.25 0.865 0.65 0.47 0.364 0.27 0.206];
% Positive delay between positive-sloped zero-crossings of input current
% and sensor output voltage:
zc_delay = 1e-3 * [4.05 4.66 4.25 3.65 3.15 0.045 0.174 0.258 0.323 0.365];

gain = vOUT./iIN;

%% Frequency Decomposition/Compensation and Signal Reconstruction
% Run band-pass filters on sensor output, apply empirically measured gains
% and time delays to invert non-uniform frequency response of sensor.

% Select data and filters from imported .mat files:
fs = 50000;
time = vout_50k(:,1);
vout = vout_50k(:,2);
filters = filters_50k;

% Extend input signal ten times:
vout = repmat(vout,10,1);

% Band-pass for each of the first 10 harmonics of 60Hz:
for n = 1:length(freq)
    vout_decomp(:,n) = filter(filters(n),vout);
end

% Compensate For System Gain:
vout_comp = vout_decomp ./ (ones(100e3,1) * gain);
```

```
44
45  % Gain Fudge Factor:
46  vout_comp = vout_comp * -6.0973;
47
48  % Compensate For System Phase Shift:
49  shift = -1 * round(zc_delay * fs);
50
51  for n = 1:length(freq)
52      vout_comp(:,n) = circshift(vout_comp(:,n),[shift(n),0]);
53  end
54
55  % Add back together all the shifted/gained harmonics:
56  vout_recon = sum(vout_comp,2);
```

Chapter 6

Experimental Setup and Results

In this chapter, we evaluate an experimental prototype of the retrofit current sensor. The stage-by-stage modelling of the sensor system presented in the previous chapters guides the design of this prototype, which we present in exhaustive detail here. Section 6.1 discusses component selections, coil design, and physical construction of the sensor as well as the test conditions under which it is evaluated. Section 6.2 lists the sensor specifications we measure. We find the our sensor prototype achieves a current resolution of at least 8 bits with a total harmonic distortion less than 0.01%. In addition, our tests show that currents as low as 20 mA RMS are detectable, and the sensor's ability to measure smaller currents is limited not by noise, but by interference from 60 Hz magnetic fields originating from sources outside the circuit breaker panel.

6.1 Experimental Setup

Photographs of the experimental setup are shown in Figures 6-1 through 6-3. Figure 6-1 shows the entire configuration, in which a circuit breaker panel with four circuit breaker units and two accessible circuits is mounted on a piece of plywood. The panel is configured such that it may operate from either utility voltage or a laboratory power source. Electrically, the panel is configured identically to a circuit breaker panel at the main utility entrance to a building, except that neutral and earth are not connected within the panel.

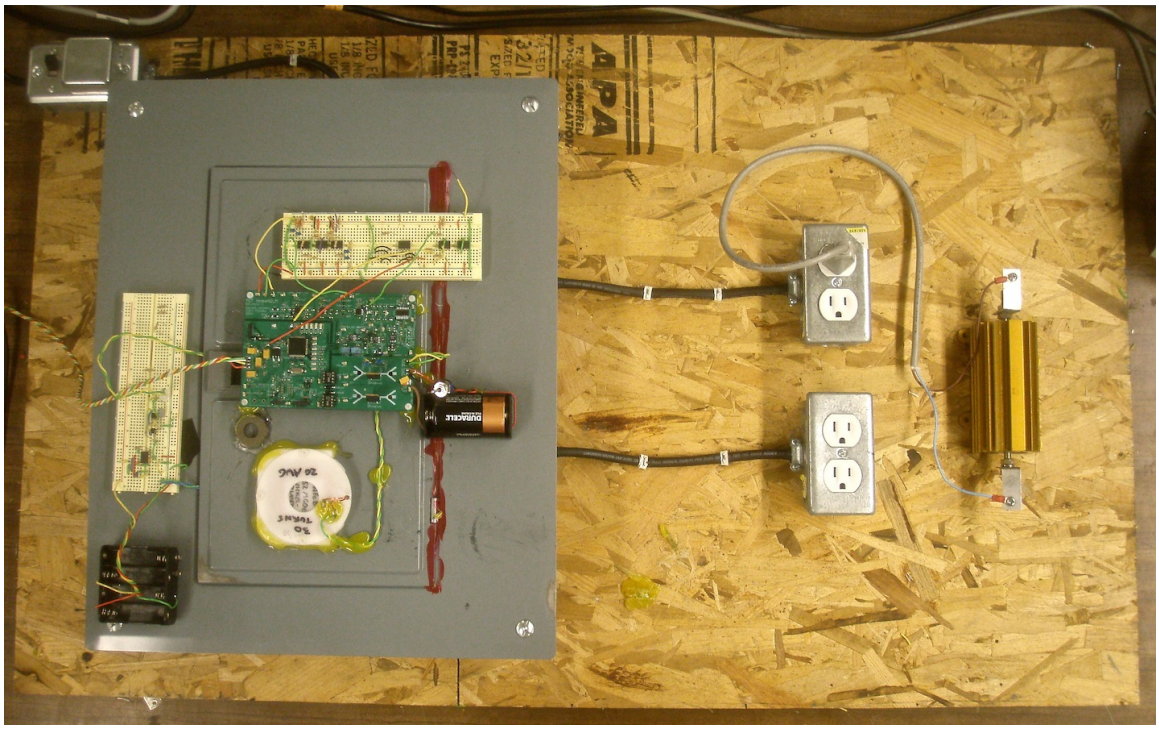


Figure 6-1: Experimental Setup

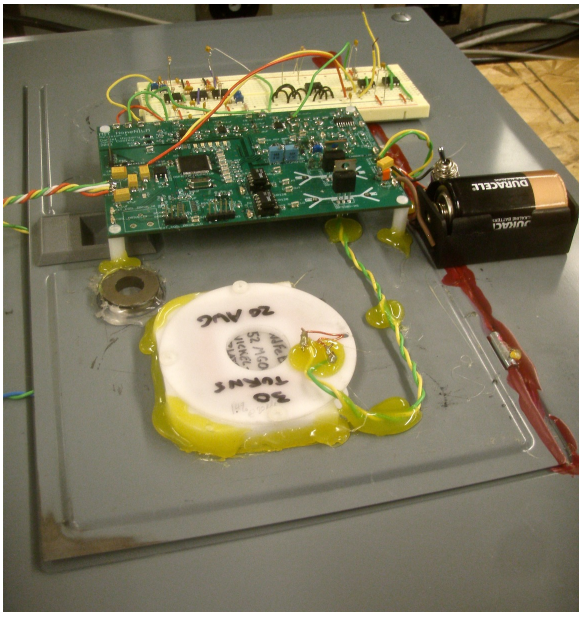


Figure 6-2: Close-up of signal conditioning electronics and outer resonator coil mounted on the circuit breaker panel.

Figure 6-3: Inner-door coil of through-door link in the experimental setup.

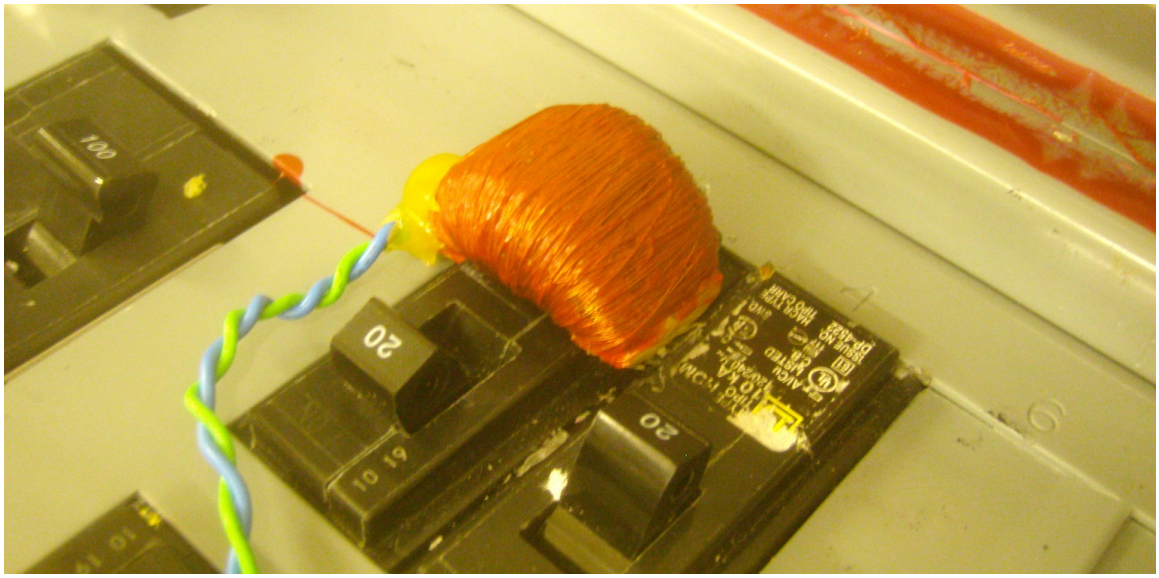


Figure 6-4: Current-sense pickup mounted on circuit breaker in the experimental setup.

The coil drive, sense, and demodulation circuitry is mounted to the front of the breaker panel on a printed circuit board (PCB). A solderless breadboard adjacent to the PCB contains additional modifications to the original PCB design. Schematics for the PCB and breadboard circuits and the layout of the PCB are available in Appendix D. Near the bottom edge of the door, the through-door coil of the outer link is wound around the bobbin fixture described in Section 3.4. The bobbin fixture is secured to the door using hot glue. The inner coil is similarly attached to the precise opposite side of the steel door, using an identical bobbin fixture, as shown in Figure 6-3.

The current-sense pickup is placed at the surface of a 20 A breaker unit, as shown in Figure 6-4. The pickup is connected to the in-panel electronics, which are constructed on a solderless breadboard mounted on the left-hand side of the circuit breaker panel. The solderless breadboard, which contains both an instrumenation amplifier-based amplification stage and the JFET modulator circuit, can be placed behind the breaker panel door without affecting operation of the sensor. For this experiment, we leave the breadboard mounted on the left-hand side of the panel for accessibility when taking measurements of the circuit.

An HP 6834B AC power source was used to generate sinusoidal test current signals, and a Bestec ATX-300-12E computer power supply was used to generate a non-sinusoidal test current typical of AC-DC converters. Sinusoidal test currents of 500 mA and higher were run through a 2Ω load resistor, while all lower currents were run through a 100Ω load resistor. Time-domain signals were measured on a Tektronix TDS-3014B oscilloscope, and frequency-domain measurements were taken with a Tektronix RSA-3303A real-time spectrum analyzer.

6.1.1 In-Panel Electronics

The current-sense pickup is constructed from two halves of a toroidal high-permeability core, the Ferroxcube TX25/15/10-3E6 with relative permeability $\mu \approx 10,000$ [13]. The two halves are joined together with hot glue and secured to the circuit breaker face. Around the toroid are 2000 windings of 35 AWG magnet wire. Electrical prop-

Current-Sense Pickup Design	
Property	Value
Toroid	Ferroxcube TX25/15/10
Material	3E6
Initial Permeability μ_i	$\approx 10000\,\mathrm{H/m}$
Turns	2000
Wire Gauge	35 AWG
Inductance L	210 mH
Resistance R	$118\,\Omega$
Open-Circuit Voltage @ 5 A RMS	$37\,\mathrm{mV_{pk\text{-}pk}}$

Table 6.1: Design and properties of the inductive current-sense pickup used in the experimental setup.

Pickup Amplifier Design	
Component	Value
R_B	$18\,\mathrm{k}\Omega$
C_R	$10\,\mu\mathrm{F}$
R_G	$6.8\,\mathrm{k}\Omega$
Inst. Amplifer	AD627
Batteries	2x AA Cells

Table 6.2: Components used for the pickup amplifier in the experimental setup.

erties of the current-sense pickup are given in Table 6.1. The compensation cap C_C across the terminals of the current-sense pickup was chosen so as to not drastically attenuate signals within our band of interest (50 Hz to 610 Hz) based on the simulation in Section 2.1 using parameters from Table 6.1.

Sense signals from the pickup are amplified by the instrumentation amplifier circuit discussed in Section 2.3.2. It's schematic is reprinted here in Figure 6-5 along with component values in Table 6.2. We select $R_G = 6.8\,\mathrm{k}\Omega$ so that the instrumentation amplifier gain to 34.4. This value is chosen empirically to work with the current levels we use in our experiment (10 mA to 5 A). In experiments in which the instrumenation amplifier is driven directly with a function generator, R_G is removed to set the gain to 5, which is the lowest possible gain for the AD627 IC.

Biasing resistors R_B are used to bias the input terminals of the instrumentation amplifier because a center-tap is difficult to implement on the current-sense pickup. Since the amplifier gain is low, DC offset from high-impedance biasing resistors or

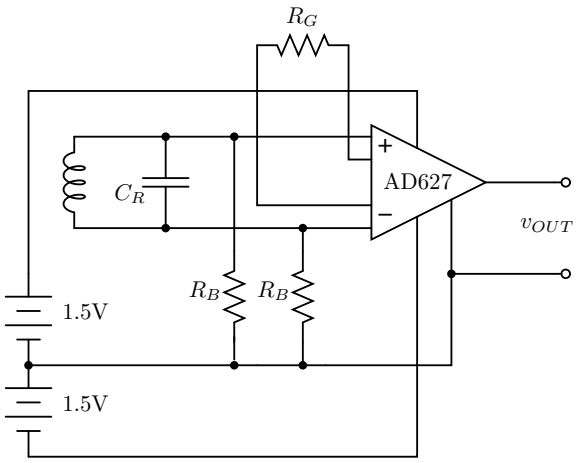


Figure 6-5: Pickup amplification circuit used in the experimental setup. Component values are given in Table 6.2.

resistor mismatch is not a concern. The value of resistors R_B is selected based on reference designs in [4].

The PN4117 JFET devices in the modulator circuit were matched using a curve tracer.

6.1.2 Coil Design

The coils used in the sensor prototype were taken from the set of test coils presented at the end of Chapter 3 in Section 3.4. Of the five coils built, the two coils with the highest Q were selected. Their measured parameters are reprinted here in Table 6.3 along with parameters of their corresponding resonant capacitors, chosen to resonate at 20 kHz. 20 kHz was chosen for the operating frequency because it is the lowest inaudible frequency above the ≈ 5 kHz relaxation point of steel observed in Section 3.3.2. In industrial applications where the sensor may be installed in environments that already have substantial background noise, a lower frequency could be considered for improved performance.

The turns ratio of the two coils is chosen to provide a voltage transformation that allows us to drive the outer coil with safe voltage levels and maintain a reasonable carrier voltage across the JFET mixer that does not drive it out of its linear range.

At the center of each coil is a core of eight 52 MGOe grade neodymium magnets

Through-Door Link Resonator Design							
Resonator	Turns	Gauge	L	R_L	C	R_C	Q
Outer	30	20 AWG	54.58 μH	1.46 Ω	1.04 μF	118.0 mΩ	4.36
Inner	1000	30 AWG	44.74 mH	1.36 kΩ	1.02 mF	84.0 Ω	3.89

Table 6.3: Properties of resonators used for the inductive through-door link in the experimental setup. Measurements are taken at 20 kHz.

of dimension 1/2"x1/2"x1/8", aligned in a pattern of four checkered poles, as shown in Figure 3-10. The magnets on either side of the door are twisted so that like poles face one another through the steel and their magnetic fields repel. The coil bobbins are secured to the door with hot glue.

6.1.3 Signal Conditioning Circuitry

The signal conditioning circuitry and coil drive are designed according to the guidelines presented in Chapter 4. The smallest resistors than can be driven by the LT1028 are selected for the LNA feedback path in order to minimize noise. The filter breakpoints are set to produce an end-to-end bandwidth of about 50 Hz to 610 Hz, and filter component values are chosen so that noise from resistors and amplifier bias currents do not exceed input noise levels from previous stages. The circuit schematics for the coil drive, low-noise amplifier, downconverting mixer, and filter chain are reprinted here in Figures 6-6, 6-7, 6-8, and 6-9, respectively. Component values for these circuits are listed in Table 6.4.

Voltage rails of ± 15 V for analog circuitry and $+5$ V for digital circuitry are provided by a BK Precision 1651 laboratory power supply. The coil drive is powered by a 1.5V D-cell battery, to eliminate any power supply contribution to noise measurements.

For fully exhaustive schematics, including schematics of all digital circuitry and component selections, the reader is referred to Appendix D.

For the measurements the follow in Section 6.2, the coil drive was configured to operate at 21 kHz with a coil drive to mixer reference phase shift of 275°, set automatically by the algorithm described in Section 4.4.2.

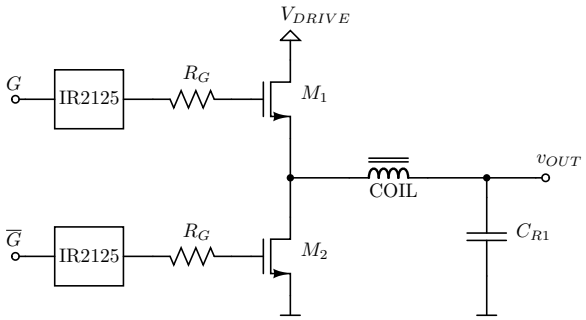


Figure 6-6: Coil drive circuit used in the experimental setup.

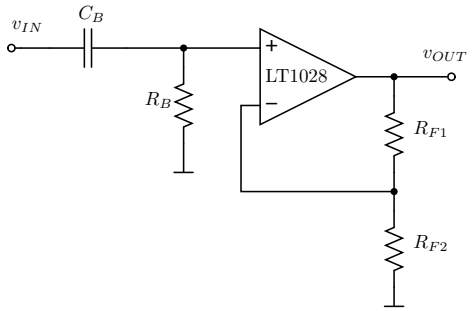


Figure 6-7: Low-noise amplifier front-end used in the experimental setup.

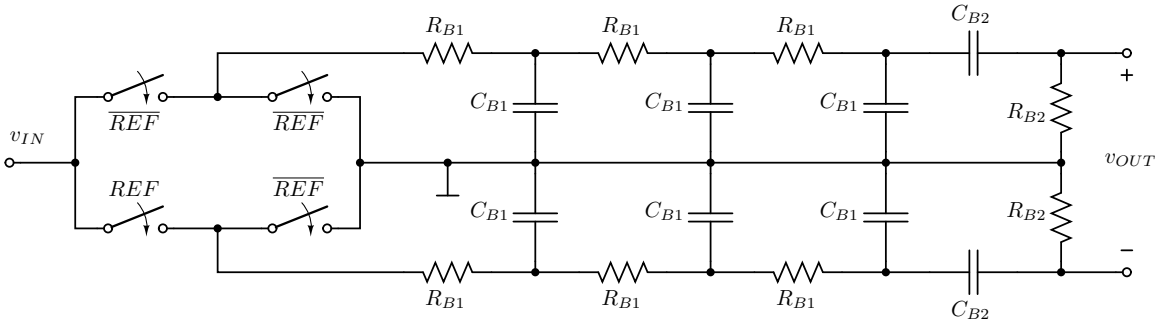


Figure 6-8: Downconverting mixer and band-pass filter used in the experimental setup.

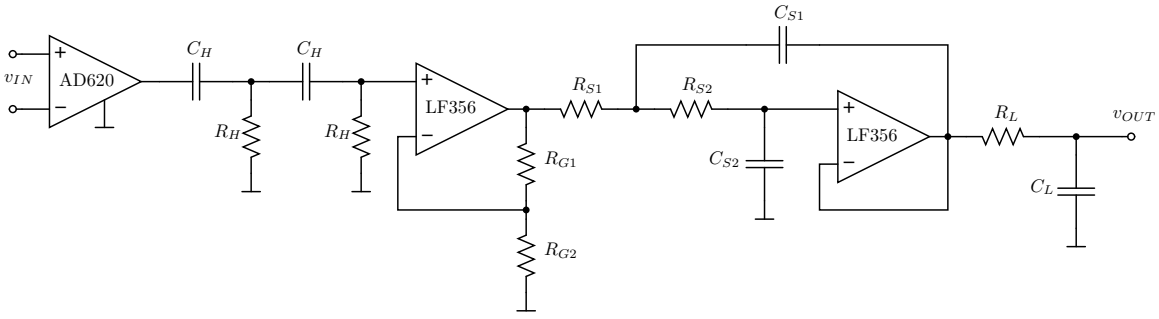


Figure 6-9: Filter chain used in the experimental setup.

Coil Drive Components	
Component	Value
R_G	$10\,\Omega$
M_1,M_2	IRF530V
FET Drivers	IR2125 [17]
Coil and C_{R1}	See Table 6.3

LNA Components	
Component	Value
C_B	$22\,\mu$F
R_B	$1.3\,\text{k}\Omega$
R_{F1}	$1.1\,\text{k}\Omega$
R_{F2}	$330\,\Omega$
Op-amp	LT1028 [21]

Mixer and BPF Components	
Component	Value
R_{B1}	$5.1\,\text{k}\Omega$
R_{B2}	$100\,\text{k}\Omega$
C_{B1}	$0.01\,\mu$F
C_{B2}	$1.0\,\mu$F
Analog Switches	ADG211A [2]

Filter Chain Components	
Component	Value
R_H	$10\,\text{k}\Omega$
C_H	$1.0\,\mu$F
R_{G1}	$1.3\,\text{k}\Omega$
R_{G2}	$300\,\Omega$
R_{S1}	$22\,\text{k}\Omega$
R_{S2}	$22\,\text{k}\Omega$
C_{S1}	$0.01\,\mu$F
C_{S2}	$0.01\,\mu$F
R_L	$22\,\text{k}\Omega$
C_L	$0.01\,\mu$F
Inst. Amp	AD620 [3]
Inst. Amp Gain	77 ($R_G = 650\,\Omega$)
Op-Amps	LF356 [26]

Table 6.4: Component values selected for signal conditioning circuitry and coil drive in the experimental setup.

6.2 System Measurements and Specifications

6.2.1 Demonstration

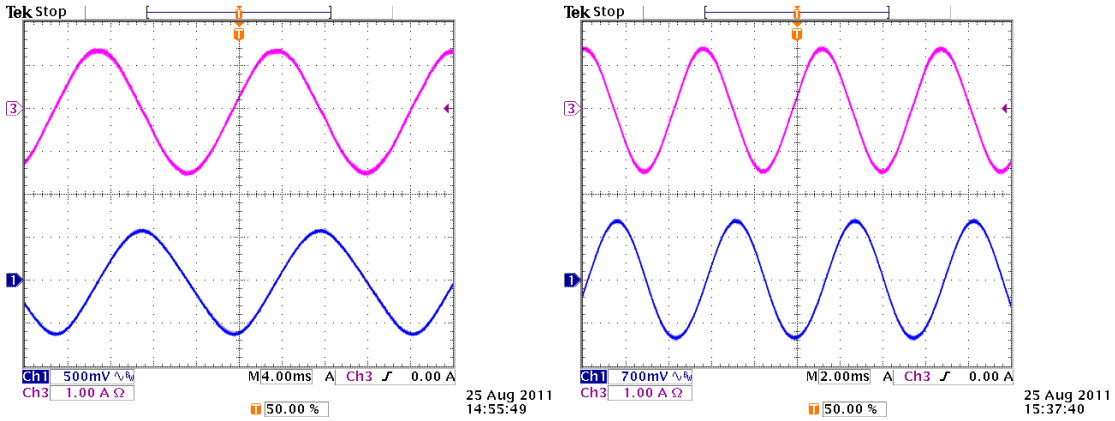
Experimental results from the prototype sensor demonstrating reconstruction of currents in the circuit breaker panel are shown in Figures 6-10 through 6-14. These waveforms are captured directly from the output of the signal conditioning circuitry, before digital processing.

Figure 6-10 shows several reconstructed sinusoidal test currents alongside the original currents as measured by a Tektronix TCP202 current probe. As we reduce the test current in the breaker, we find that at this level of pickup amplifier gain (34.4, $R_G = 6.8\,\mathrm{k}\Omega$), our minimum detectable signal is limited by interference from 60 Hz magnetic fields originating from sources outside the circuit breaker box. The 60 Hz and 180 Hz 1 A RMS test currents shown appear largely unaffected by this interference, while it becomes more noticable in the 60 Hz 500 mA RMS and 100 mA RMS currents. The interference can be eliminated from the measurement by triggering the oscilloscope from a 61 Hz test current and averaging out the interference over many sample periods, as demonstrated in Figure 6-11.

The 60 Hz component of the unwanted external interference produces a voltage on the current-sense pickup that is roughly equivalent to that which would be produced by 20 mA RMS of current in the circuit breaker. Figure 6-12 shows the interference by itself, measured at the analog system output, when no current is running through the breaker. Figure 6-13 demonstrates perfectly constructive and destructive interference between a 60 Hz 20 mA RMS current in the circuit breaker and the 60 Hz component of the interfering signal.

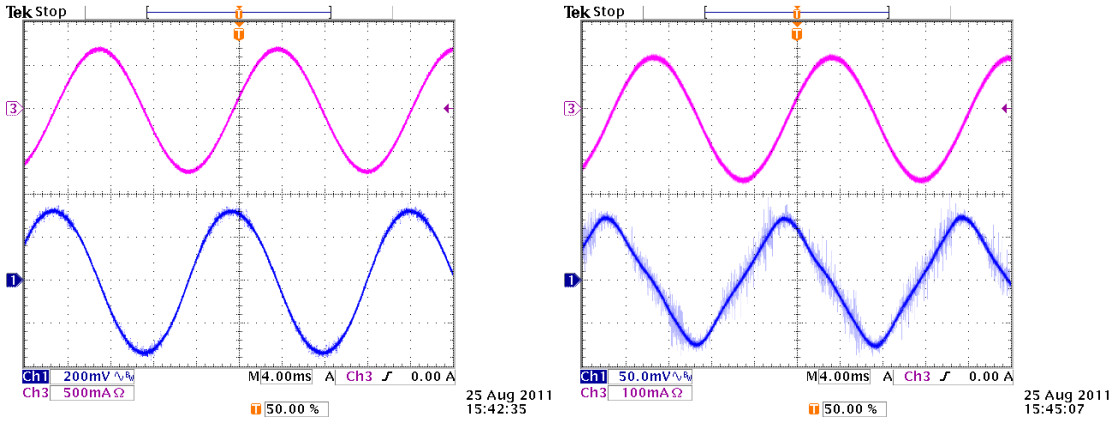
The programmable power source was used to demonstrate the system response to step transients. Figure 6-14 shows a reconstructed series of step transients from 0 mA RMS to 250 mA RMS and then to 500 mA RMS, all at 60 Hz. These are measured at the same analog system output as the previous measurements, and are shown alongside the original currents measured with a current probe.

The sample ATX power supply was used to power a emachines W3609 computer



(a) 60 Hz, 1 A RMS

(b) 180 Hz, 1 A RMS



(c) 60 Hz, 500 mA RMS

(d) 60 Hz, 100 mA RMS

Figure 6-10: Reconstructed (bottom) and original (top) test current signals.

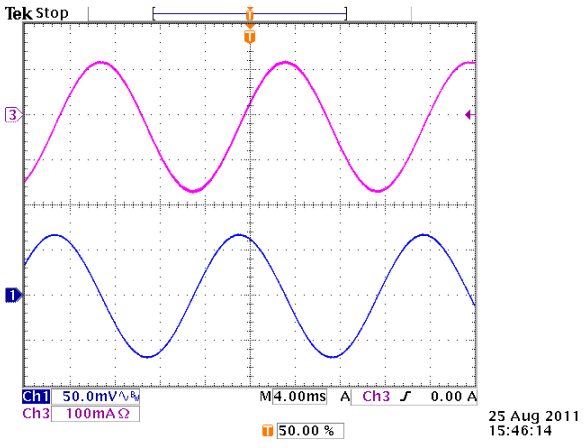


Figure 6-11: 61 Hz, 100 mA RMS test current, averaged over 512 cycles to remove interference.

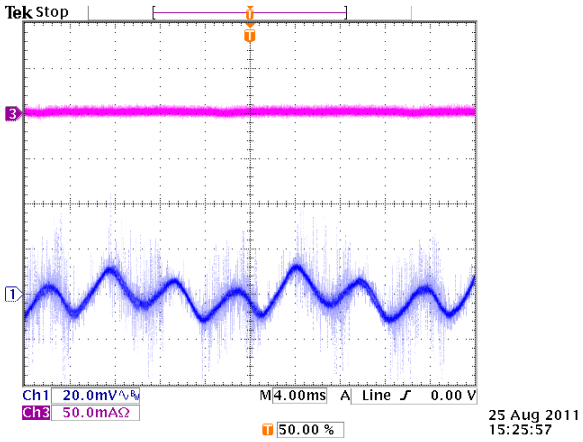
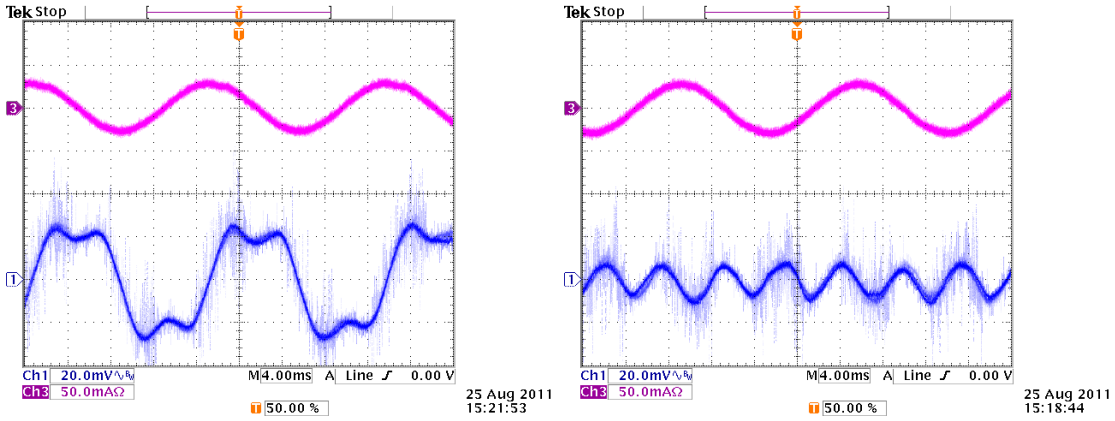


Figure 6-12: Interference signal at sensor output (bottom).



(a) Constructive Interference (b) Destructive Interference

Figure 6-13: Constructive and destructive interference between a 20 mA RMS, 60 Hz test current and unwanted signals on the current-sense pickup of origin outside the circuit breaker panel.

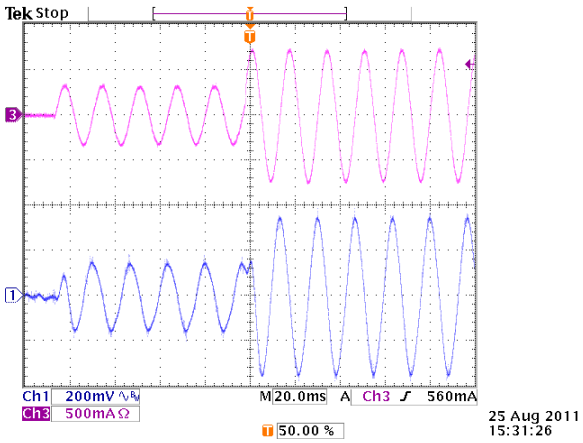


Figure 6-14: A 60 Hz step-transient test current (top) and reconstruction (bottom).

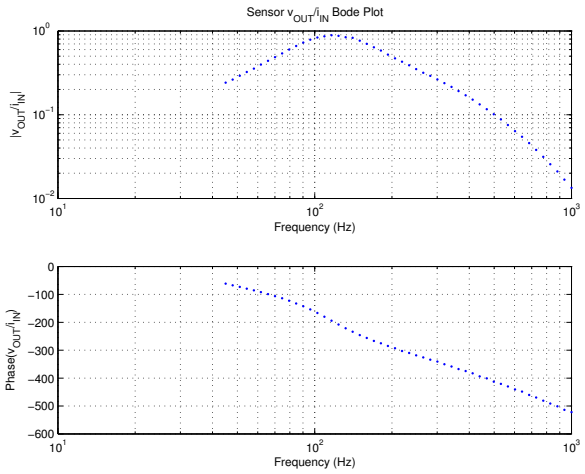


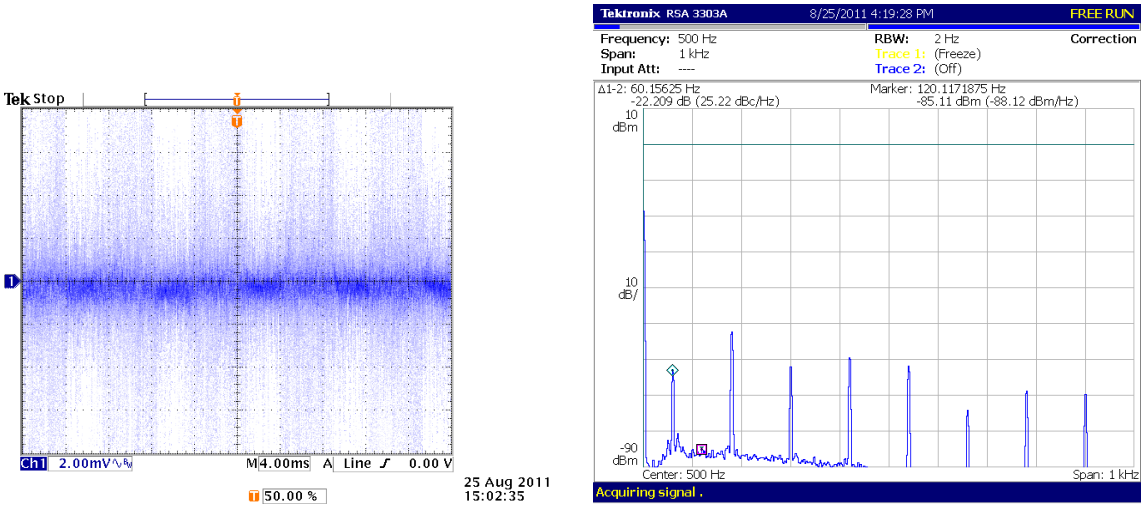
Figure 6-15: Frequency response of the experimental sensor prototype.

to produce a test current with higher harmonic content. The harmonic content of the ATX supply current, consisting primarily of odd harmonics of 60 Hz, is typical for an unfiltered or lightly filtered full-bridge rectifier at the front-end of many AC-DC power supplies. For experiments using the sample ATX power supply, the circuit breaker power source was connected to utility voltage. In Section 5.2 this test current is processed by a MATLAB®-based implementation of a digital frequency response compensator, using the experimental setup described here.

6.2.2 Specifications

Frequency Response

The frequency response of the sensor is measured by running a 1 A RMS current through a circuit breaker and measuring the magnitude and phase difference between voltage signals sensed at the analog sensor output and the original current measured at the load. Fifty data points were taken at log-scale frequencies from 45 Hz to 1 kHz, and are plotted in Figure 6-15. This data is used to design the digital filter that flattens the frequency response of the system.



(a) Time-Domain Output Noise

(b) Noise Spectrum

Figure 6-16: Sensor output noise with coil drive power disconnected.

Noise

We measure the total noise contribution of the signal conditioning electronics and inductive link by disconnecting the power from the coil drive. In this configuration the input to the low-noise amplifier at the front end of the signal processing chain is effectively shorted by the resonant capacitor of the outer-door resonator over our frequencies of interest (around 20 kHz). We measure total output noise at roughly 2 mV peak-to-peak, which corresponds to about 330 μV RMS noise. An oscilloscope capture of the output noise, triggered on the 60 Hz AC line voltage, is shown in Figure 6-16 alongside a corresponding spectrum.

When the coil drive is activated, clock instability raises the noise floor by about 20 dBm. We take this measurement by reconnecting the coil drive power and shorting the terminals of the current-sense pickup at the input to the pickup amplifier. A spectrum of the noise floor with the coil drive engaged is shown in Figure 6-17. This noise floor is the one that limits the minimum detectable signal of the sensor, if the pickup amplifier gain is sufficiently low so that external magnetic interference is not a problem.

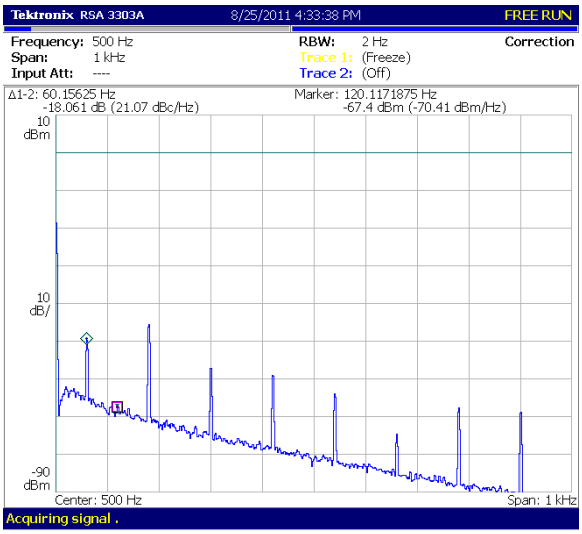


Figure 6-17: Sensor output noise spectrum with coil drive power engaged.

Distortion

Distortion measurements of the entire sensor are difficult to make because the programmable power source in the experimental setup, the HP 6834B, produces currents that are often already distorted beyond the amount of distortion expected from the sensor. Figure 6-18 shows the spectrum of the voltage across a 2Ω load resistor driven with a 500 mA RMS 60 Hz current by the power source. The spectrum contains a significant third harmonic component, and already has a total harmonic distortion of 0. Figure 6-19 shows spectra of the voltage across the current-sense pickup and the corresponding reconstructed signal at the analog output of the sensor. The increase in third harmonic power with respect to fundamental power in both of these spectra is very small, although some second-harmonic content is added.

To obtain more precise measurements of distortion, which is mainly caused by the nonlinear behavior of the JFET modulator circuit and inductive through-door link, the current-sense pickup is removed, and replaced with an Agilent O function generator at the input to the pickup amplifer. For the following measurements, the gain of the pickup amplifier is reduced to 5 ($R_G = \infty$) so that inputs within the output range of the function generator do not saturated the JFET modulator.

Figure 6-21 shows sensor output spectra for various input levels of the function

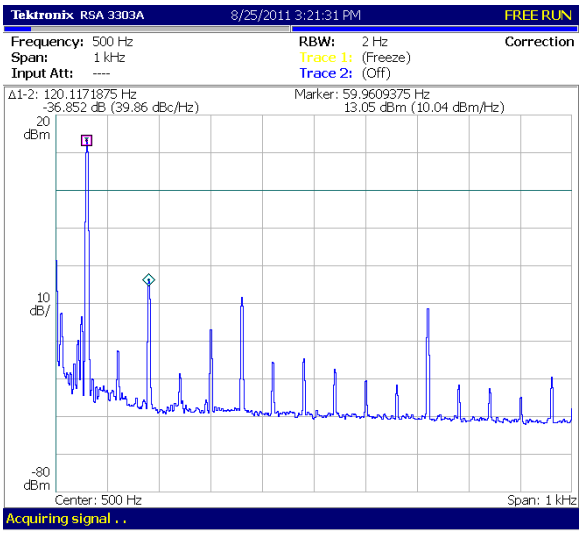
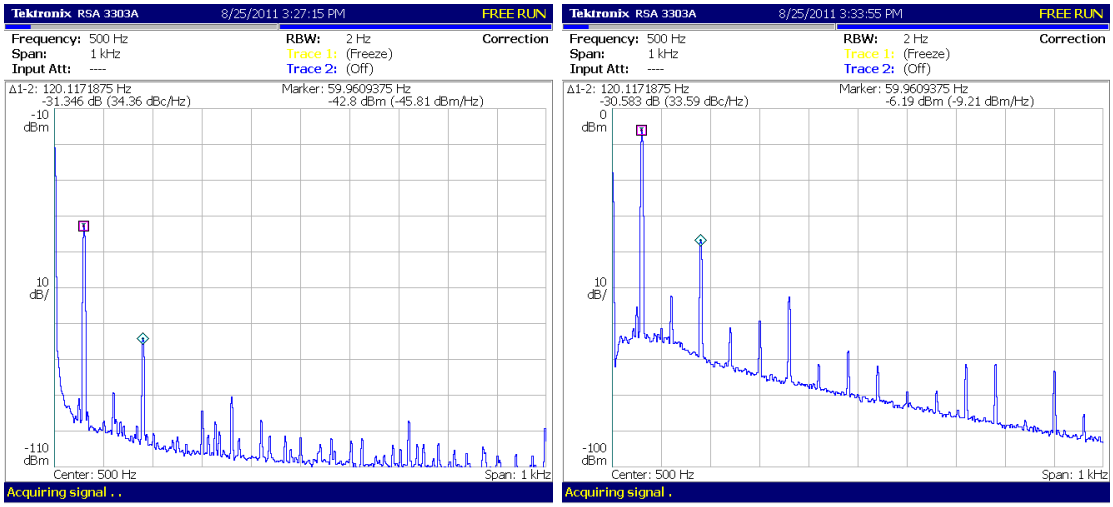


Figure 6-18: Spectrum of voltage across 2 Ω load resistor corresponding to a 500 mA test current sourced by the HP power source.



(a) Current-Sense Pickup (b) Sensor Analog Output

Figure 6-19: Spectra of current-sense pickup and sensor output voltages corresponding to a 500 mA test current sourced by the HP power source.

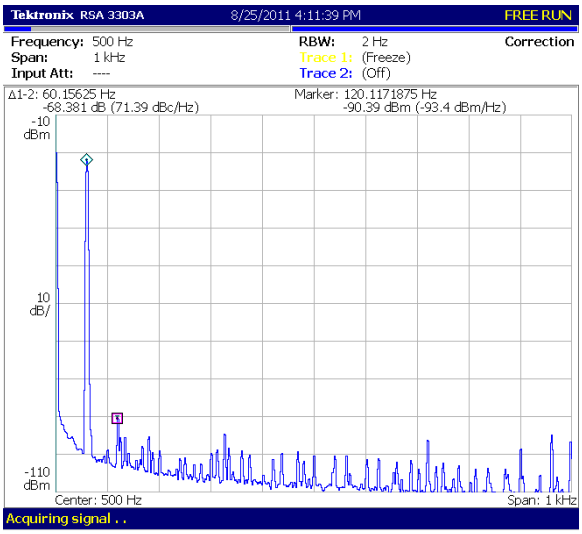


Figure 6-20: Spectrum of 55 mV peak-to-peak test voltage from the function generator.

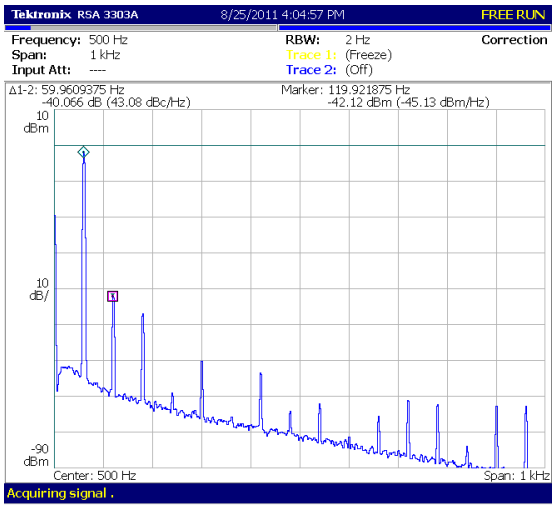
generator. The input spectrum at 55 mV peak-to-peak, shown in Figure 6-20, is very pure. As the input magnitude increases, so does distortion at the output. Our metric for distortion is *Total Harmonic Distortion* (THD), given by:

$$\text{THD} = \frac{\sum_{n=2}^{\infty} P_{n\cdot 60\text{Hz}}}{P_{60\text{Hz}}} \tag{6.1}$$

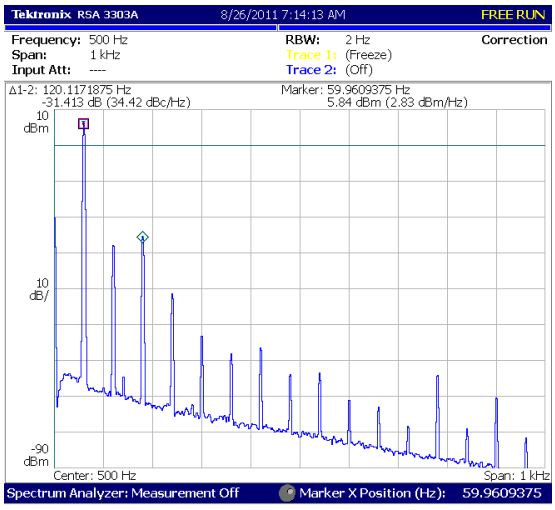
where P_f is the signal power at a given frequency f. Figure 6-21 shows spectra at signal levels where total harmonic distortion is approximately 0.01%, 0.1%, and 1.0%. Power levels at the individual 60 Hz harmonics from these spectra are given in Table 6.5.

Resolution

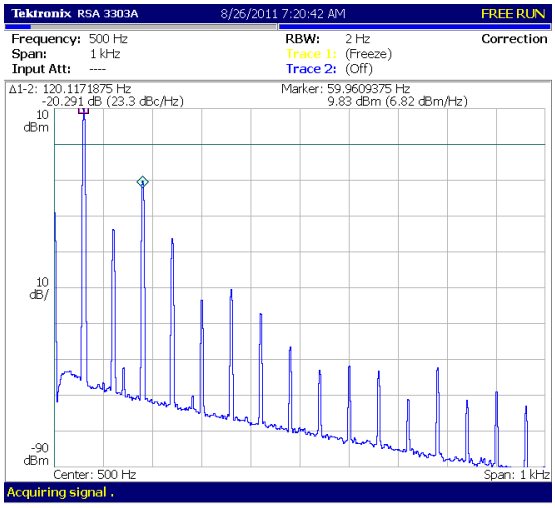
The power of the noise floor near 60 Hz, shown in Figure 6-17, is approximately -65dBm. The power of the 60 Hz pickup in the same figure is approximately -50dBm. We can define the resolution of the sensor with respect to either of these two figures as the ratio of the power level of the fundamental component of our maximum-amplitude test signal at the output of the sensor to the power of the limiting signal (be it noise or interference). Measured resolution specifications calculated from the spectra in



(a) ≈ 0.01% THD



(b) ≈ 0.10% THD



(c) ≈ 1.00% THD

Figure 6-21: Sensor output spectra at various function generator input levels.

Sensor Output Harmonic Powers, THD, and Resolution			
Harmonic	Spectrum 6-21a	Spectrum 6-21b	Spectrum 6-21c
60 Hz	−2.05 dBm	5.84 dBm	9.81 dBm
120 Hz	−42.12 dBm	−27.95 dBm	−23.77 dBm
180 Hz	−46.95 dBm	−25.57 dBm	−10.46 dBm
240 Hz	−68.97 dBm	−41.40 dBm	−26.30 dBm
300 Hz	−69.12 dBm	−53.15 dBm	−43.41 dBm
360 Hz	−75.62 dBm	−58.04 dBm	−40.48 dBm
420 Hz	−63.46 dBm	−56.49 dBm	−47.20 dBm
480 Hz	−74.16 dBm	−63.87 dBm	−56.56 dBm
540 Hz	−71.95 dBm	−63.55 dBm	−62.90 dBm
600 Hz	−81.19 dBm	−71.01 dBm	−61.86 dBm
THD	0.013%	0.116%	1.010%

Table 6.5: Table of harmonic powers at the sensor analog output under three separate drive levels whose spectra are shown in Figure 6-21. For each drive level, we calculate the THD according to the formula in Equation 6.1.

Sensor Resolution for Given Maximum THD		
Maximum THD	Resolution to 60 Hz Interference	Resolution to Noise Floor
0.013%	7.85 bits	10.18 bits
0.116%	9.16 bits	11.49 bits
1.010%	9.83 bits	12.15 bits

Table 6.6: 60 Hz Sensor resolution for various maximum THD levels. Resolution is calculated as a ratio of signal power to external 60 Hz interference power and as ratio of signal power to noise power.

Figures 6-21 are given in Table 6.6. The table demonstrates that we can achieve a resolution of approximately 8 bits while maintaining a THD of only 0.01%. Linearity can be traded for resolution, but such a trade-off has diminishing returns: we gain one bit of resolution at a maximum THD of 0.1%, but see a smaller improvement when increasing the maximum tolerable THD to 1.0%.

Chapter 7

Conclusion

Research demonstrates that given the tools to directly monitor their energy consumption, consumers will respond by adjusting their use patterns. "Smart" metering of consumption information disaggregated by end-use has the potential to significantly alter the way in which consumers understand their use patterns, revealing where inefficiencies exist on an appliance-by-appliance basis. However, the availability of appropriate sensing and information delivery systems remains a chief bottleneck in many situations. Metering hardware and access to metered information will likely limit the implementation of new electric energy conservation strategies in the near future.

This thesis proposes an alternative to traditional clamp or Hall-effect current sensors that aims to reduce the financial and technical barriers-to-entry limiting the proliferation of electricity metering disaggregated by end-use. This alternative measures current in the utility feed by sensing the resulting magnetic field at the face of a circuit breaker in a standard breaker panel. The sensor requires no skilled installation, and can be interrogated through the steel panel door with no direct electrical contact, permitting the door to remain closed to comply with safety regulations.

The proposed sensor could be a "silver bullet" for many power monitoring and control problems. The sensor is as easy to install in a retrofit situation as in new work. This approach could make it easy to provide essential, comprehensible information about opportunities and the success of efforts for energy conservation.

7.1 Thesis Summary

Chapter 2 discussed the mechanics of detecting the current through a circuit breaker without the use of a wrap-around sensor. A inductive pickup capable of sensing current at the breaker face was presented in combination with two designs for an amplification stage. The current-sense pickup and pickup amplifer can be implemented independently in situations where the panel door does not need to be closed or does not exist (such as in a secondary breaker panel). Chapter 2 also presented a passive, balanced, adaptively-referencing JFET modulator circuit capable of up-modulating the sensed current signal to a carrier frequency sufficiently high for through-door transmission. The modulator circuit performs continous modulation of its impedance proportional to the sensed current signal, and does not require a DC power supply.

Chapter 3 presented an inductive through-door link capable of transmitting information through a thin piece of steel by impedance modulation. Analytical modelling demonstrated that the performance of the link is closely related to the quality factors Q of the coupled resonators on either side of the steel door, as well as the coupling coefficient k between them. Motivated by these results, the chapter discusses ways to maximize Q through thoughtful coil design, and to increase k by saturating the steel, focusing magnetic flux from permanent magnets laterally through the door.

Chapter 4 discussed the circuitry necessary to operate the inductive through-door link and reconstruct the sensed current signal outside the breaker panel. The outer coil of the link is driven with a half-bridge circuit at carrier frequency. The function of signal conditioning electronics amounts to demodulation of an amplitude-modulated signal with very low modulation depth at a known carrier frequency. Noise is avoided by introducing substantial gain at a low-noise front-end amplifier, reducing the effective thermal noise contribution of later active stages. Numerous filter circuits limit the sensed signal to the bandwidth of interest, further limiting noise. Phase matching between the amplitude-modulated carrier and the reference carrier at the downconverting mixer is achieved digitally with a hill-climbing algorithm that use the DC level of the downmodulated unsurpressed carrier as a heuristic.

Chapter 5 presented an example implementation of a digital compensator that inverts the non-uniform frequency response of the analog sensor electronics. The compensator algorithm capitalizes on the assumption that all frequency content in the sensed signal is concentrated at or near the harmonics of 60 Hz by extracting individual harmonics and independently applying the appropriate magnitude and phase changes to each. The algorithm was successfully tested on a current signal generated by an ATX AC-DC power supply.

Chpater 6 describes an experimental prototype of the sensor system, including all the components described in Chapters 2-5. The prototype is implemented on a standard circuit breaker panel that is configured to use test currents from a both laboratory power source and the utility line. Measurements demonstrated that the sensor is capable of discenring current signals at a resolution of approximately 8 bits at a total harmonic distortion of 0.01%. The minimum detectable current was found to be limited to 20 mA RMS by interference from 60 Hz magnetic fields originating from sources outside the circuit breaker panel.

7.2 Future Work

7.2.1 Miniaturization

The development of a miniaturization of signal conditioning electronics in the experimental sensor prototype described in Chapter 6 is in progress. Schematics of the revision are given in Appendix D and PCB layout is underway.

A miniaturization of the current sensing electronics at the breaker face has already been developed as a single printed circuit board (PCB) that holds the current-sense pickup, pickup amplifier, batteries, and the JFET modulator circuit. The PCB is small enough to fit gracefully over a single 20 A circuit breaker unit. A photo of the miniaturization is shown in Figure 7-1. An additional miniaturization was constructed using the transformer-based pickup amplifier discussed in Section 2.3.1. Future revisions of this PCB may be implemented as standalone sensors for application in

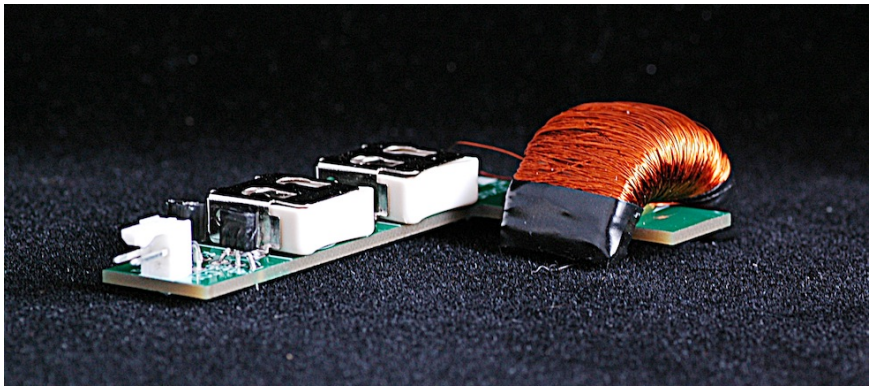


Figure 7-1: PCB containing the current-sense pickup, amplifier stage, and JFET modulator circuit.

diagnostic applications where the break panel door need not remain closed, but non-instrusive current measurements are necessary. Schematics and PCB layouts for both miniaturizations are also provided in Appendix D.

7.2.2 Full-Band Frequency Response Compensation

The functionality of the sensor can be increased if an digital frequency response compensator is designed to function at all frequencies within the sensor bandwidth, and not just the harmonics of 60 Hz. This would allow the sensor to perfectly reconstruct non-periodic signals and transients with non-harmonic frequency components, enhancing its ability to identify loads on a circuit. Construction of such a compensator is more difficult than the compensator presented in Chapter 5 because the transfer function of the analog sensor electronics is of high order.

7.2.3 Alternatives to the Inductive Through-Door Link

This thesis presents an inductive link as a means to transmit information from the current-sensing electronics through the steel door of the circuit breaker panel. Other alternatives that could be explored include thermal and ultrasonic transmitters and receivers, which have been previously used to achieve communication through steel []. If these alternatives are found to exhibit superior performance to the inductive link, the gain of the signal processing chain could be reduced, relaxing noise constraints.

Furthermore, thermal and ultrasonic systems could be used for through-door power transmission as an alternative to battery power for the pickup amplifier circuit.

Appendix A

Application Notes

A.1 Circuit Breaker Panel Configuration

The circuit breaker panel in the experimental setup is configured exactly as a normal main circuit breaker would be in a real setting, except for three differences:

- Neutral is not connected to earth inside the breaker box.
- The main line entering the breaker panel is single-phase.
- The main line entering the breaker panel is switched and fused.

A photo of the inside of the breaker box is shown in Figure A-1. The box is a QO Series Main Box, McMaster-Carr Part Number 6790K51. It is a standard breaker box that would be commonly be used for 120V/240V service inside a home. A main breaker for both 120V phases is at the top, with power rails for each phase on the left and right below. A bus bar in a "π" shape is connected to neutral for all circuits. A screw at the top center of the neutral bus bar normally connects the bus bar to the enclosure, earthing the enclosure. In our setup we do not include this screw because we are not connecting neutral and earth in the box. Instead earth is connected to a separate bus bar on the left-hand side of the box, which is connected directly to the enclosure, isolated from the neutral bus bar.

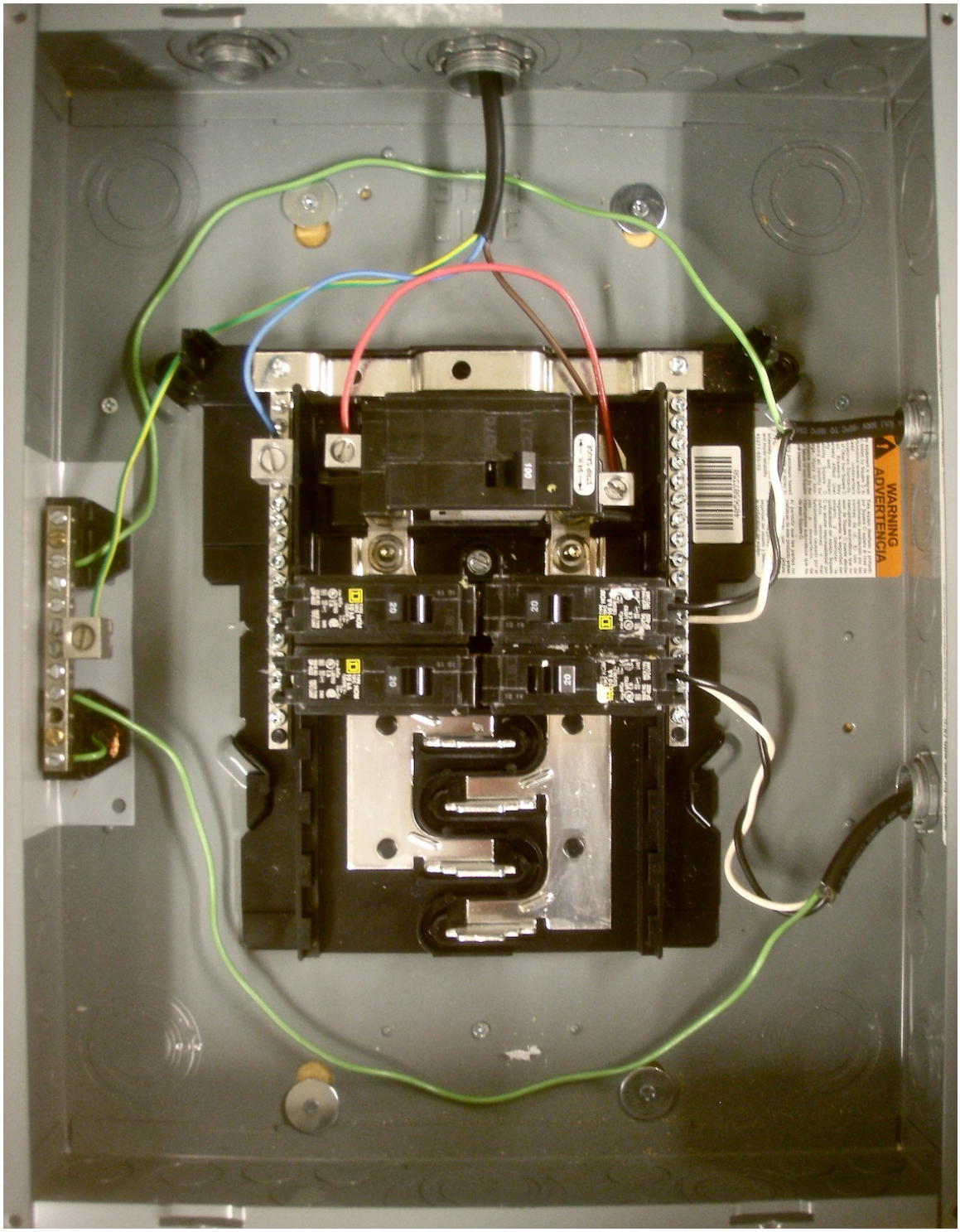


Figure A-1: Inside of the circuit breaker panel used in the experimental setup.

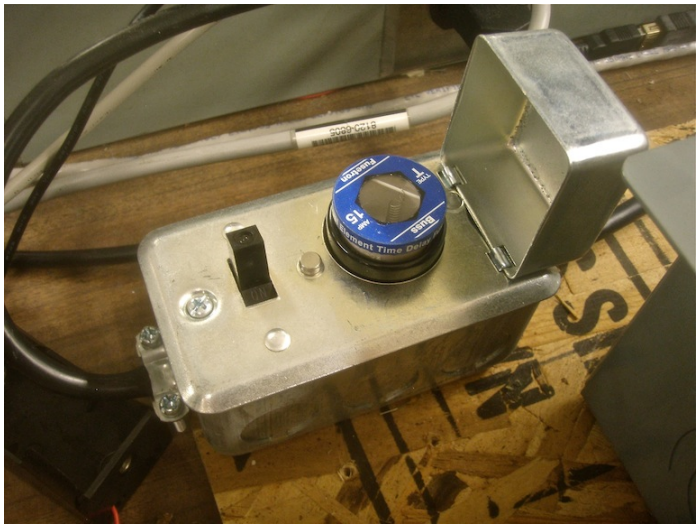


Figure A-2: Power entrance to the circuit breaker box.

The main power entrance to the box is shown in Figure A-2. It has a standard U.S. 120V wall plug connector. The wall plug connector can be connected to a three-phase phase breakout box for use with the HP 6834B power source, as well as directly to utility voltage for testing realistic loads. The power entrance is switched and has an edison-socket 15A fuse. Once inside the breaker panel, line conductor is connected to both of the two phase rails, while neutral is connected to the main neutral bus-bar and earth is connected to the special earth bus-bar on the left-hand side of the box. Four 20 A Square D QO Series breaker units are installed (McMaster-Carr Part Number 6782K11). The two rightmost breakers are currently in use. Each is connected to a separate phase rail. The upper breaker is connected to the upper outlet box in the experimental setup, while the lower breaker is connected to the lower outlet box.

Conductor designations inside the breaker are represented by the following colors:

- Line: Brown, Red, Black
- Neutral: Blue, White
- Earth: Green

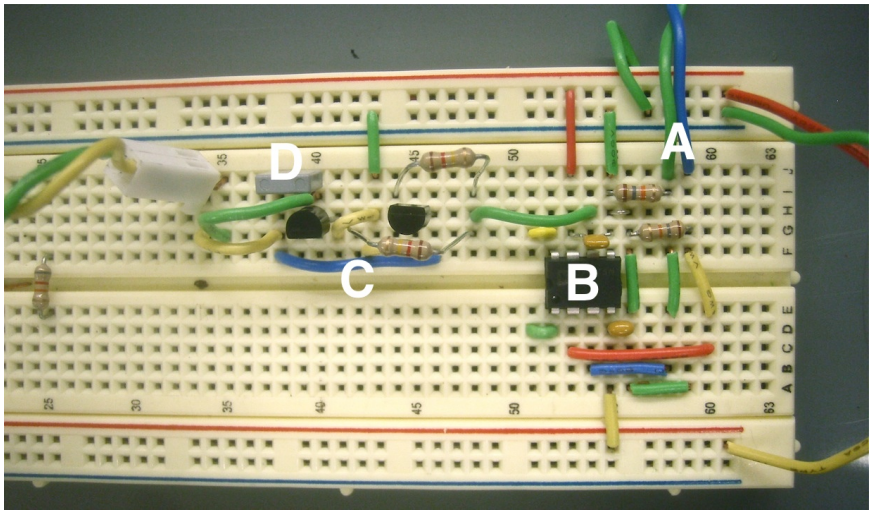


Figure A-3: Breadboard with in-panel current sensing electronics.

A.2 In-Panel Electronics

The current-sense pickup should be positioned on the face of a circuit breaker roughly half-way between the switch and the bottom edge of the breaker. It should be positioned such that the direction of the turns of wire on the pickup is parallel with the length of the breaker. The two leads from the pickup should be connected to the input terminals of the pickup amplifier in use. The inner coil of the through-door link should be connected to the JFET source/drain terminals of the JFET impedance modulator circuit.

The breadboard with the in-panel electronics used in the experimental setup is shown and labeled in Figure A-3. (A) is the current-sense pickup connection point, (B) is the AD627 instrumentation amplifier which is connected to the JFET modulator circuit (C) through gate resistors. (D) is the resonant capacitor of the inner resonator of the through-door link.

The PCB with the in-panel electronics (discussed in the Setion 7.2.1 but not used in the experimental setup) is shown in Figure A-4. Two SR44 silver-oxide battery cells are mounted on the top of the board, along with the current-sense pickup (with glue) and the discrete PN4117A JFETs. The amplifier electronics are surface-mount components on the bottom side of the board. The "COIL" molex connector should be connected to the inner-door coil, while the "PICKUP" molex connector is

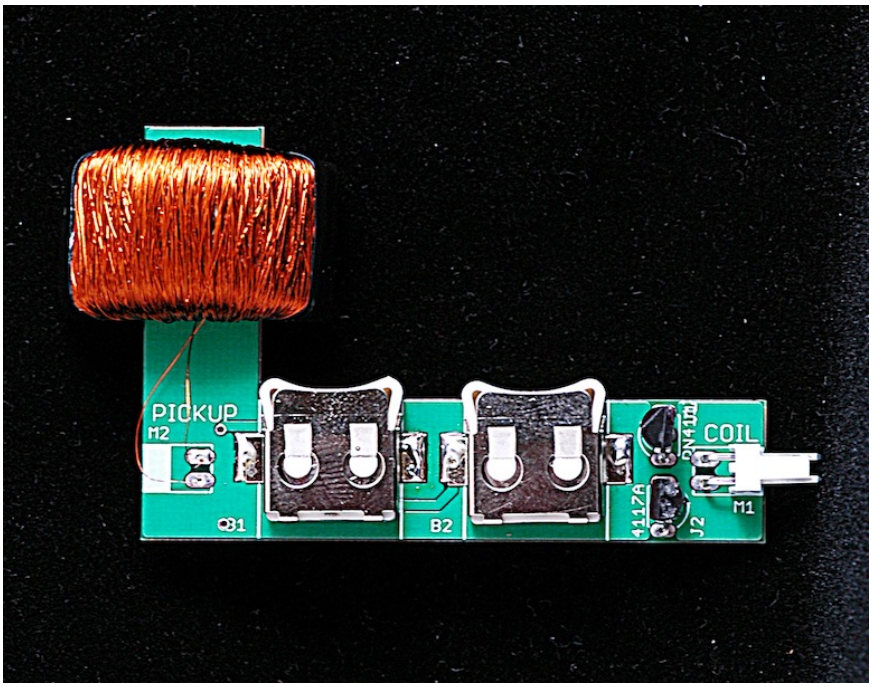


Figure A-4: PCB with in-panel current sensing electronics.

optional. If the pickup is mounted on this PCB, its leads can be soldered directly to the "PICKUP" pads. If not, the molex connector can be used. It is important to be delicate when inserting and removing the SR44 batteries, as it is possible to tear off the surface-mount solder pads with which their holders are attached to the PCB. Often the solder pad directly beneath the battery holder requires a bump of solder to properly make contact with the negative terminal of the inserted battery.

A.3 Through-Door Link Coils

The through-door coil mounting brackets are secured to the panel door with hot glue. If the hot glue begins to unstick, simply add a little more and apply pressure for a couple minutes. The coils can be inserted carefully into the bracket by sliding from the side. When inserting the coils, make sure that the magnets at their cores are aligned so that poles oppose one another - otherwise, they will become very difficult to remove from the steel because of their strong attraction forces. Once the coils are in place, they can be secured with three 6-32 nylon machine screws.

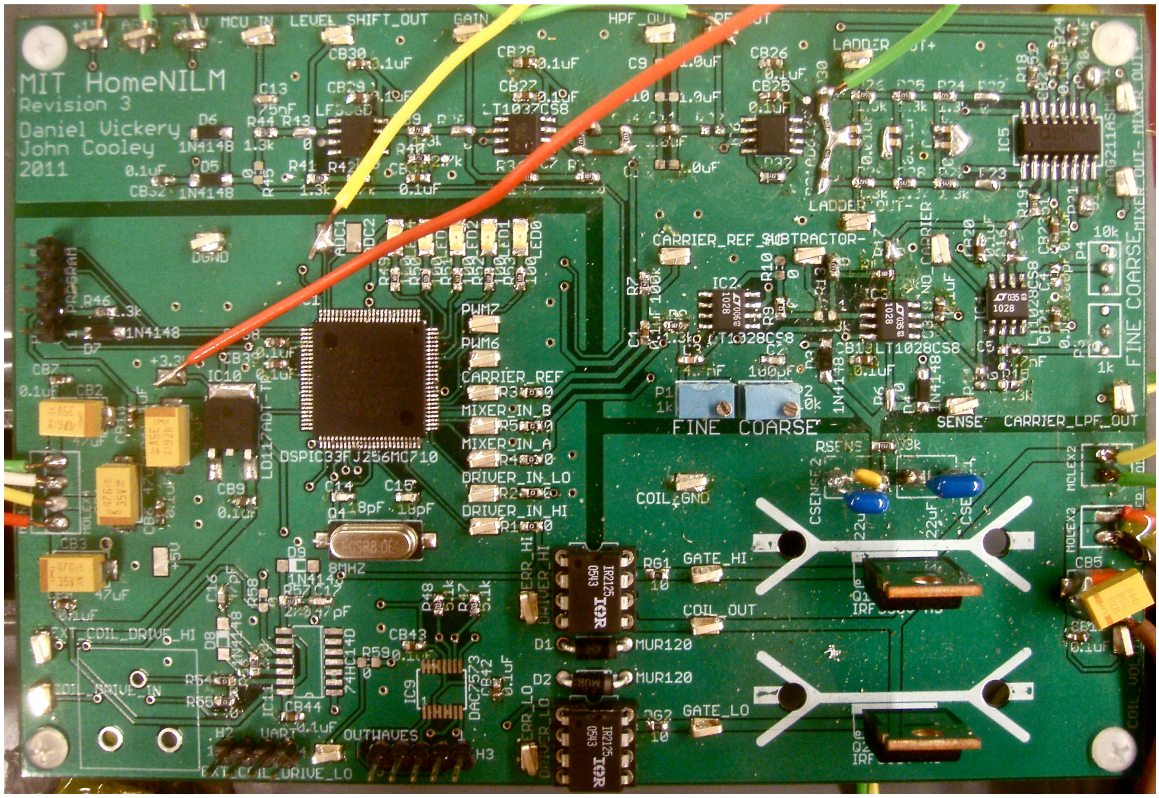


Figure A-5: PCB with coil drive and signal conditioning electronics.

A.4 Signal Conditioning PCB

A.4.1 Overview and Setup

A photo of the PCB containing the signal conditioning electronics and coil drive is shown in Figure A-5. To run the board, power should be connected to the molex connector labeled "MAIN_POWER" (far left). The convention with all molex connectors on the board is that the locking tab on the female connector should be facing towards the outer edge of board to which the male connector is adjacent. Power required is ±15 V, 5 V, and common. The ±15 V rail is used for the analog electronics and can be increased to an absolute maximum of ±18 V. The 5 V rail is used for the digital electronics, which all run at 3.3 V, regulated from 5 V by an IC on the board. Currently, no devices use the 5 V rail directly.

The outer coil of the through-door link should be connected to the molex terminal labeled "COIL" (far right). The DC voltage for the coil drive circuit is connected

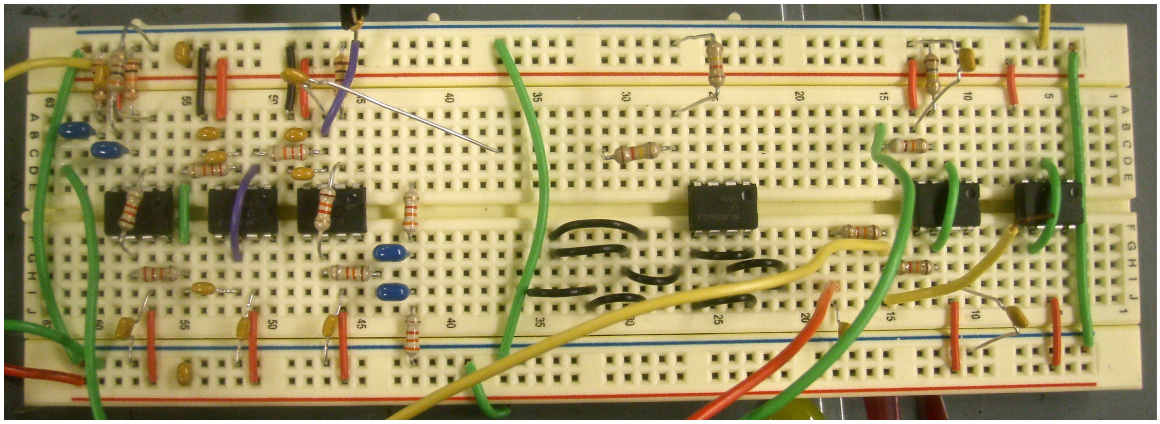


Figure A-6: Breadboard with additional signal conditioning electronics.

to the molex terminal directly below labeled "COIL_POWER". Once the through-door coil and two power connectors are connected and turned on, the circuit will be operating.

The adjacent breadboard with additional circuitry shown in the experimental setup is shown in detail in Figure A-6. The left of this breadboard contains several LF356 op-amp circuits that form the filter chain that follows the AD620 instrumentation amplifier in the signal conditioning circuitry. The right side of this breadboard contains an LF356 op-amp level-shifter that shifts and scales the DC output level of the differential low-pass filter for analog-to-digital conversion. Note that if the coil drive DC power level is change from its current nominal level of 1.5 V, the scale factor of this level shifter will need to change proportionally.

Oscilloscope measurements in Chapter 6 were taken at the node where the scope probe is connected in Figure A-6.

A.4.2 Programming the dsPIC33FJ256MC710

The standard method of programming the dsPIC33FJ256MC710 microcontroller requires Microchip's MPLAB software, which runs exclusively on modern Windows platforms (although beta versions exist for Mac OS X and GNU/Linux). With MPLAB and the proper USB drivers for the MPLAB ICD2 programmer puck installed, the programming procedure is as follows:

1. Connect the ICD2 programmer puck to the PC USB port.
2. Connect the programmer dongle (molex) to the five-pin programming header on the PCB labeled "UART".
3. Open MPLAB and the source code file or hex file.
4. Under the "Programmer" menu, go to "Programmer" and select MPLAB ICD2.
5. Under the "Configure" menu, click "Select Device..." and select the dsPIC33FJ256MC710.
6. If necessary, click the "BUILD" button to compile the code to generate a .hex file from the .c file. This .hex file is what is actually copied into the program memory of the PIC.
7. Under the "Programmer" menu, click "Connect to Programmer"
8. Under the "Programmer" menu, click "Program"
9. You're Done!

A.4.3 Microprocessor Control

The user can interface with the on-board microprocessor over a serial UART to adjust the carrier frequency, mixer referece carrier phase offset, and coil drive switching dead-time. The user can also command the microprocessor to run the automatic phase calibration algorithm. A Python program called homenilm_ctl.py was written to provide an interface for commanding the microprocessor. The program requires the pySerial Python library. Once the user's computer is properly connected to the UART, the program can be run with:

```
python ./homenilm_ctl.py /path/to/serial/device
```

The program will print explicit instructions for its use onscreen when launched.

In our experimental setup, the computer is connected to the microprocessor UART using a SparkFun USB to RS232 adapter, shown in Figure A-7. The pinout of the

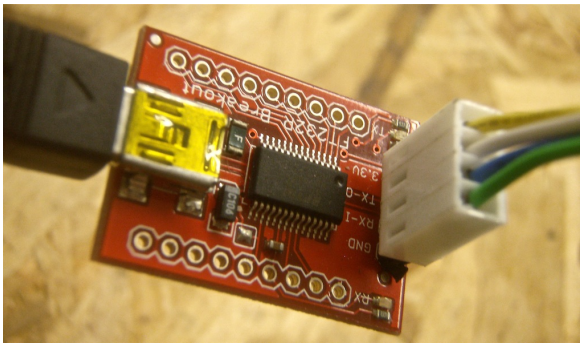


Figure A-7: SparkFun USB to RS232 adapter.

SparkFun adapter does not match the pinout of the connector onboard, so a special connector is used. A standard serial port can be used in place of USB, but a 3.3V level-shifter such as the Maxim MAX232 IC must be used.

Appendix B

Design and Construction Notes

B.1 Current-Sense Pickup Construction

The inductive current-sense pickup is formed from a half-toroid of high permeability ferrite material such as 3E6 (used in our experimental setup).

The half-toroid is formed from a full toroid, which can be halved with a lubricated band saw, such as the one in 10-012. When halving toroids, I simply "eyeballed" what looked to be about the center of the toroid.

If the toroid is not sufficiently wide enough, two or more can be combined to increase the cross-sectional area. The two halves can be glued together with hot glue. When combining toroids, a clamp should be used to ensure a tight fit between the two. With the toroids clamped together, apply hot glue liberally, and cut off the excess once it has solidified.

Winding the formed toroid must be done by hand. It is important to pay careful attention to the winding pattern to ensure a tight packing, but it is not necessary to keep track of turn count, since the approximate Ω/Turn values for the cores used in the experimental setup are recorded in Chapter 2. The DC resistance of the winding can be measured periodically to estimate the current turn count.

Once the pickup is wound, it is usually advantageous to pot it so that the windings to not come loose over time. Many potting materials can be used, but in the past "liquid electrical tape" worked well. To apply, brush on liberally while wearing gloves,

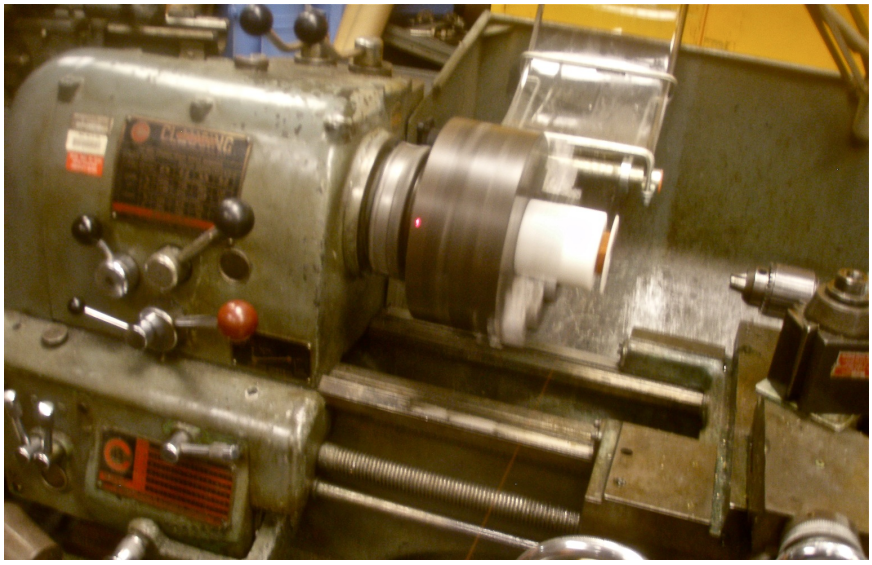


Figure B-1: Coil winding on the lathe.

with a fume extractor present. Wait five minutes, rotate the pickup, and repeat. After sufficient liquid electrical tape has been applied, let the pickup sit for about 24 hours for it to fully dry.

B.2 Through-Door Link Coil Construction

B.2.1 Winding

Winding the coils for the inductive through-door link is straightforward to do by hand if the turn count is small. However, if the turn count is in the hundreds or above, using a mill or lathe will be much easier. A fixture has been developed to hold the coil bobbins in place on the mill for winding. A drawing of the fixture is shown in Figure B-2.

A photo of a winding setup on the lathe in the LEES machine shop is shown in Figure B-1. The bobbin-holder fixture is secured in the lathe chuck, with the bobbin press-fitted on the fixture. For winding, the lathe should be set to the lowest speed possible. The desired wire should be on a spool that can freely rotate, positioned level with the bobbin in the fixture. It is important to set the direction of the lathe appropriately. When the lathe is engaged, carefully monitor the winding progress for

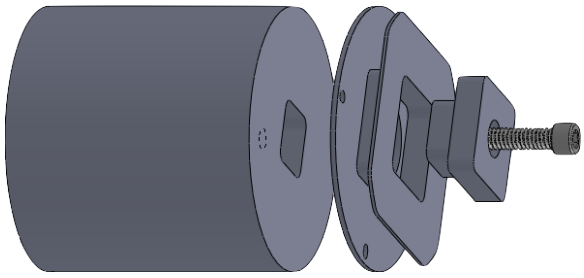


Figure B-2: Fixture for coil winding on the lathe.

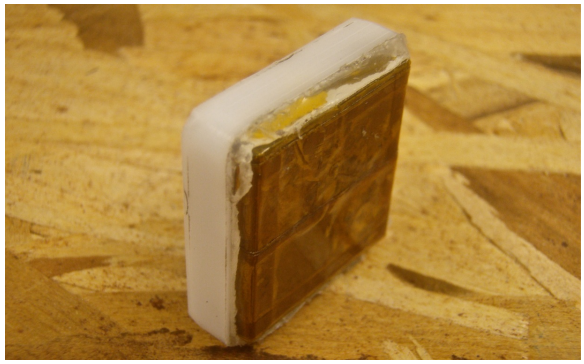


Figure B-3: Permanent magnets placed in delrin holder.

tangles. Safety glasses should be worn at all times.

Turns can be counted by timing the duration that the lathe is on, and multiplying by the frequency of the motor. Alternatively, a laser frequency counter can be used to improve accuracy.

B.2.2 Permanent Magnet Configuration

The 52 MGOe neodymium magnets used in the experimental setup are incredibly strong, and should be handled with care. To construct a core for a bobbin, *carefully* align block magnets in the pole pattern shown in Figure 3-10. When aligning the magnets, use a small object to guide the magnets into place. Do *NOT* allow the magnets to "snap" towards each other, as this could cause them to crack or shatter.

Once the magnets are aligned, cover them with a couple layers of kapton tape to prevent them front chipping. Once taped, the magnets can be inserted into their delrin holder. To secure the magnets, carefully apply hot glue around their edges, while they are centered in the holder. Once the glue dries, cut off any excess. The

magnets should always have sufficient clearance that they may rest flush against the steel of the breaker panel door. A photo of magnets secured in their delrin holder is shown in Figure B-3.

B.2.3 Bobbin Construction Process Plan

The following construction process plan for the bobbins holding the through-door coils was originally written by Andrew Carlson '12.

1. (Cold Saw) Rough cut blanks from delrin round stock, $\approx 0.2''$ longer than final thickness. This can be done on the band saw, but the cold saw is faster and produces much straighter cuts.

2. (Lathe) Square blank ends and face to final thickness. The lathe chuck jaws should be flipped to provide a flat surface to butt blanks up against. Shims can be used to space blank off of the chuck face.

3. **[Optional]** (Lathe) Drill $\gtrsim 0.5''$ hole through center of blank using a $\approx 1/2''$ drill bit. This is for locating stock center in subsequent milling operations. This is not necessary is the fixture is made for milling operations.

4. **[Optional]** (CNC Mill) Machine $\approx 0.005''$ oversized shallow pocket in aluminum plate (for fixture) using a $1/2''$ flat endmill. This fixture is useful if producing multiple bobbins. Other fixture options are possible as well.

5. (CNC Mill) Run program to machine rectangular and circular pockets in blanks with a $1/4''$ flat endmill.

6. (CNC Mill) Clamp lathe fixture into mill vice with plug installed in fixture. Rotate fixture to align with mill coordinate system. The dial indicator should be used to align the fixture with the mill coordinate system, or the flats could be machined on the existing fixture. A V-block should be used to better hold the fixture.

7. (CNC Mill) Clamp the bobbin to the fixture. The plug should be pressed into the bobbin such that the boss extends through the circular pocket in the bobbin. The boss is then pressed into the lathe fixture. A 1/4-20 bolt is used to clamp the bobbin-plug assembly to the fixture.

8. (CNC Mill) Run program to machine flats, groove, and bolt holes in bobbin using a $1/2''$ flat endmill, a $4''$ OD slitting saw, and a $1/8''$ flat endmill, respectively. The sitting saw $4''$ nominal OD, $3/8''$ wide. Borrowed from Edgerton student shop, all tools zeroed on top of blank.

9. Remove bobbin from fixture. Care should be taken while removing the bobbin, as it will be pretty flimsy.

B.3 In-Panel Electronics PCB Revision Notes

The in-panel electronics PCB is relatively small, and has few known bugs. In the future, the following changes should be implemented:

- Component values should be removed from the silkscreens.
- The library package for the SR44 battery holder need to be adjusted to match the actual package.
- The silkscreen line indicating the appropriate pickup position should be moved lower on the board design with the AD627 instrumentation amplifier.
- The length of board on which the pickup rests should be made less wide, so smaller toroids can be used if desired.
- The many 0Ω resistors can be removed now that our design is finalized.
- Testpoints would be helpful.
- If space is available, a variable capacitor could be added to more precisely tune the resonator.

B.4 Signal Conditioning PCB Revision Notes

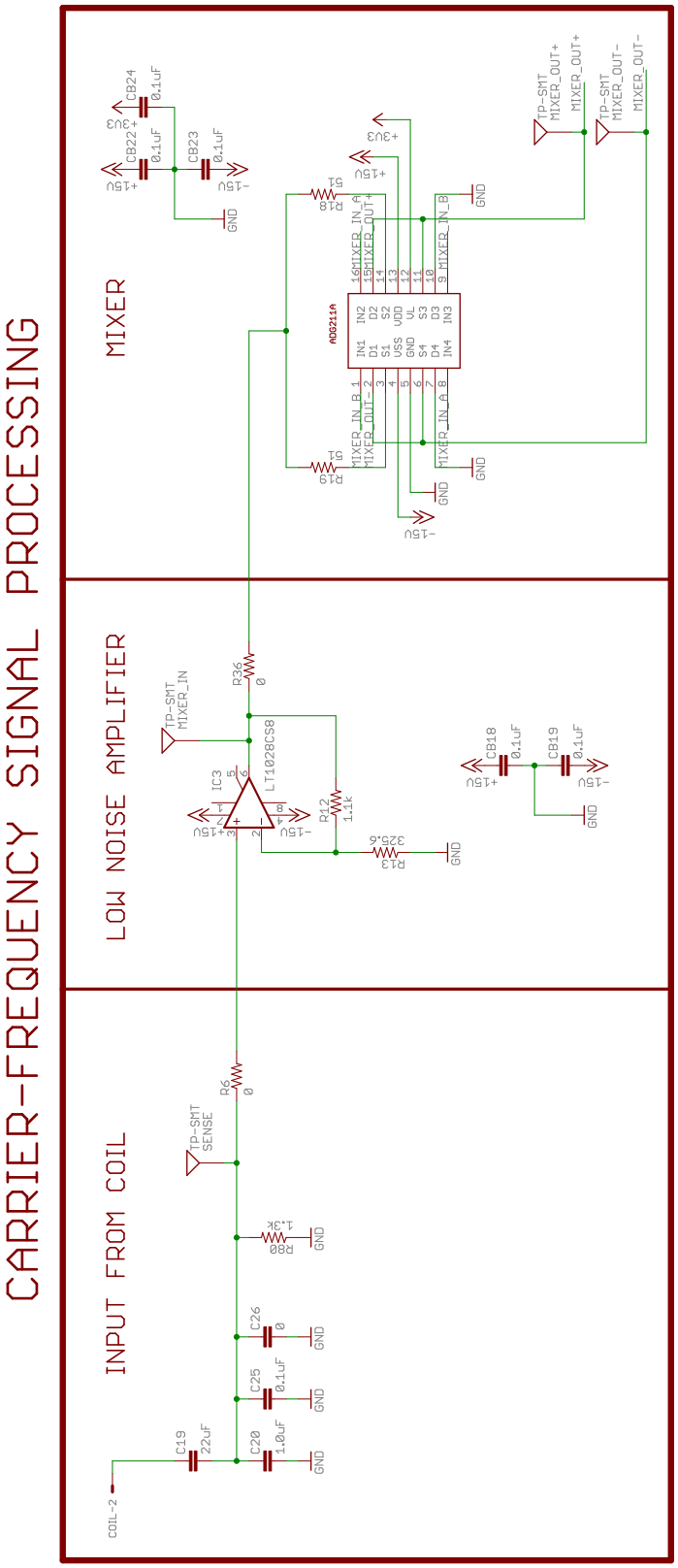
- Rearrange the UART header pins for compatibility with the Sparkfun FTDI USB to RS232 breakout board and add more clearance, or simply implement the USB to RS232 converter on-board.
- Change the programming header silkscreen footprint to a molex connector.
- Add a low ESR tantalum capacitor for coil drive power bypassing.
- Power FET heatsinks in the coil drive circuit are unnecessary and can be removed.

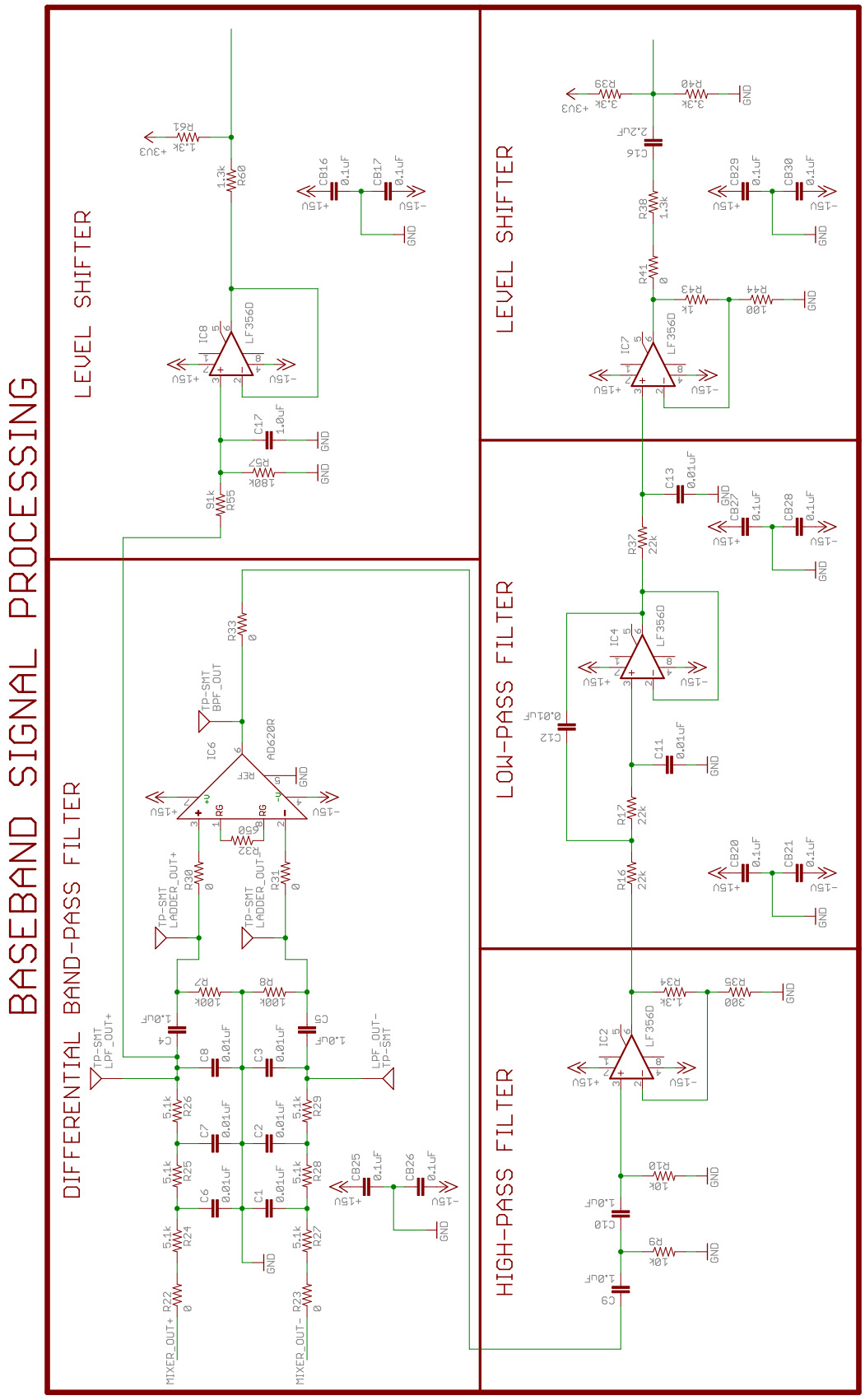
Appendix C

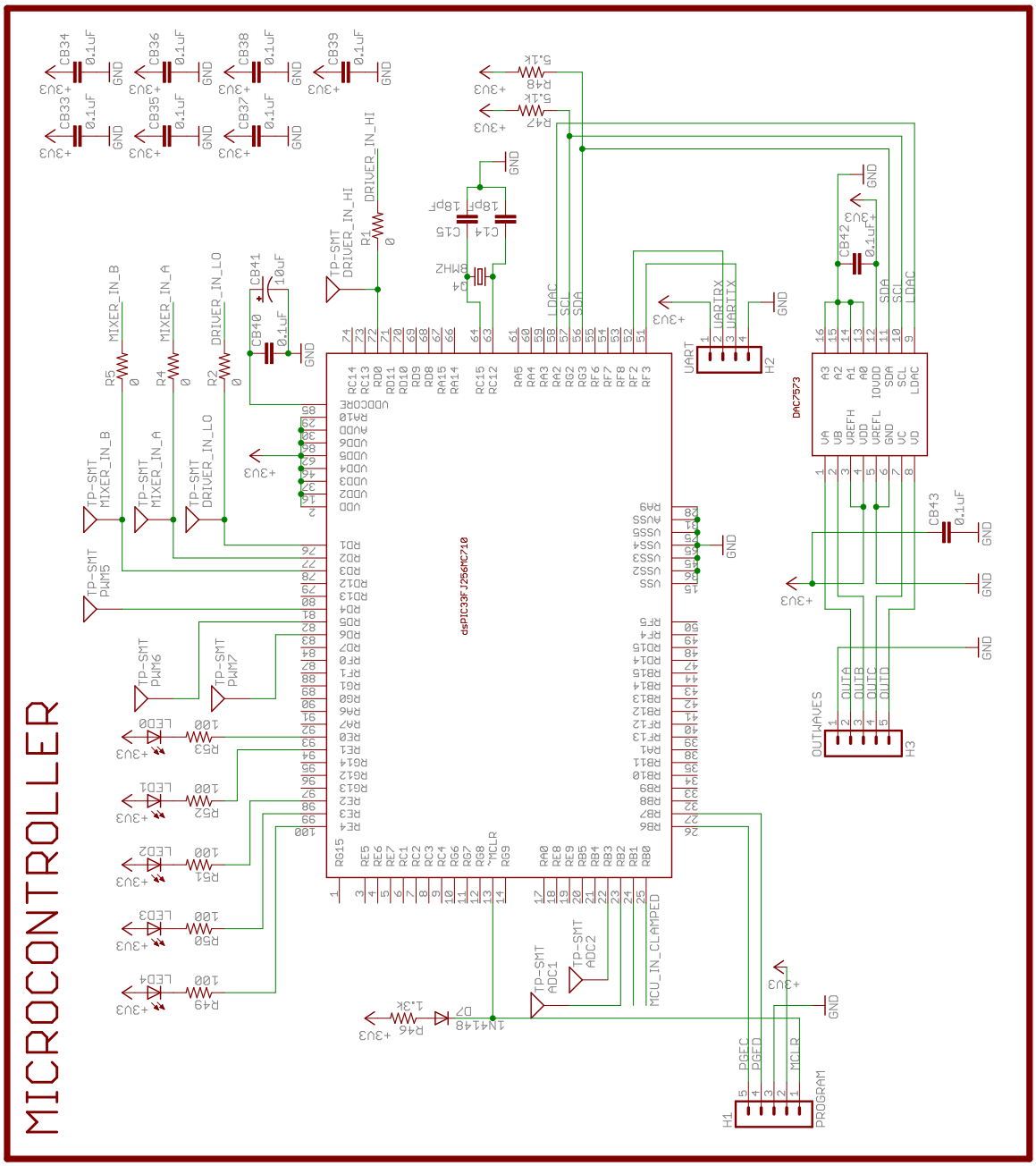
Experimental Setup Schematics

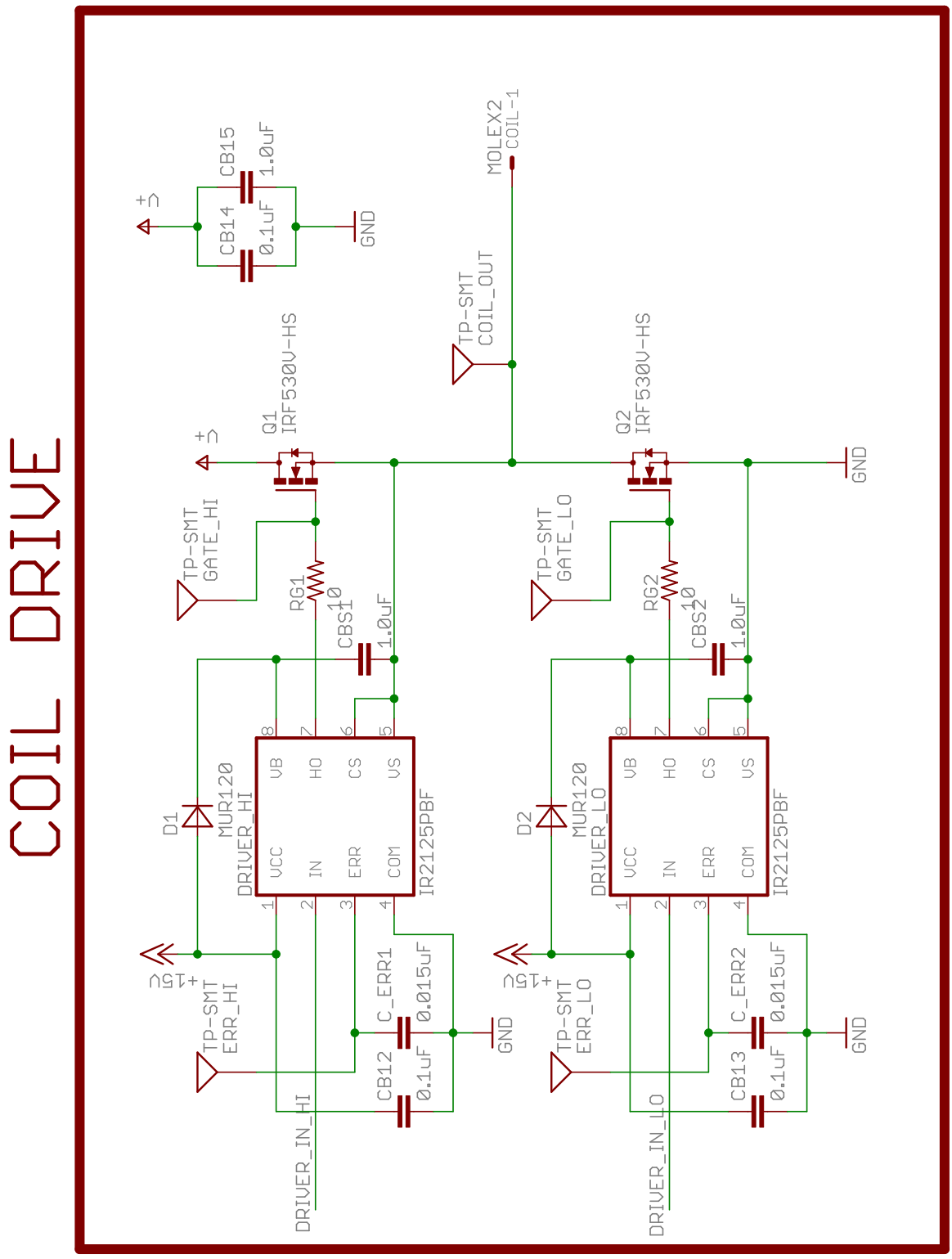
This appendix lists the complete electrical schematics of our experimental sensor prototype.

C.0.1 Signal Conditioning Circuitry



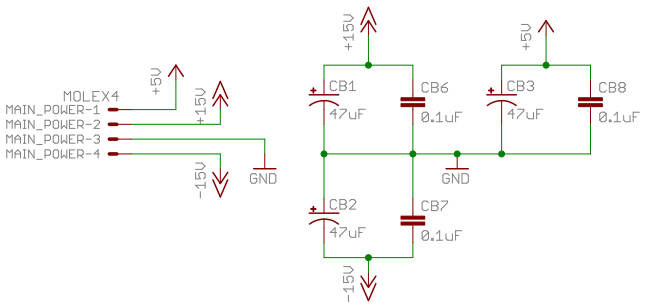

BASEBAND SIGNAL PROCESSING
DIFFERENTIAL BAND-PASS FILTER
LEVEL SHIFTER
LOW-PASS FILTER
HIGH-PASS FILTER
LEVEL SHIFTER
IC8
LF356D
IC6
AD620R
IC4
LF356D
IC2
LF356D
IC7
LF356D
+15V
-15V
GND
+3V3
TP-SMT
BPF_OUT
TP-SMT
LPF_OUT+
TP-SMT
LPF_OUT-
TP-SMT
LADDER_OUT+
TP-SMT
LADDER_OUT-
MIXER_OUT+
MIXER_OUT-
R33
R32
R30
R31
R22
R23
R24
R25
R26
R27
R28
R29
R7
R8
R55
R57
R60
R61
R37
R17
R16
R34
R35
R10
R9
R38
R41
R43
R44
R39
R40
C4
C8
C3
C5
C7
C2
C6
C1
C17
C13
C12
C11
C10
C9
C16
CB16
CB17
CB25
CB26
CB27
CB28
CB20
CB21
CB29
CB30
1.3k
91k
1.0uF
0.01uF
0.1uF
2.2uF
22k
10k
100
1k
3.3k
300
5.1k
100k
1800k
650
0


MICROCONTROLLER
dsPIC33FJ256MC710
DAC7573
MIXER_IN_B
MIXER_IN_A
DRIVER_IN_LO
DRIVER_IN_HI
LDAC
SCL
SDA
UART
U1RARX
U1RATX
OUTWAVES
OUTA
OUTB
OUTC
OUTD
PROGRAM
PGEC
PGED
MCLR
MCU_IN_CLAMPED
ADC1
ADC2
PWM5
PWM6
PWM7
1N4148
+3V3
GND

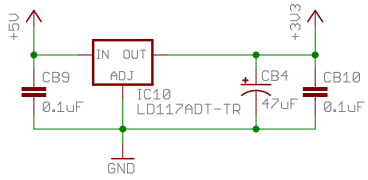

COIL DRIVE
+5
CB15
1.0uF
CB14
0.1uF
GND
MOLEX2
COIL-1
TP-SMT
COIL_OUT
Q1
IRF530V-HS
Q2
IRF530V-HS
GND
TP-SMT
GATE_HI
TP-SMT
GATE_LO
RG1
10
RG2
10
CBS1
1.0uF
CBS2
1.0uF
D1
MUR120
D2
MUR120
DRIVER_HI
DRIVER_LO
VB
HO
CS
VS
VCC
IN
ERR
COM
IR2125PBF
+15V
TP-SMT
ERR_HI
TP-SMT
ERR_LO
C_ERR1
0.015uF
C_ERR2
0.015uF
CB12
0.1uF
CB13
0.1uF
GND
GND
DRIVER_IN_HI
DRIVER_IN_LO

POWER

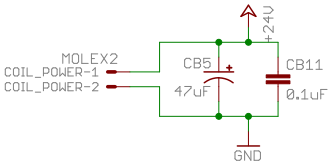
MAIN POWER



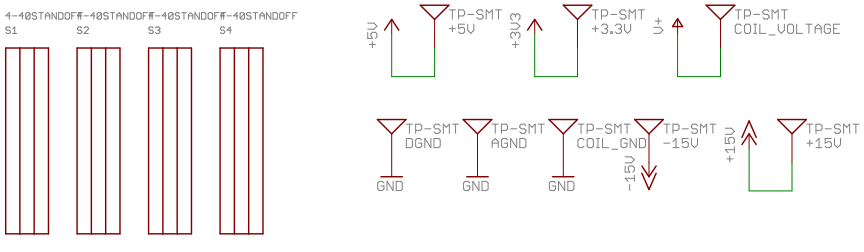
3.3V REGULATOR



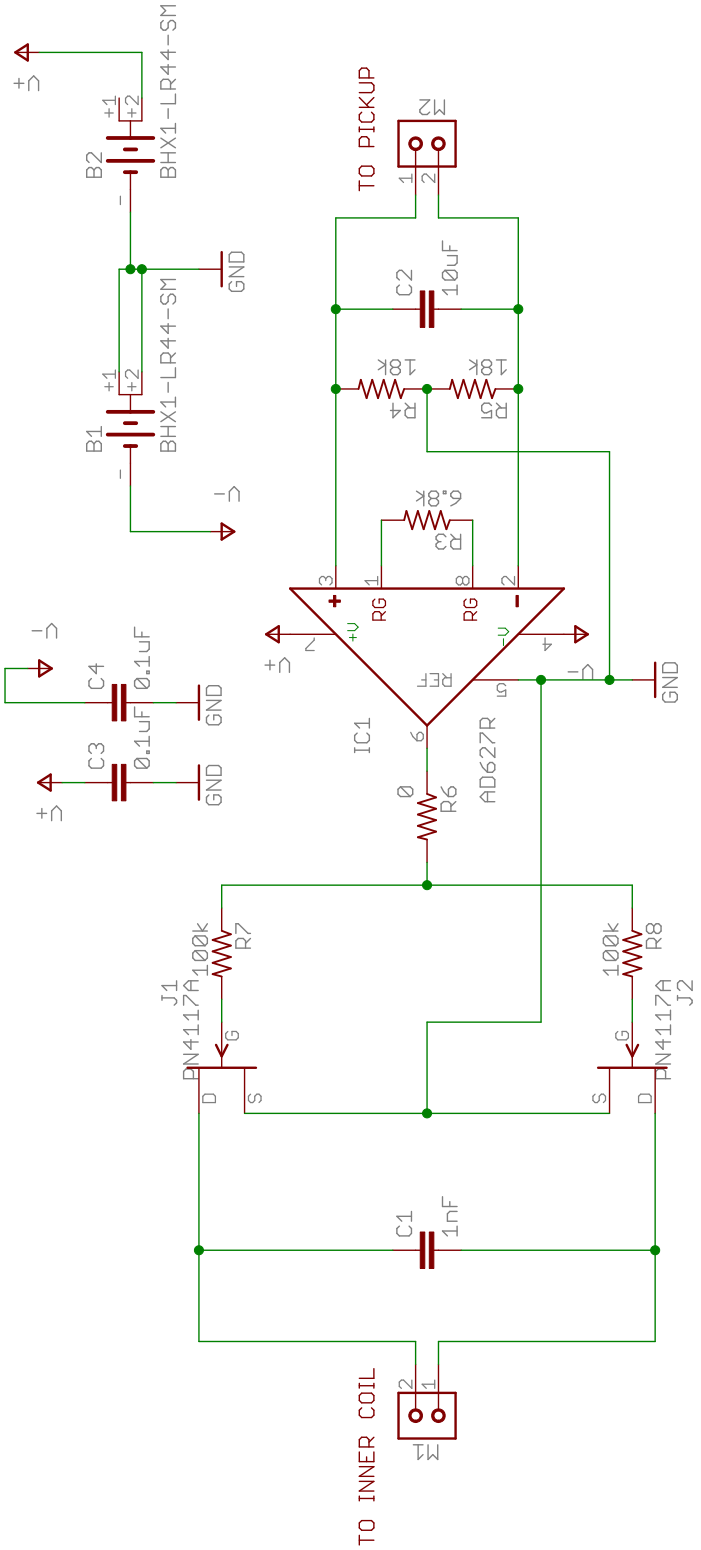
COIL POWER



EVERYTHING ELSE



C.0.2 Pickup Amplifier Circuitry



Appendix D

Printed Circuit Boards

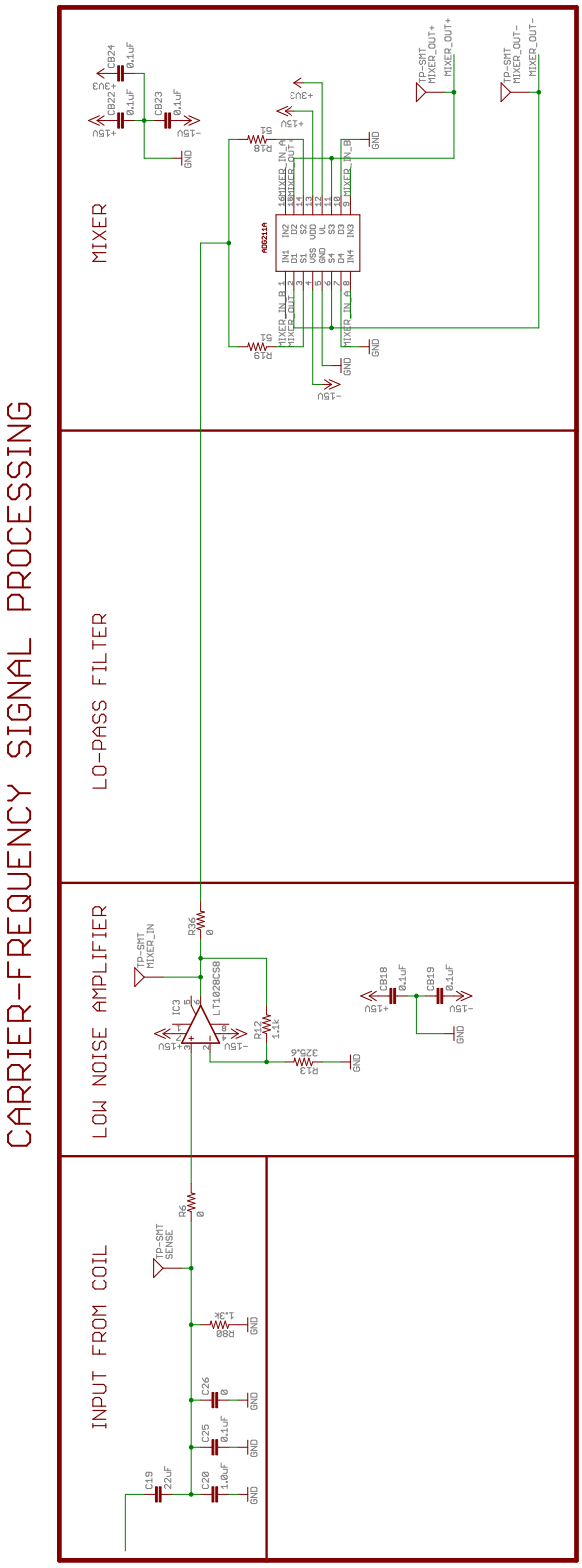
This appendix contains complete schematics and mechanical drawings of printed circuit boards (PCBs) of previous, current, and future revisions of the experimental sensor prototype.

- Section D.1 lists the schematics for PCB outside the breaker panel that contains the coil drive and signal processing circuitry (outer PCB).
- Section D.1.1 contains schematics for a revision of the outer PCB that is currently in progress. These are very similar to the schematics of the experimental setup, and have only minor changes. They are included nonetheless for completeness.
- Sections D.1.2, D.1.3, and D.1.4 contain schematics, layouts, and a bill of materials for the current revision of the outer PCB, which was modified for use in our experimental setup.
- Section D.2 lists schematics, layouts, and bills of materials for two new printed circuit boards that hold the current-sensing eletronics. These PCBs can be attached directly to the breaker face. One version of the PCB uses an instrumentation amplifier-based pickup amplification stage, while the other uses a passive transformer-based pickup amplification stage. The PCB with the instrumentation amplifier design was discussed in Section 7.2.1 and a photo is

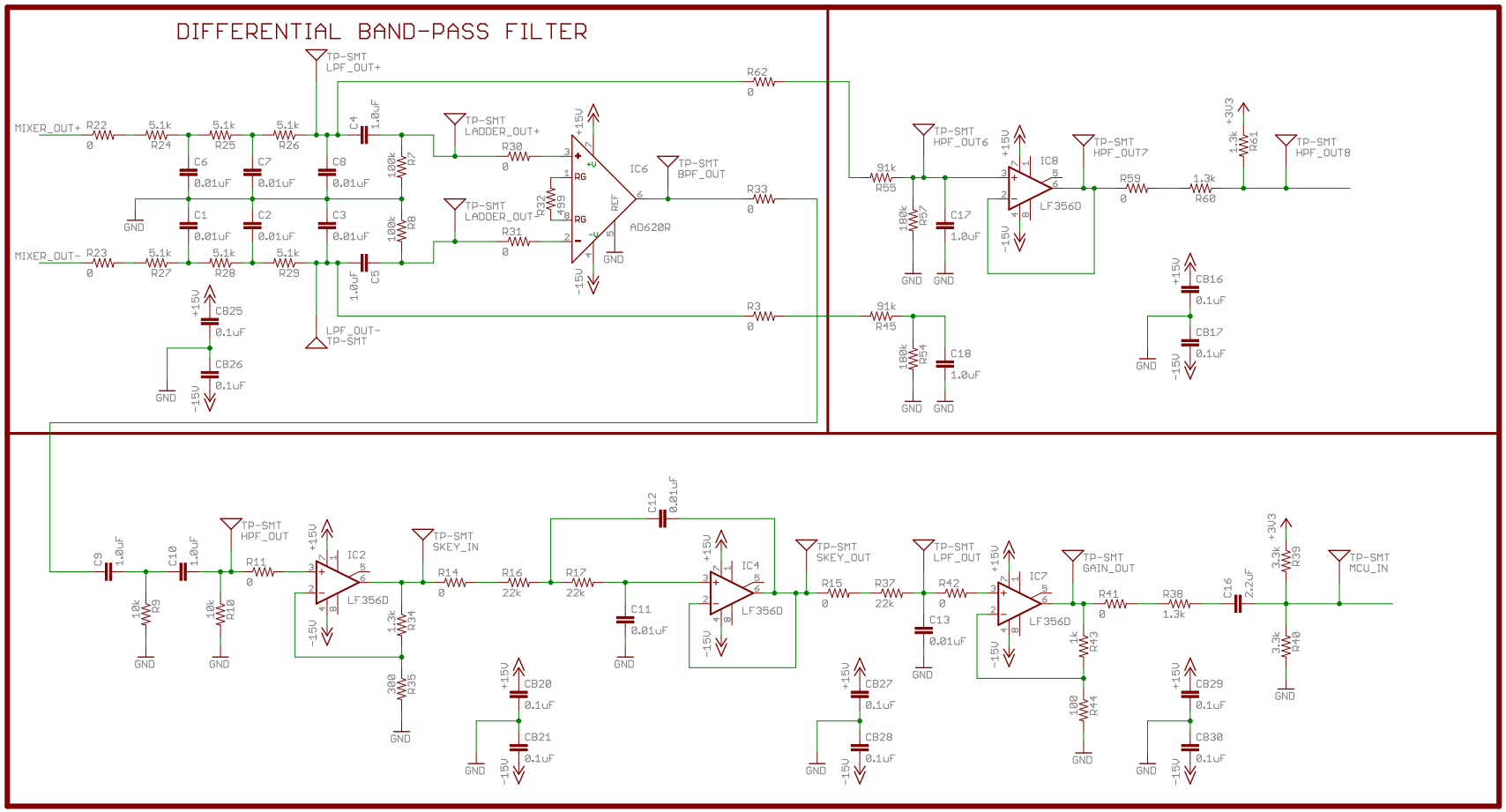
shown in Figure 7-1. These PCBs were not used in our experimental sensor prototype, although the PCB with the instrumenation amplifier design is electrically identical to the circuit used in the prototype.

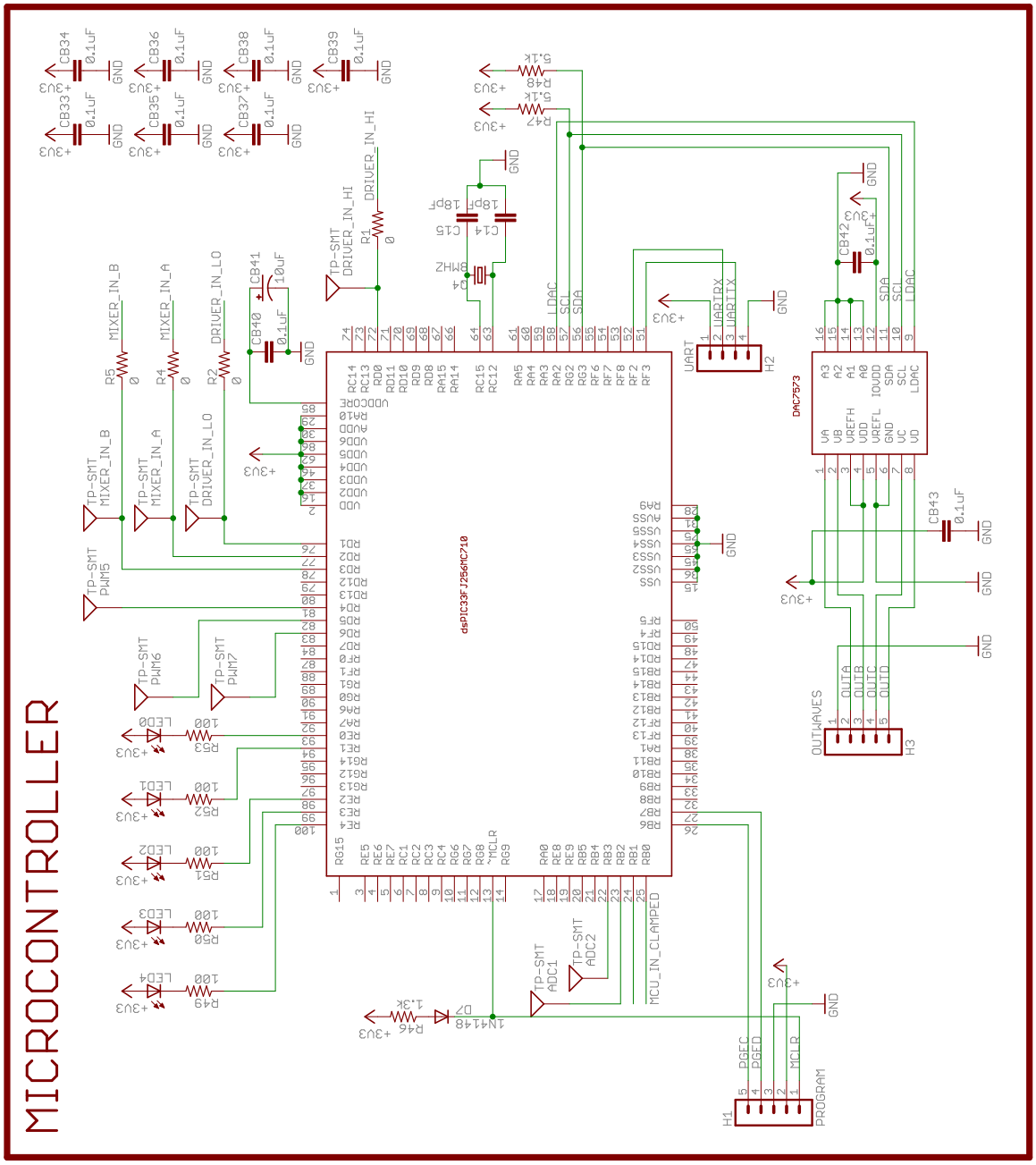
D.1 Signal Conditioning Circuitry

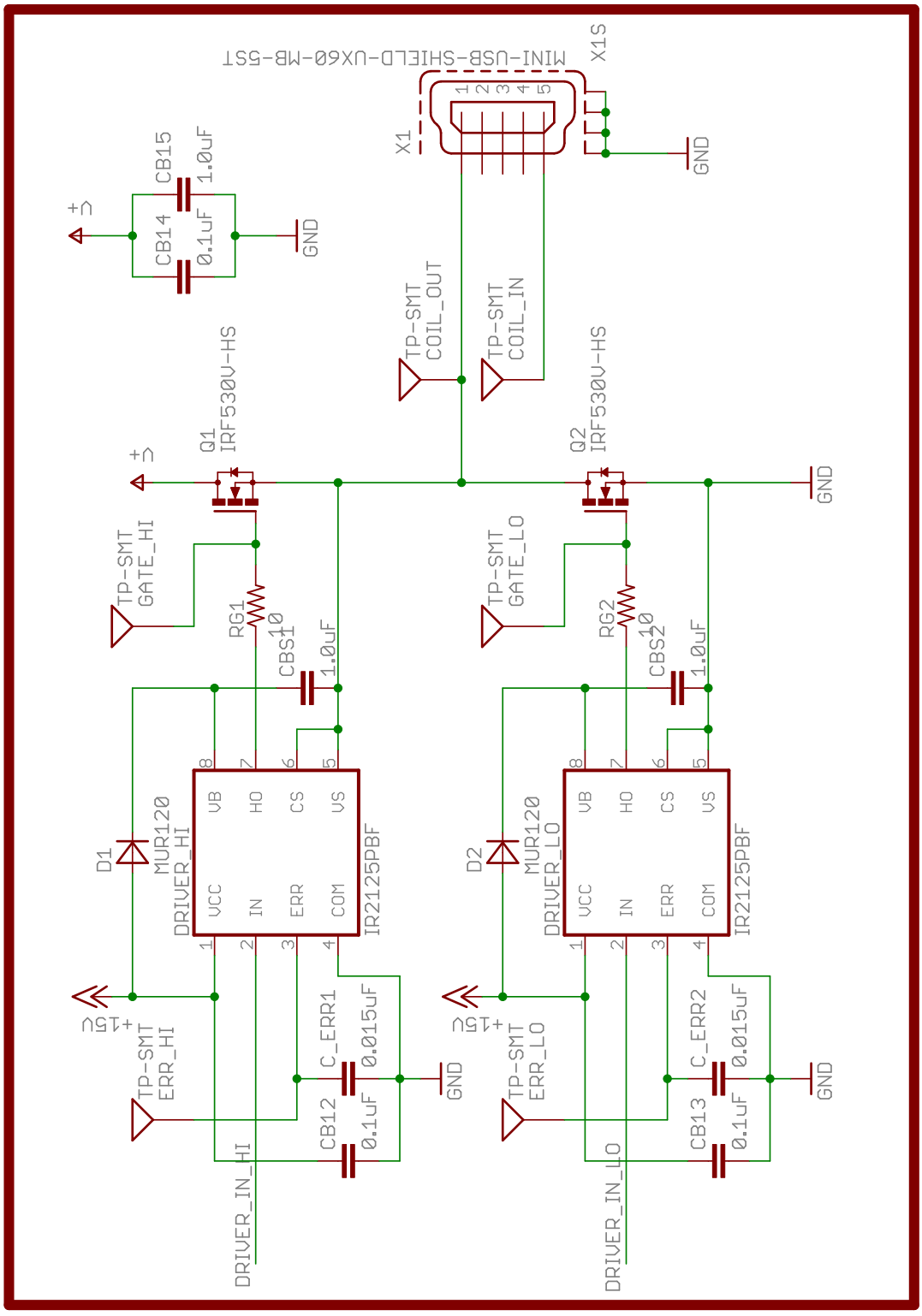
D.1.1 Future Revision Schematics



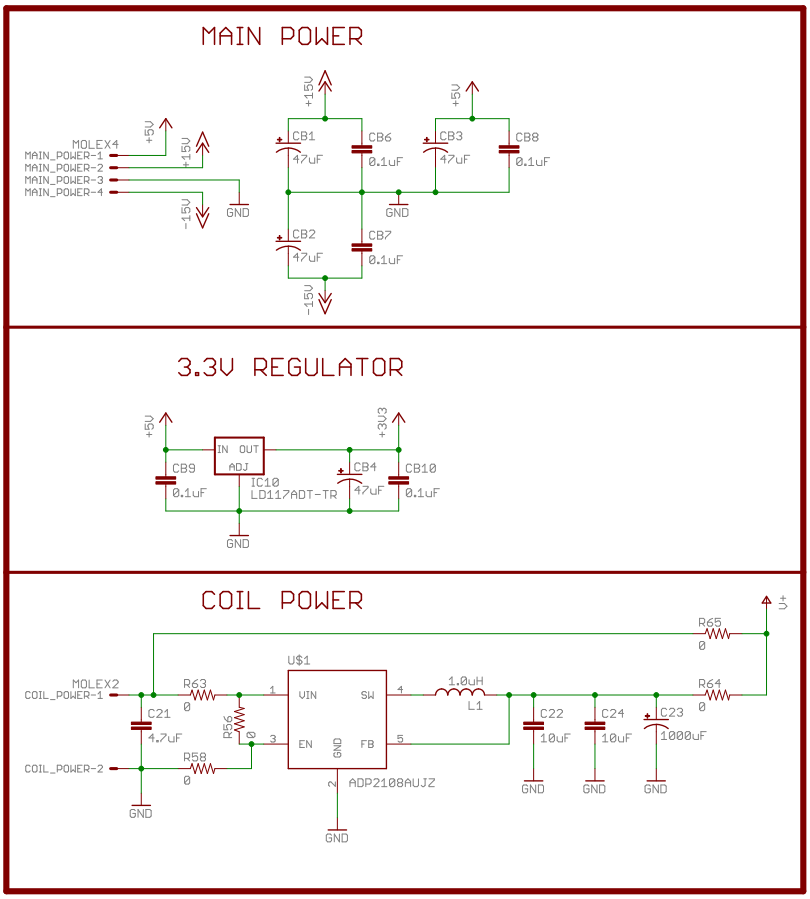
BASEBAND SIGNAL PROCESSING



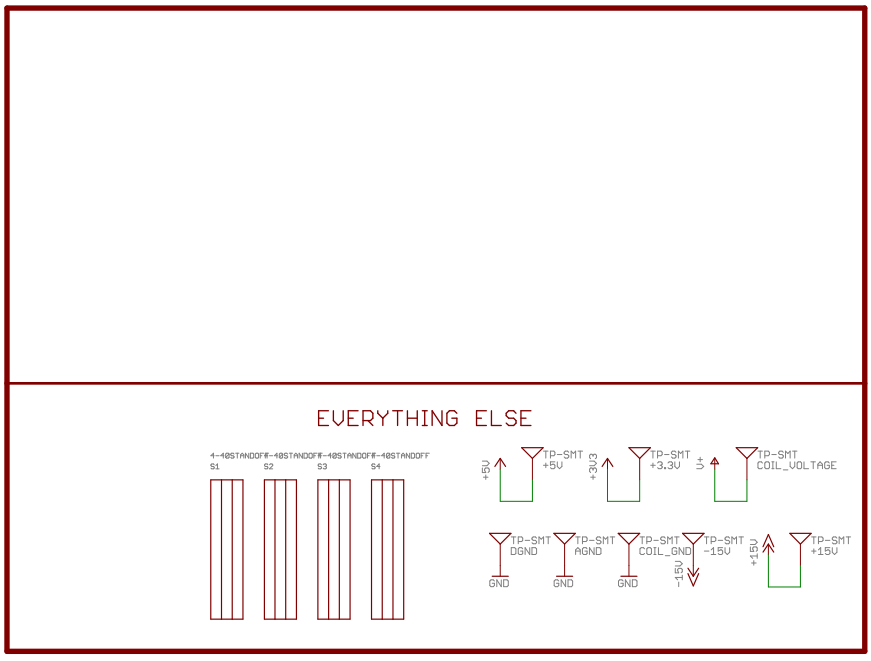

MICROCONTROLLER
dsPIC33FJ256MC710
DAC7573
UART
H1
H2
H3
PROGRAM
OUTWAVES
MCU_IN_CLAMPED
1N4148
LDAC
SCL
SDA
MCLR
PGED
PGEC


COIL DRIVE
MINI-USB-SHIELD-UX60-MB-5ST
X1S
X1
GND
CB15
1.0uF
CB14
0.1uF
+5
TP-SMT
COIL_OUT
TP-SMT
COIL_IN
Q1
IRF530V-HS
Q2
IRF530V-HS
TP-SMT
GATE_HI
TP-SMT
GATE_LO
RG1
10
RG2
10
CBS1
1.0uF
CBS2
1.0uF
D1
MUR120
D2
MUR120
DRIVER_HI
DRIVER_LO
VB
HO
CS
VS
VCC
IN
ERR
COM
IR2125PBF
+15
TP-SMT
ERR_HI
TP-SMT
ERR_LO
C_ERR1
0.015uF
C_ERR2
0.015uF
CB12
0.1uF
CB13
0.1uF
DRIVER_IN_HI
DRIVER_IN_LO

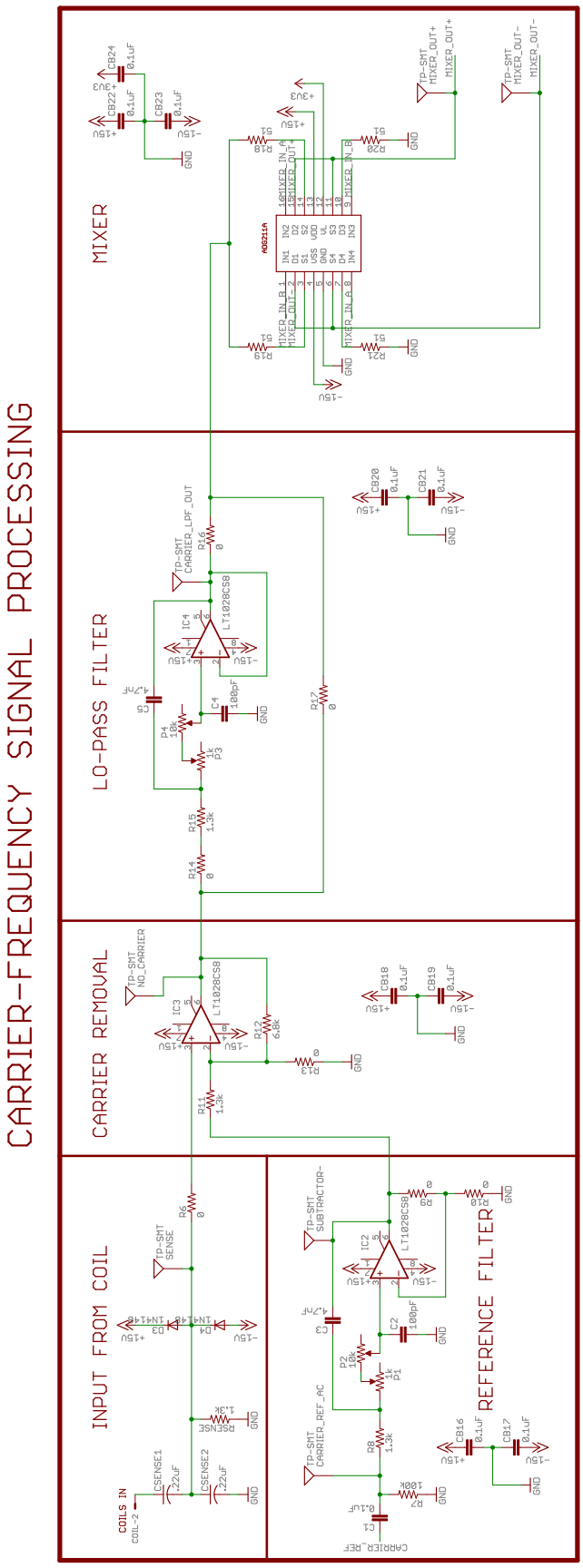
POWER

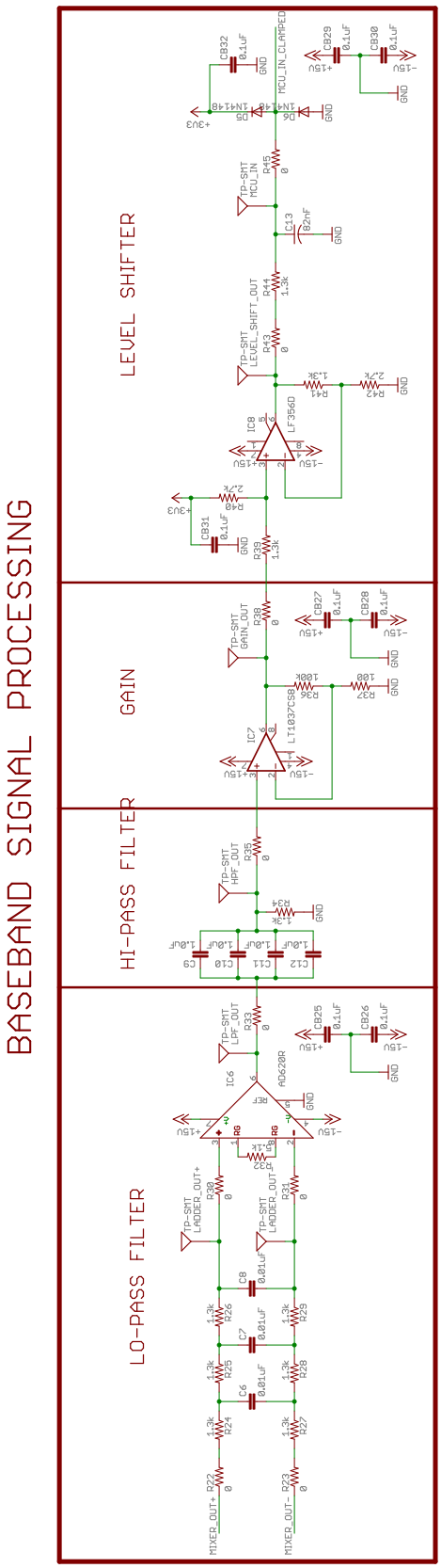


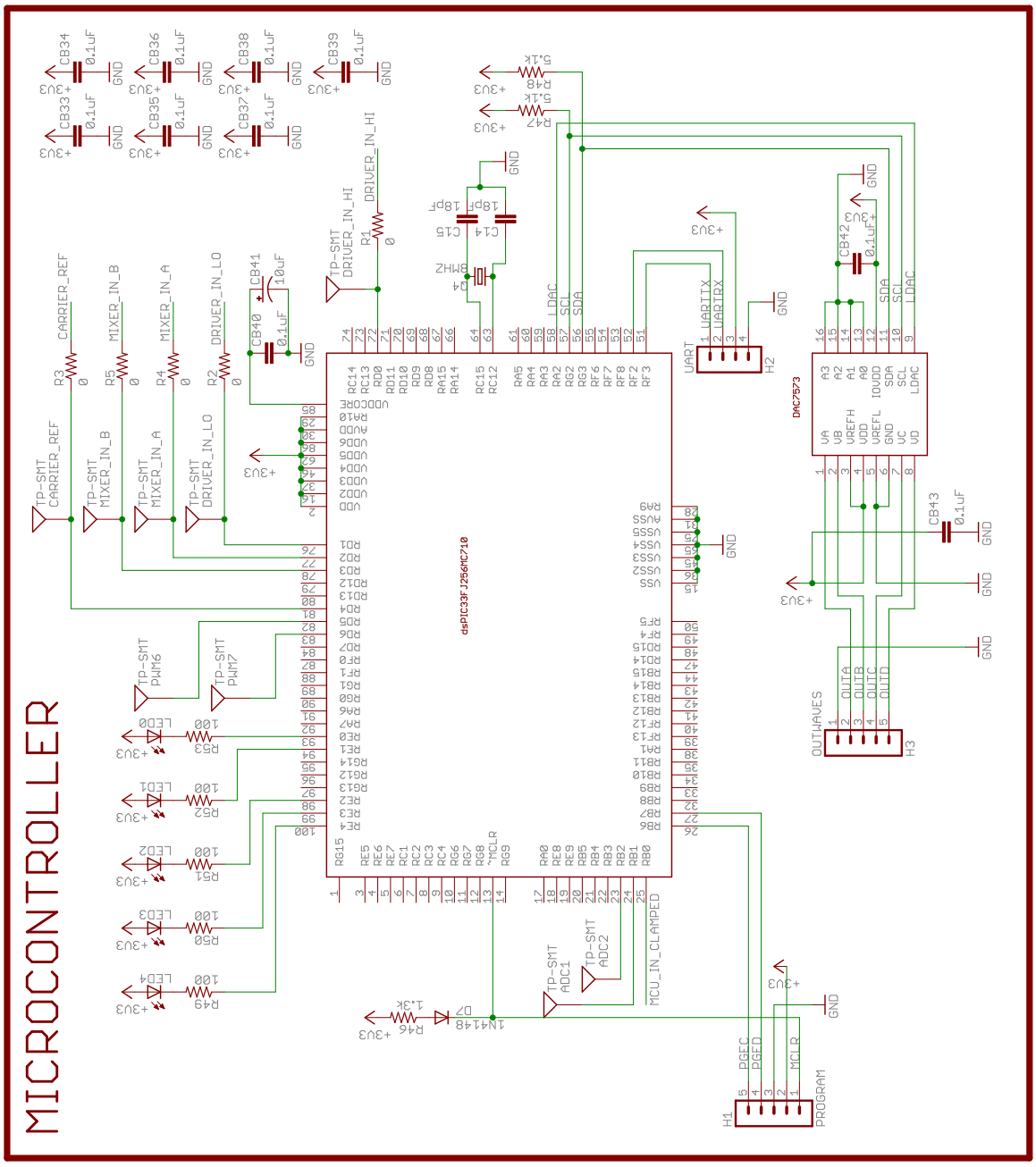
EXTRAS

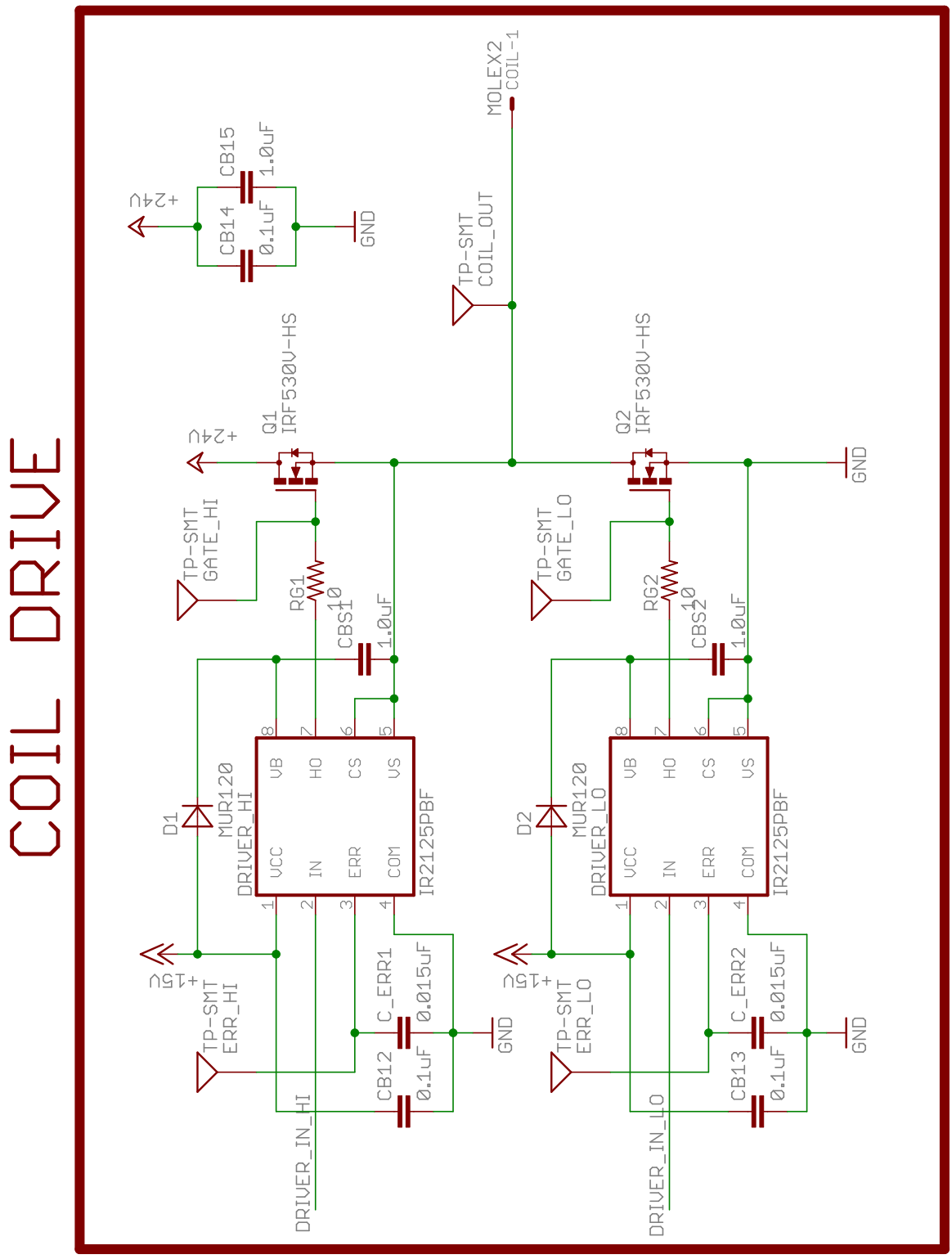


D.1.2 Previous Revision Schematics

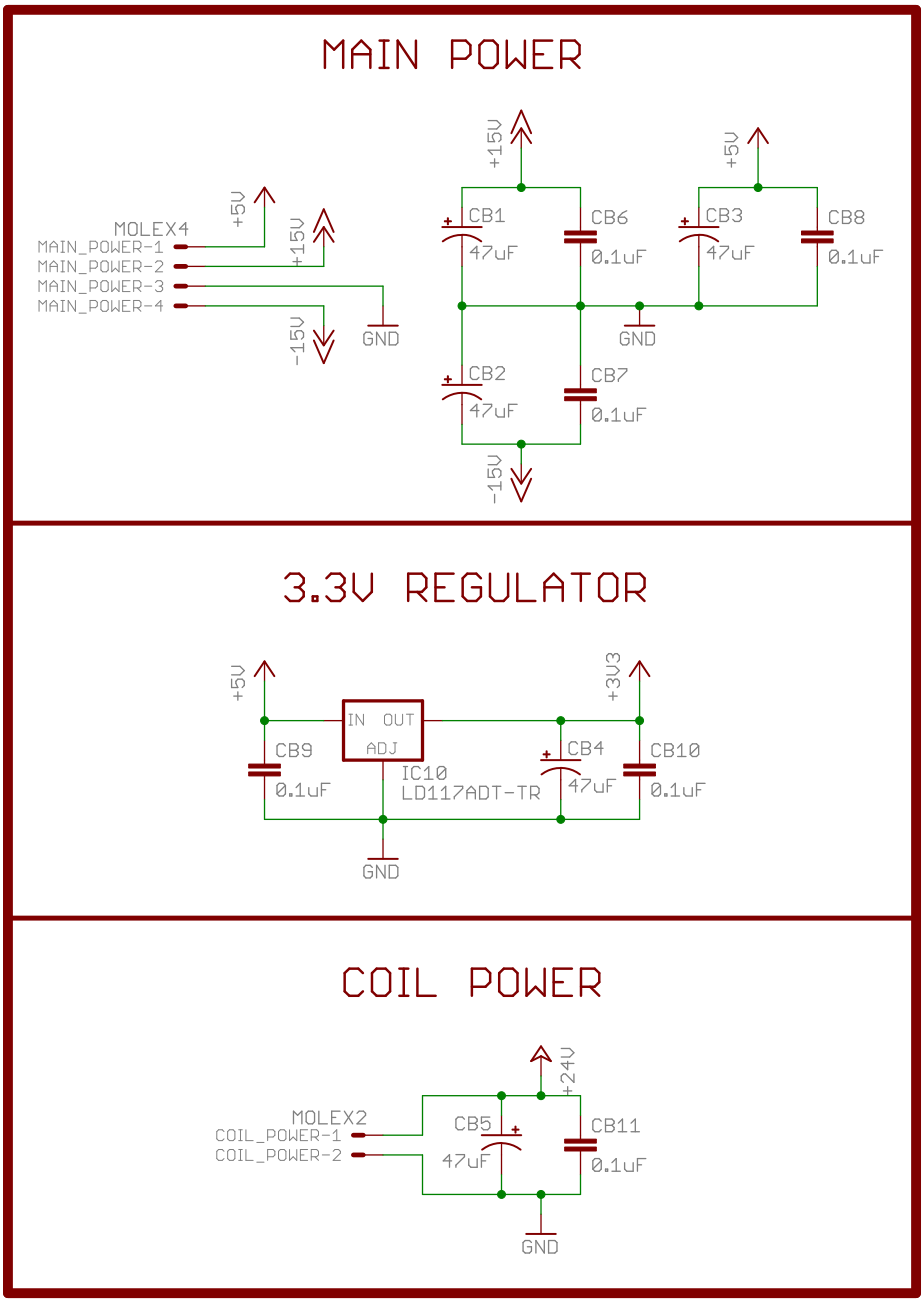



BASEBAND SIGNAL PROCESSING
LO-PASS FILTER
HI-PASS FILTER
GAIN
LEVEL SHIFTER
MCU_IN_CLAMPED
MIXER_OUT+
MIXER_OUT-
AD620R
LF356D
LT1037CS8

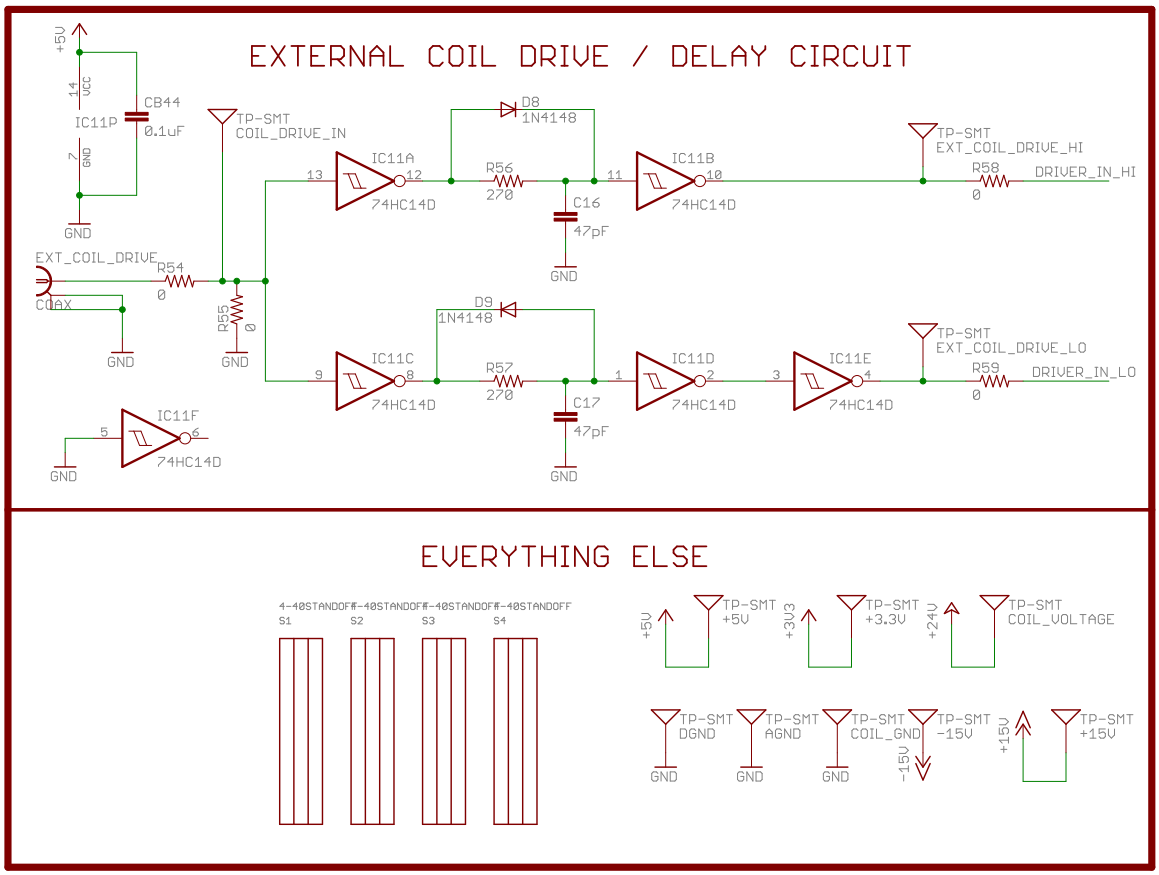

MICROCONTROLLER
dsPIC33FJ256MC710
DAC7573
CARRIER_REF
MIXER_IN_B
MIXER_IN_A
DRIVER_IN_LO
DRIVER_IN_HI
LDAC
SCL
SDA
UART
UARTTX
UARTRX
OUTWAVES
OUTA
OUTB
OUTC
OUTD
PROGRAM
PGEC
PGED
MCLR
MCU_IN_CLAMPED
ADC1
ADC2
PWM6
PWM7
1N4148
+3V3
GND


COIL DRIVE
MOLEX2
COIL-1
TP-SMT
COIL_OUT
CB15
1.0uF
CB14
0.1uF
+24C
GND
Q1
IRF530V-HS
Q2
IRF530V-HS
TP-SMT
GATE_HI
TP-SMT
GATE_LO
RG1
10
RG2
10
CBS1
1.0uF
CBS2
1.0uF
D1
MUR120
D2
MUR120
DRIVER_HI
DRIVER_LO
VB
HO
CS
VS
VCC
IN
ERR
COM
IR2125PBF
+15C
TP-SMT
ERR_HI
TP-SMT
ERR_LO
C_ERR1
0.015uF
C_ERR2
0.015uF
CB12
0.1uF
CB13
0.1uF
DRIVER_IN_HI
DRIVER_IN_LO

POWER

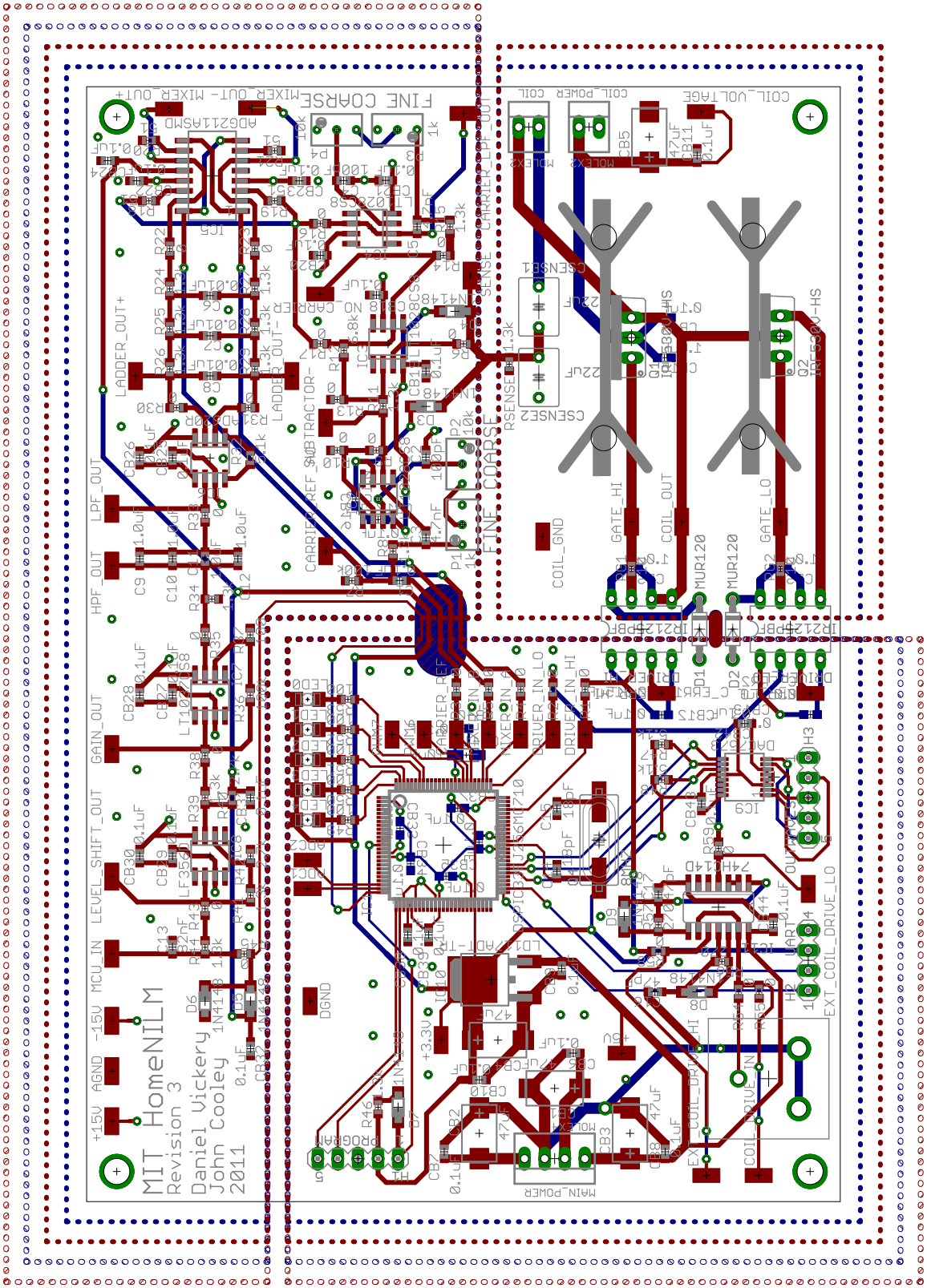

MAIN POWER
MOLEX4
MAIN_POWER-1
MAIN_POWER-2
MAIN_POWER-3
MAIN_POWER-4
+5V
+15V
-15V
GND
CB1
47uF
CB6
0.1uF
CB2
47uF
CB7
0.1uF
CB3
47uF
CB8
0.1uF
3.3V REGULATOR
IN OUT
ADJ
IC10
LD1117ADT-TR
CB9
0.1uF
CB4
47uF
CB10
0.1uF
+3V3
COIL POWER
MOLEX2
COIL_POWER-1
COIL_POWER-2
+24V
CB5
47uF
CB11
0.1uF

EXTRAS

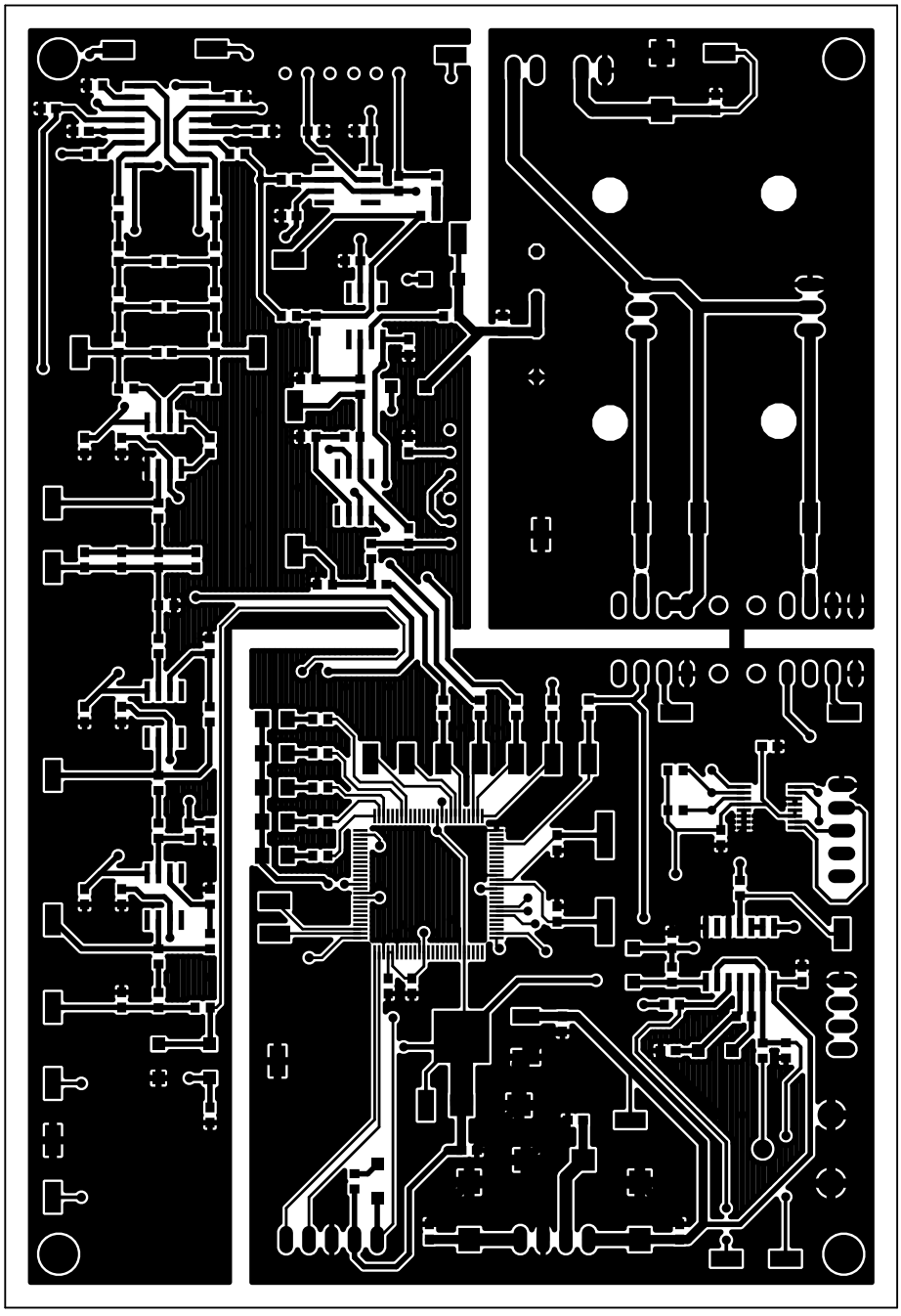

EXTERNAL COIL DRIVE / DELAY CIRCUIT
+5V
14
VCC
IC11P
CB44
0.1uF
7
GND
GND
TP-SMT
COIL_DRIVE_IN
EXT_COIL_DRIVE
COAX
R54
0
R55
0
GND
GND
IC11A
74HC14D
13
12
D8
1N4148
R56
270
C16
47pF
GND
IC11B
74HC14D
11
10
TP-SMT
EXT_COIL_DRIVE_HI
R58
0
DRIVER_IN_HI
D9
1N4148
IC11C
74HC14D
9
8
R57
270
C17
47pF
GND
IC11D
74HC14D
1
2
IC11E
74HC14D
3
4
TP-SMT
EXT_COIL_DRIVE_LO
R59
0
DRIVER_IN_LO
IC11F
74HC14D
5
6
GND
EVERYTHING ELSE
4-40STANDOFF
S1
4-40STANDOFF
S2
4-40STANDOFF
S3
4-40STANDOFF
S4
+5V
TP-SMT
+5V
+3V3
TP-SMT
+3.3V
+24V
TP-SMT
COIL_VOLTAGE
TP-SMT
DGND
GND
TP-SMT
AGND
GND
TP-SMT
COIL_GND
GND
-15V
TP-SMT
-15V
+15V
TP-SMT
+15V

D.1.3 Previous Revision PCB Layout

Complete Layout



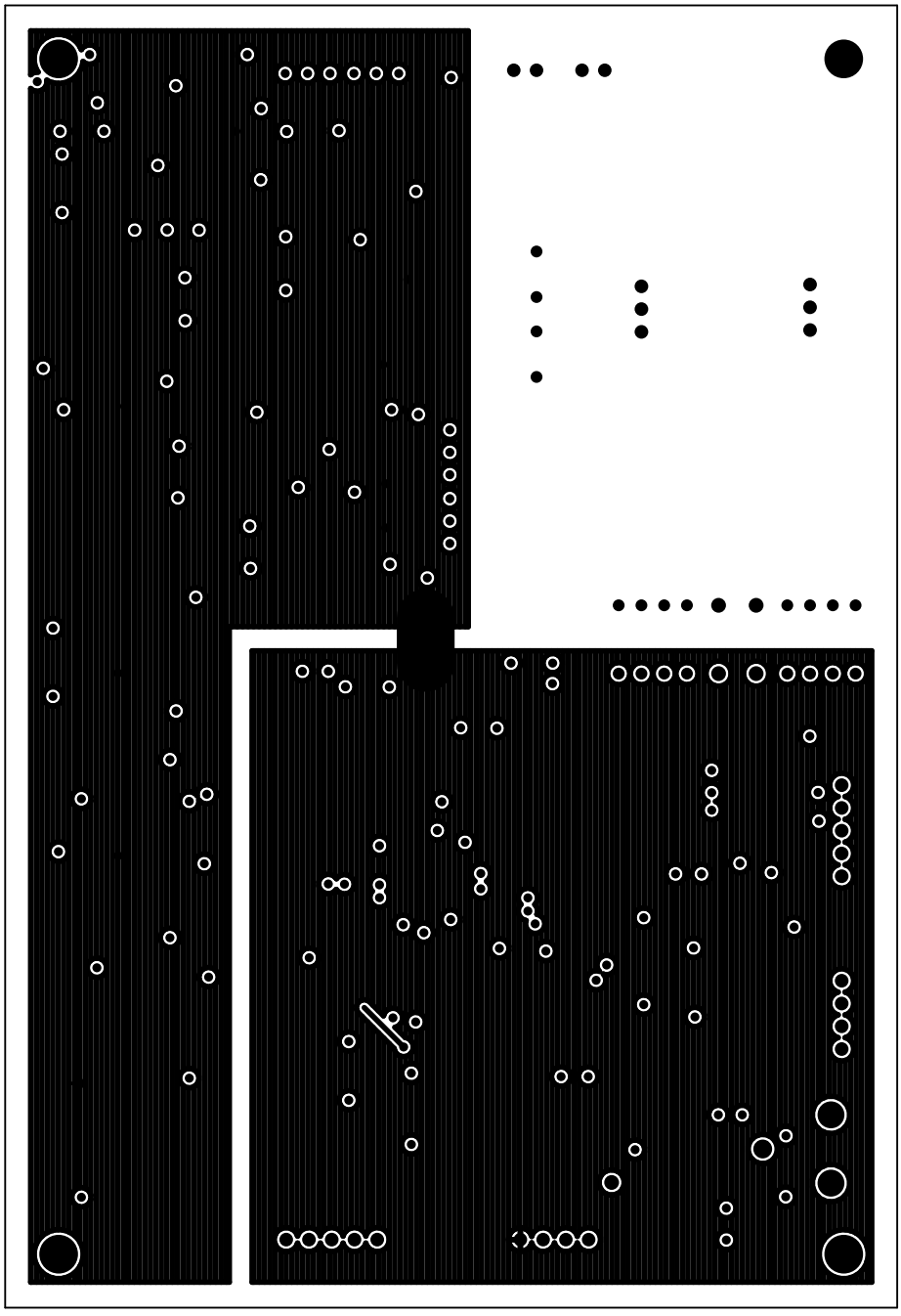
Layer 1 Copper



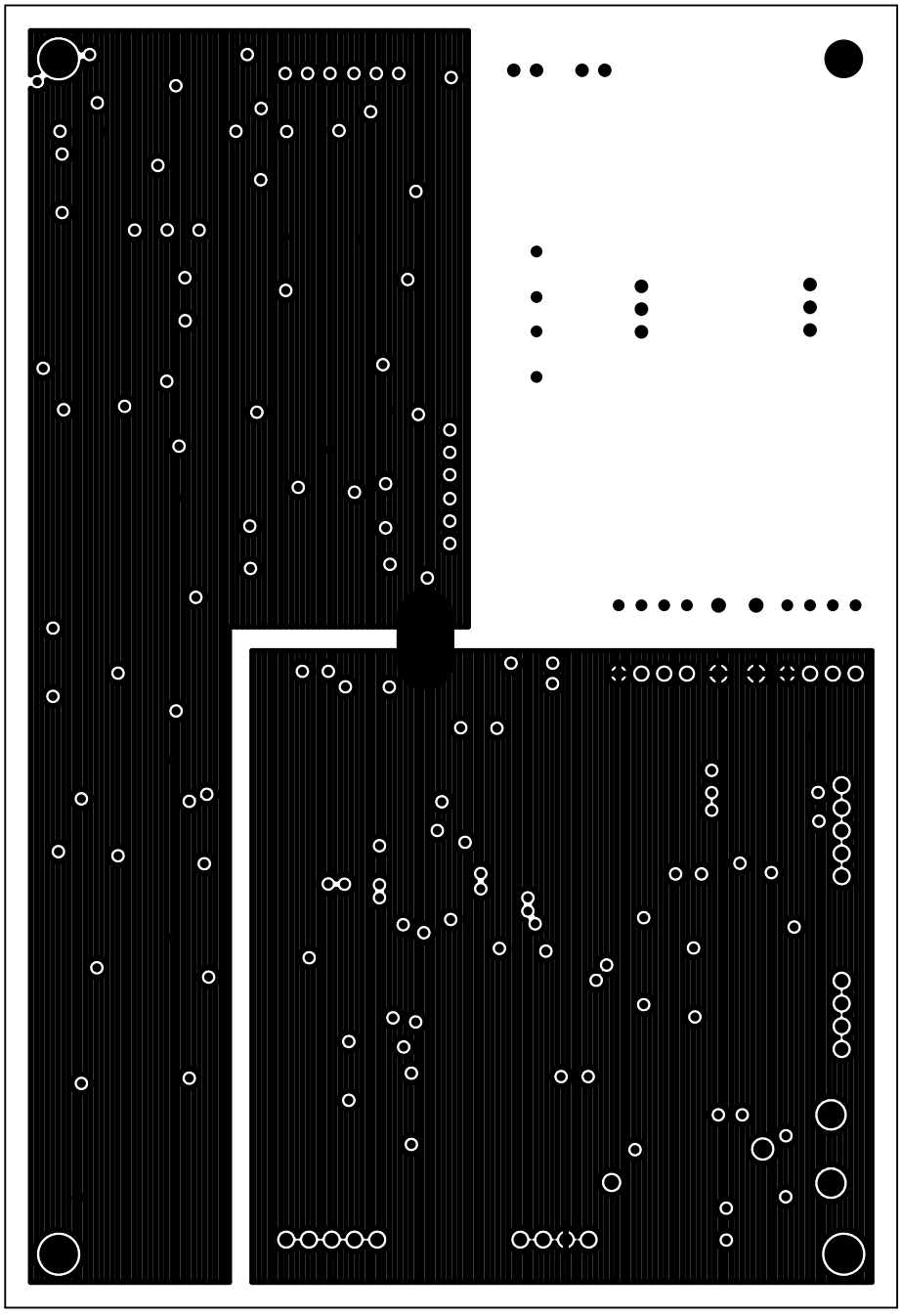
cam.zip
Layer: outerboard.cmp

28 Jan 2011,12:51 PM

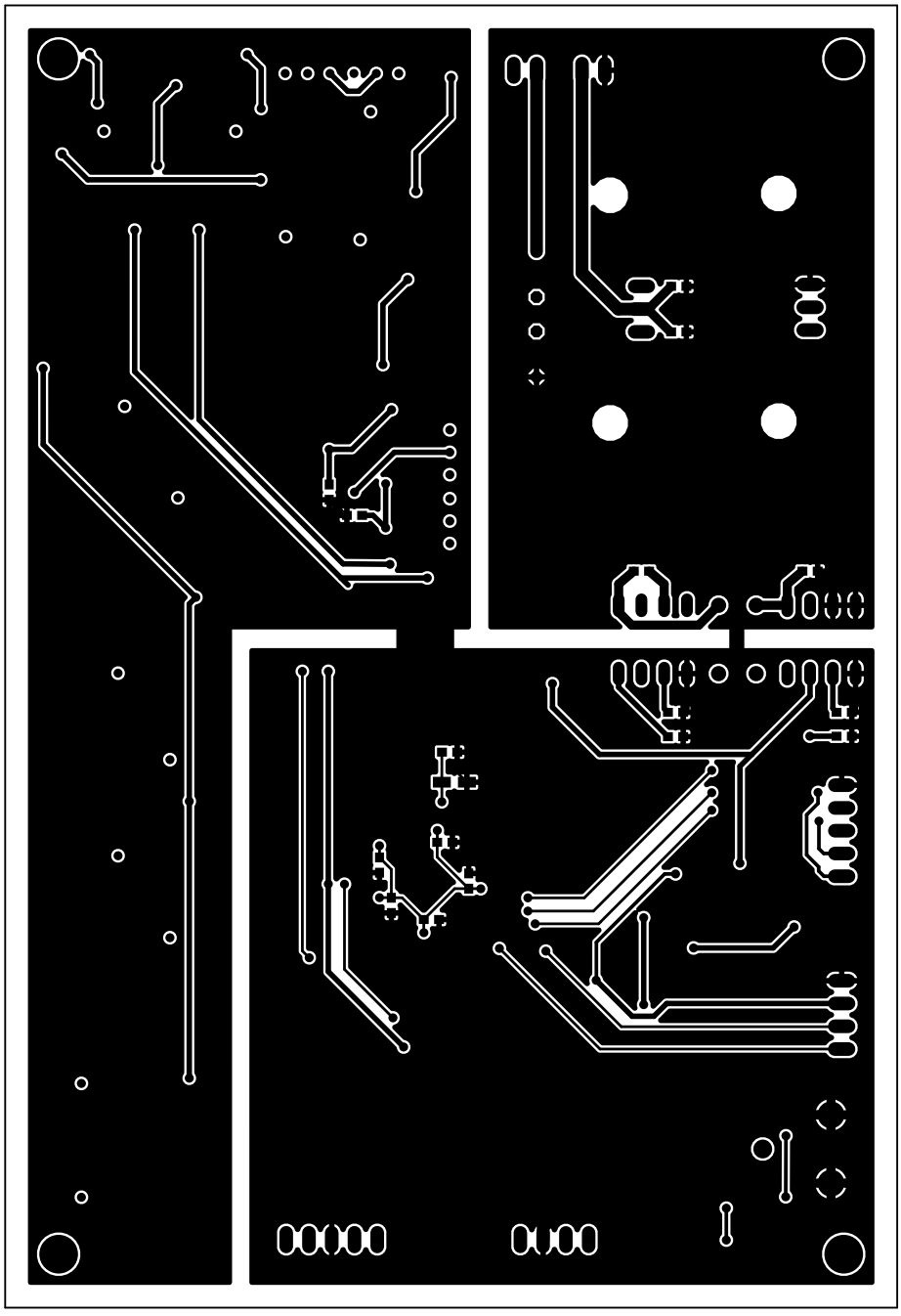
Layer 2 Copper



Layer 3 Copper



Layer 4 Copper



D.1.4 Previous Revision Bill Of Materials

Part	Value	Vendor	Vendor Part Number
+3.3V	TP-SMT	Digi-Key	5016KCT-ND
+5V	TP-SMT	Digi-Key	5016KCT-ND
+15V	TP-SMT	Digi-Key	5016KCT-ND
-15V	TP-SMT	Digi-Key	5016KCT-ND
ADC1	TP-SMT	Digi-Key	5016KCT-ND
ADC2	TP-SMT	Digi-Key	5016KCT-ND
AGND	TP-SMT	Digi-Key	5016KCT-ND
C1	0.1uF	Digi-Key	311-1366-1-ND
C2	100pF	Digi-Key	445-1281-1-ND
C3	4.7nF	Digi-Key	399-1088-1-ND
C4	100pF	Digi-Key	445-1281-1-ND
C5	4.7nF	Digi-Key	399-1088-1-ND
C6	0.01uF	Digi-Key	490-1512-1-ND
C7	0.01uF	Digi-Key	490-1512-1-ND
C8	0.01uF	Digi-Key	490-1512-1-ND
C9	1.0uF	Digi-Key	587-2400-1-ND
C10	1.0uF	Digi-Key	587-2400-1-ND
C11	1.0uF	Digi-Key	587-2400-1-ND
C12	1.0uF	Digi-Key	587-2400-1-ND
C13	82nF	Digi-Key	PCC1761CT-ND
C14	18pF	Digi-Key	399-1052-1-ND
C15	18pF	Digi-Key	399-1052-1-ND
C16	47pF	Digi-Key	445-1277-1-ND
C17	47pF	Digi-Key	445-1277-1-ND
CARRIER_LPF_OUT	TP-SMT	Digi-Key	5016KCT-ND
CARRIER_REF	TP-SMT	Digi-Key	5016KCT-ND
CARRIER_REF_AC	TP-SMT	Digi-Key	5016KCT-ND

Continued on next page

Part	Value	Vendor	Vendor Part Number
CB1	47uF	Digi-Key	495-1585-1-ND
CB2	47uF	Digi-Key	495-1585-1-ND
CB3	47uF	Digi-Key	495-1585-1-ND
CB4	47uF	Digi-Key	495-1585-1-ND
CB5	47uF	Digi-Key	718-1408-1-ND
CB6	0.1uF	Digi-Key	311-1366-1-ND
CB7	0.1uF	Digi-Key	311-1366-1-ND
CB8	0.1uF	Digi-Key	311-1366-1-ND
CB9	0.1uF	Digi-Key	311-1366-1-ND
CB10	0.1uF	Digi-Key	311-1366-1-ND
CB11	0.1uF	Digi-Key	311-1366-1-ND
CB12	0.1uF	Digi-Key	311-1366-1-ND
CB13	0.1uF	Digi-Key	311-1366-1-ND
CB14	0.1uF	Digi-Key	311-1366-1-ND
CB15	1.0uF	Digi-Key	587-2400-1-ND
CB16	0.1uF	Digi-Key	311-1366-1-ND
CB17	0.1uF	Digi-Key	311-1366-1-ND
CB18	0.1uF	Digi-Key	311-1366-1-ND
CB19	0.1uF	Digi-Key	311-1366-1-ND
CB20	0.1uF	Digi-Key	311-1366-1-ND
CB21	0.1uF	Digi-Key	311-1366-1-ND
CB22	0.1uF	Digi-Key	311-1366-1-ND
CB23	0.1uF	Digi-Key	311-1366-1-ND
CB24	0.1uF	Digi-Key	311-1366-1-ND
CB25	0.1uF	Digi-Key	311-1366-1-ND
CB26	0.1uF	Digi-Key	311-1366-1-ND
CB27	0.1uF	Digi-Key	311-1366-1-ND
CB28	0.1uF	Digi-Key	311-1366-1-ND

Continued on next page

Part	Value	Vendor	Vendor Part Number
CB29	0.1uF	Digi-Key	311-1366-1-ND
CB30	0.1uF	Digi-Key	311-1366-1-ND
CB31	0.1uF	Digi-Key	311-1366-1-ND
CB32	0.1uF	Digi-Key	311-1366-1-ND
CB33	0.1uF	Digi-Key	311-1366-1-ND
CB34	0.1uF	Digi-Key	311-1366-1-ND
CB35	0.1uF	Digi-Key	311-1366-1-ND
CB36	0.1uF	Digi-Key	311-1366-1-ND
CB37	0.1uF	Digi-Key	311-1366-1-ND
CB38	0.1uF	Digi-Key	311-1366-1-ND
CB39	0.1uF	Digi-Key	311-1366-1-ND
CB40	0.1uF	Digi-Key	311-1366-1-ND
CB41	10uF	Digi-Key	718-1123-1-ND
CB42	0.1uF	Digi-Key	311-1366-1-ND
CB43	0.1uF	Digi-Key	311-1366-1-ND
CB44	0.1uF	Digi-Key	311-1366-1-ND
CBS1	1.0uF	Digi-Key	587-2400-1-ND
CBS2	1.0uF	Digi-Key	587-2400-1-ND
COIL	MOLEX2	Digi-Key	929400E-01-36-ND
COIL_DRIVE_IN	TP-SMT	Digi-Key	5016KCT-ND
COIL_GND	TP-SMT	Digi-Key	5016KCT-ND
COIL_OUT	TP-SMT	Digi-Key	5016KCT-ND
COIL_POWER	MOLEX2	Digi-Key	WM4200-ND
COIL_VOLTAGE	TP-SMT	Digi-Key	5016KCT-ND
CSENSE1	.22uF	Digi-Key	BC1628-ND
CSENSE2	.22uF	Digi-Key	BC1628-ND
C_ERR1	0.015uF	Digi-Key	445-5189-1-ND
C_ERR2	0.015uF	Digi-Key	445-5189-1-ND

Continued on next page

Part	Value	Vendor	Vendor Part Number
D1	MUR120	UROP	
D2	MUR120	UROP	
D3	1N4148	Digi-Key	1N4148WTPMSCT-ND
D4	1N4148	Digi-Key	1N4148WTPMSCT-ND
D5	1N4148	Digi-Key	1N4148WTPMSCT-ND
D6	1N4148	Digi-Key	1N4148WTPMSCT-ND
D7	1N4148	Digi-Key	1N4148WTPMSCT-ND
D8	1N4148	Digi-Key	1N4148WTPMSCT-ND
D9	1N4148	Digi-Key	1N4148WTPMSCT-ND
DGND	TP-SMT	Digi-Key	5016KCT-ND
DRIVER_HI	IR2125PBF	UROP	
DRIVER_IN_HI	TP-SMT	Digi-Key	5016KCT-ND
DRIVER_IN_LO	TP-SMT	Digi-Key	5016KCT-ND
DRIVER_LO	IR2125PBF	UROP	
ERR_HI	TP-SMT	Digi-Key	5016KCT-ND
ERR_LO	TP-SMT	Digi-Key	5016KCT-ND
EXT_COIL_DRIVE	COAX	Digi-Key	A24539-ND
EXT_COIL_DRIVE_HI	TP-SMT	Digi-Key	5016KCT-ND
EXT_COIL_DRIVE_LO	TP-SMT	Digi-Key	5016KCT-ND
GAIN_OUT	TP-SMT	Digi-Key	5016KCT-ND
GATE_HI	TP-SMT	Digi-Key	5016KCT-ND
GATE_LO	TP-SMT	Digi-Key	5016KCT-ND
H1	PROGRAM	Digi-Key	929400E-01-36-ND
H2	UART	Digi-Key	929400E-01-36-ND
H3	OUTWAVES	Digi-Key	929400E-01-36-ND
HPF_OUT	TP-SMT	Digi-Key	5016KCT-ND

Continued on next page

Part	Value	Vendor	Vendor Part Number
IC1	DSPIC33FJ256MC710	Digi-Key	DSPIC33FJ256MC710-I/PF-ND
IC2	LT1028CS8	Digi-Key	LT1028CS8#PBF-ND
IC3	LT1028CS8	Digi-Key	LT1028CS8#PBF-ND
IC4	LT1028CS8	Digi-Key	LT1028CS8#PBF-ND
IC5	ADG211ASMD	Digi-Key	ADG211AKRZ-ND
IC6	AD620R	Digi-Key	AD620ARZ-ND
IC7	LT1037CS8	Digi-Key	LT1037CS8#PBF-ND
IC8	LF356D	Digi-Key	LF356M-ND
IC9	DAC7573	Digi-Key	296-15745-5-ND
IC10	LD117ADT-TR	Digi-Key	LM1117DT-3.3-ND
IC11	74HC14D	Digi-Key	MM74HC14M-ND
LADDER_OUT+	TP-SMT	Digi-Key	5016KCT-ND
LADDER_OUT-	TP-SMT	Digi-Key	5016KCT-ND
LED0		Digi-Key	754-1136-1-ND
LED1		Digi-Key	754-1136-1-ND
LED2		Digi-Key	754-1136-1-ND
LED3		Digi-Key	754-1136-1-ND
LED4		Digi-Key	754-1136-1-ND
LEVEL_SHIFT_OUT	TP-SMT	Digi-Key	5016KCT-ND
LPF_OUT	TP-SMT	Digi-Key	5016KCT-ND
MAIN_POWER	MOLEX4	Digi-Key	WM4202-ND
MCU_IN	TP-SMT	Digi-Key	5016KCT-ND
MIXER_IN_A	TP-SMT	Digi-Key	5016KCT-ND
MIXER_IN_B	TP-SMT	Digi-Key	5016KCT-ND
MIXER_OUT+	TP-SMT	Digi-Key	5016KCT-ND
MIXER_OUT-	TP-SMT	Digi-Key	5016KCT-ND
NO_CARRIER	TP-SMT	Digi-Key	5016KCT-ND

Continued on next page

Part	Value	Vendor	Vendor Part Number
P1	1k	Digi-Key	490-3007-ND
P2	10k	Digi-Key	490-3008-ND
P3	1k	Digi-Key	490-3007-ND
P4	10k	Digi-Key	490-3008-ND
PWM6	TP-SMT	Digi-Key	5016KCT-ND
PWM7	TP-SMT	Digi-Key	5016KCT-ND
Q1	IRF530V-HS	UROP	
Q2	IRF530V-HS	UROP	
Q4	8MHZ	Digi-Key	XC735CT-ND
R1	0	Digi-Key	311-0.0GRCT-ND
R2	0	Digi-Key	311-0.0GRCT-ND
R3	0	Digi-Key	311-0.0GRCT-ND
R4	0	Digi-Key	311-0.0GRCT-ND
R5	0	Digi-Key	311-0.0GRCT-ND
R6	0	Digi-Key	311-0.0GRCT-ND
R7	100k	Digi-Key	RMCF0603JT100KCT-ND
R8	1.3k	Digi-Key	311-1.3KGRCT-ND
R9	0	Digi-Key	311-0.0GRCT-ND
R10	0	Digi-Key	311-0.0GRCT-ND
R11	1.3k	Digi-Key	311-1.3KGRCT-ND
R12	6.8k	Digi-Key	RMCF0603JT6K80CT-ND
R13	0	Digi-Key	311-0.0GRCT-ND
R14	0	Digi-Key	311-0.0GRCT-ND
R15	1.3k	Digi-Key	311-1.3KGRCT-ND
R16	0	Digi-Key	311-0.0GRCT-ND
R17	0	Digi-Key	311-0.0GRCT-ND
R18	51	Digi-Key	311-51GRCT-ND
R19	51	Digi-Key	311-51GRCT-ND

Continued on next page

Part	Value	Vendor	Vendor Part Number
R20	51	Digi-Key	311-51GRCT-ND
R21	51	Digi-Key	311-51GRCT-ND
R22	0	Digi-Key	311-0.0GRCT-ND
R23	0	Digi-Key	311-0.0GRCT-ND
R24	1.3k	Digi-Key	311-1.3KGRCT-ND
R25	1.3k	Digi-Key	311-1.3KGRCT-ND
R26	1.3k	Digi-Key	311-1.3KGRCT-ND
R27	1.3k	Digi-Key	311-1.3KGRCT-ND
R28	1.3k	Digi-Key	311-1.3KGRCT-ND
R29	1.3k	Digi-Key	311-1.3KGRCT-ND
R30	0	Digi-Key	311-0.0GRCT-ND
R31	0	Digi-Key	311-0.0GRCT-ND
R32	5.1k	Digi-Key	311-5.1KGRCT-ND
R33	0	Digi-Key	311-0.0GRCT-ND
R34	1.3k	Digi-Key	311-1.3KGRCT-ND
R35	0	Digi-Key	311-0.0GRCT-ND
R36	100k	Digi-Key	311-100KGRCT-ND
R37	100	Digi-Key	311-100GRCT-ND
R38	0	Digi-Key	311-0.0GRCT-ND
R39	1.3k	Digi-Key	311-1.3KGRCT-ND
R40	2.7k	Digi-Key	311-2.7KGRCT-ND
R41	1.3k	Digi-Key	311-1.3KGRCT-ND
R42	2.7k	Digi-Key	311-2.7KGRCT-ND
R43	0	Digi-Key	311-0.0GRCT-ND
R44	1.3k	Digi-Key	311-1.3KGRCT-ND
R45	0	Digi-Key	311-0.0GRCT-ND
R46	1.3k	Digi-Key	311-1.3KGRCT-ND
R47	5.1k	Digi-Key	311-5.1KGRCT-ND

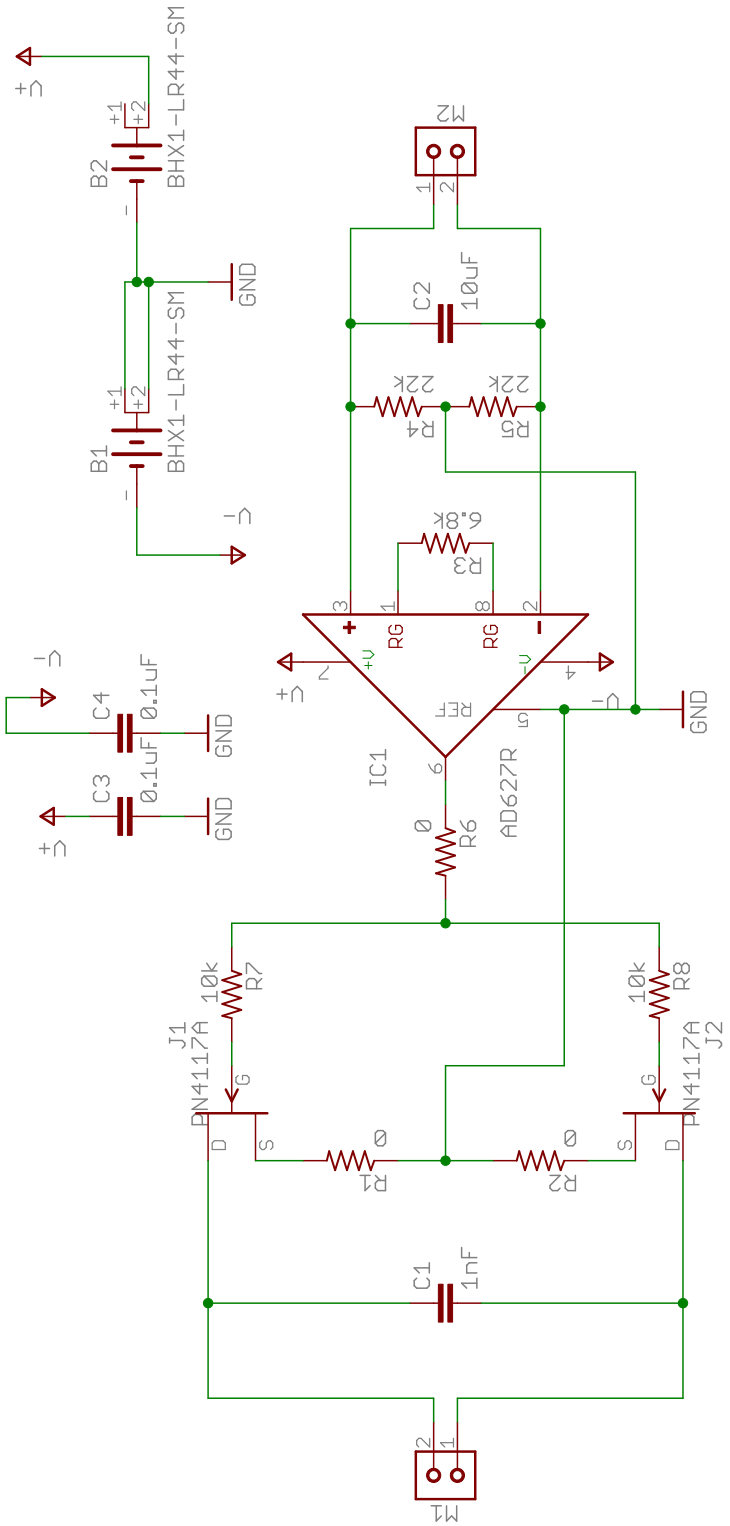
Continued on next page

Part	Value	Vendor	Vendor Part Number
R48	5.1k	Digi-Key	311-5.1KGRCT-ND
R49	100	Digi-Key	311-100GRCT-ND
R50	100	Digi-Key	311-100GRCT-ND
R51	100	Digi-Key	311-100GRCT-ND
R52	100	Digi-Key	311-100GRCT-ND
R53	100	Digi-Key	311-100GRCT-ND
R54	0	Digi-Key	311-0.0GRCT-ND
R55	0	Digi-Key	311-0.0GRCT-ND
R56	270	Digi-Key	311-270GRCT-ND
R57	270	Digi-Key	311-270GRCT-ND
R58	0	Digi-Key	311-0.0GRCT-ND
R59	0	Digi-Key	311-0.0GRCT-ND
RG1	10	Digi-Key	541-10SACT-ND
RG2	10	Digi-Key	541-10SACT-ND
RSENSE	1.3k	Digi-Key	311-1.3KGRCT-ND
S1	4-40STANDOFF	Digi-Key	1808K-ND
S2	4-40STANDOFF	Digi-Key	1808K-ND
S3	4-40STANDOFF	Digi-Key	1808K-ND
S4	4-40STANDOFF	Digi-Key	1808K-ND
SENSE	TP-SMT	Digi-Key	5016KCT-ND
SUBTRACTOR-	TP-SMT	Digi-Key	5016KCT-ND

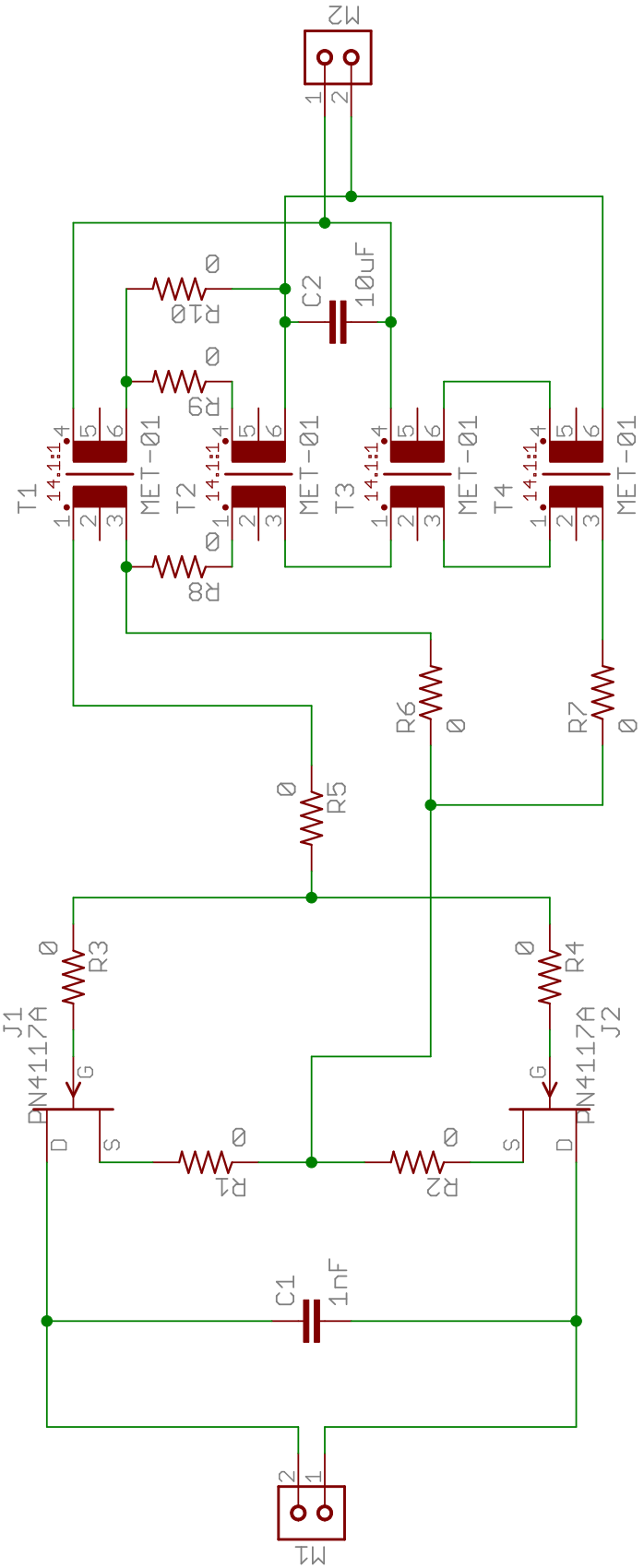
D.2 Current-Sense Circuitry

D.2.1 PCB Schematics

Instrumentation Amplifier Design

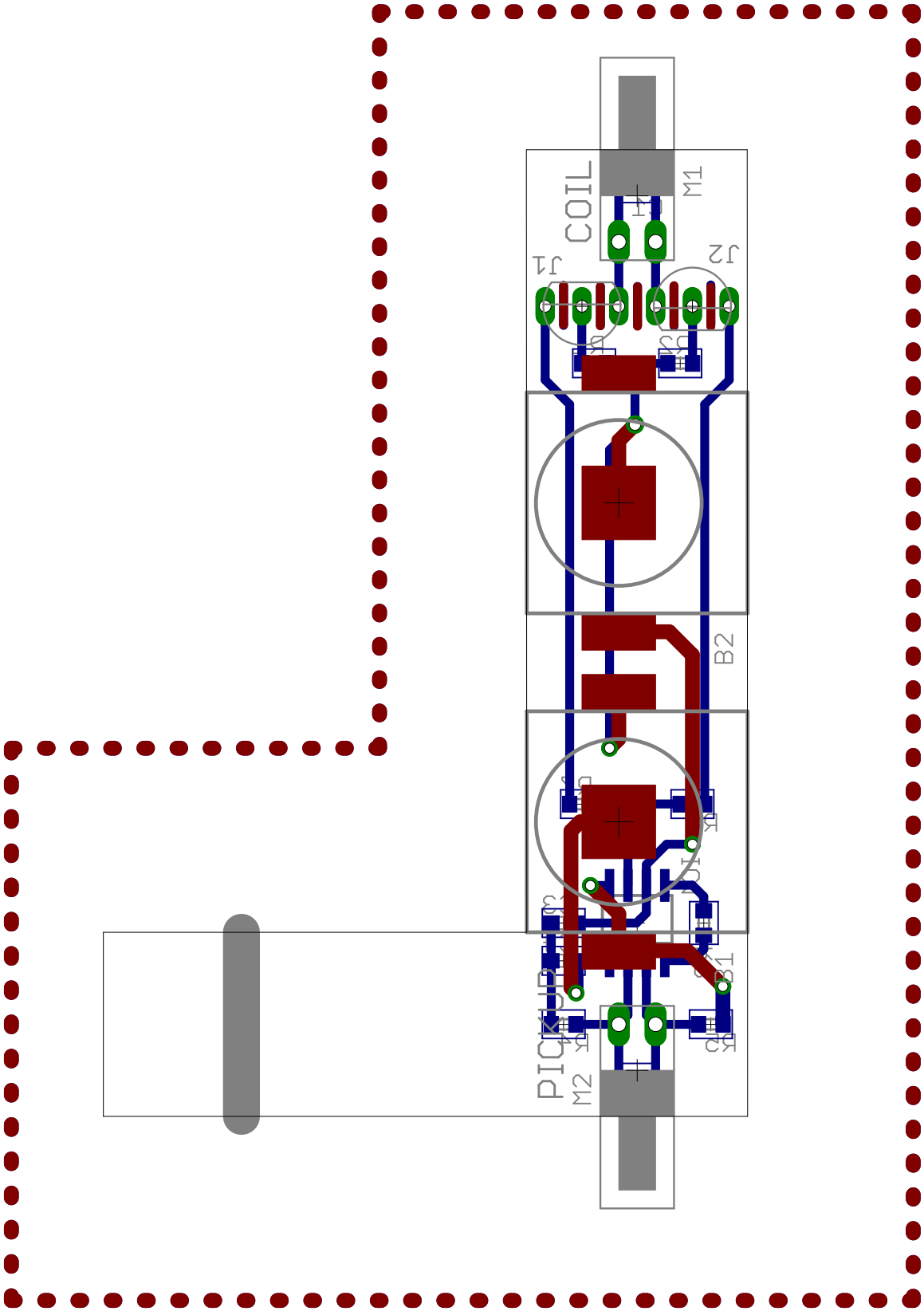


Audio Transformer Design

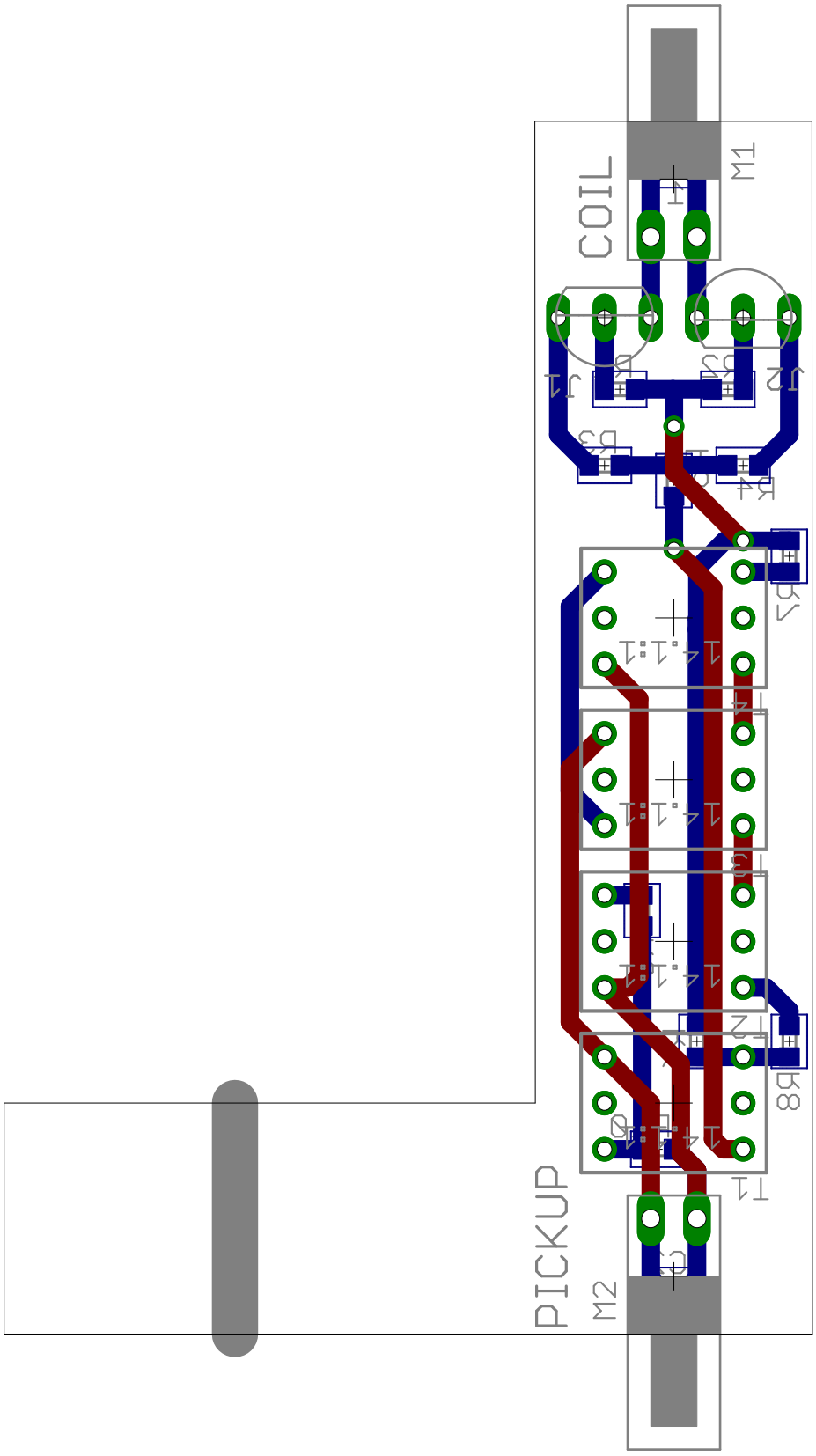


D.2.2 PCB Layout

Instrumentation Amplifier Design



Audio Transformer Design



D.2.3 PCB Bill Of Materials

Instrumentation Amplifier Design

Part	Value	Vendor	Vendor Part Number
B1	BHX1-LR44-SM	Digi-Key	BHX1-LR44-SM-ND
B2	BHX1-LR44-SM	Digi-Key	BHX1-LR44-SM-ND
C1	1nF	Digi-Key	445-5371-1-ND
C2	10uF	Digi-Key	490-3896-1-ND
C3	0.1uF	Digi-Key	478-6208-1-ND
C4	0.1uF	Digi-Key	478-6208-1-ND
IC1	AD627R	Digi-Key	AD627ARZ- R7CT-ND
J1	PN4117A	Mouser	512-PN4117AD26Z
J2	PN4117A	Mouser	512-PN4117AD26Z
M1	MOLEX2H	Digi-Key	WM4300-ND
M2	MOLEX2H	Digi-Key	WM4300-ND
R1	1.3k	Digi-Key	311-1.3KGRCT-ND
R2	1.3k	Digi-Key	311-1.3KGRCT-ND
R3	6.8k	Digi-Key	311-6.8KGRCT- ND
R4	22k	Digi-Key	311-20KGRCT-ND
R5	22k	Digi-Key	311-20KGRCT-ND
R6	0	Digi-Key	311-0.0GRCT-ND
R7	10k	Digi-Key	311-10KGRCT- ND
R8	10k	Digi-Key	311-10KGRCT- ND

Audio Transformer Design

Part	Value	Vendor	Vendor Part Number
C1	1nF	Digi-Key	445-5371-1-ND
C2	10uF	Digi-Key	490-3896-1-ND
J1	PN4117A	Mouser	512-PN4117AD26Z
J2	PN4117A	Mouser	512-PN4117AD26Z
M1	MOLEX2H	Digi-Key	WM4300-ND
M2	MOLEX2H	Digi-Key	WM4300-ND
R1	1.3k	Digi-Key	311-1.3KGRCT-ND
R2	1.3k	Digi-Key	311-1.3KGRCT-ND
R3	0	Digi-Key	311-0.0GRCT-ND
R4	0	Digi-Key	311-0.0GRCT-ND
R5	0	Digi-Key	311-0.0GRCT-ND
R6	0	Digi-Key	311-0.0GRCT-ND
R7	0	Digi-Key	311-0.0GRCT-ND
R8	0	Digi-Key	311-0.0GRCT-ND
R9	0	Digi-Key	311-0.0GRCT-ND
R10	0	Digi-Key	311-0.0GRCT-ND
T1	MET-01	Digi-Key	MT4143-ND
T2	MET-01	Digi-Key	MT4143-ND
T3	MET-01	Digi-Key	MT4143-ND
T4	MET-01	Digi-Key	MT4143-ND

Appendix E

Software

This appendix contains source code listings for:

- The microprocessor on the signal conditioning electronics board,
- A Python program for communicating with the microprocessor,
- MATLAB simulations and scripts used to generate figures for this thesis.

E.1 Signal Conditioning Electronics

E.1.1 dsPIC33FJ256MC710 Microcontroller

types.h

```
1  /*** types.h ***/
2
3  /* Exact-width types. WG14/N843 C99 Standard, Section 7.18.1.1 */
4  typedef signed   char int8_t;
5  typedef signed   int  int16_t;
6  typedef signed   long int32_t;
7  typedef unsigned char uint8_t;
8  typedef unsigned int  uint16_t;
9  typedef unsigned long uint32_t;
```

delays.h

```
1  /*** delays.h ***/
2
3  /* delay_us(x) and delay_ms(x) for C30 */
4  #ifndef __DELAYS_H
5  #define delay_us(x) __delay32(((x*FCY)/1000000L)) // delays x us
6  #define delay_ms(x) __delay32(((x*FCY)/1000L))    // delays x ms
7  #define delay_s(x)  __delay32((x*FCY))            // delays x s
8  #define __DELAYS_H
9  #endif
```

main.h

```
1  /*** main.h ***/
2
3  #if defined(__dsPIC33F__)
4  #include "p33Fxxxx.h"
5  #elif defined(__PIC24H__)
6  #include "p24Hxxxx.h"
7  #endif
8
9  #include <libpic30.h>
10 #include "delays.h"
11 #include "types.h"
```

main.c

```
/*** main.c ***/

/*
 *  MIT HomeNILM Revision 3 Firmware
 *  Written by Daniel Vickery (drv@alum.mit.edu)
 *
 *  with help from:
 *    John Cooley (jjcooley@alum.mit.edu)
 *    Steven Leeb (sbleeb@mit.edu)
 *
 *  August, 2011
 *
 */

#include "main.h"
#include "serial.h"
#include "oc_control.h"
#include "adc.h"
#include "autocal.h"
#include "leds.h"

/* Initial OC Module Parameters */
#define INIT_FREQ        20   // Start-up coil drive frequency
#define INIT_CR_PHASE    0    // Start-up carrier-supression reference phase
#define INIT_MIXER_PHASE 75   // Start-up mixer LO phase
#define INIT_ST_DELAY    200  // Start-up 1/2-bridge shoot-thru delay

/*** CONFIGURATION BITS: ***/

// Use external primary oscillator (crystal) with PLL.
// This should run at 50MHz (N1 = 2, N2 = 4, M = 50 by default):
_FOSCSEL(FNOSC_PRIPLL);

// Clock Switching is disabled and Fail Safe Clock Monitor is disabled
// Primary Oscillator Mode: XT Oscillator
_FOSC(FCKSM_CSDCMD & POSCMD_XT);

_FWDT(FWDTEN_OFF); // Disable Watchdog Timer.
_FPOR(FPWRT_PWR1); // Turn off the power-up timers.
_FGS(GCP_OFF);     // Disable Code Protection

/*** MAIN PROGRAM: ***/

int main (void) {
```

```
45    /* Set the stage. */
46    initLEDs();
47    initUART1();
48    initTimers();
49    initOCModules();
50    initADC();
51
52    /* Set initial OC module parameters. */
53    carrier_frequency = INIT_FREQ;
54    carrier_ref_phase = INIT_CR_PHASE;
55    mixer_phase = INIT_MIXER_PHASE;
56    shoot_thru_delay = INIT_ST_DELAY;
57
58    /* Start the show. */
59    updateOCModules();
60    updateOCModules();
61
62    /* Initialize memory for incoming data packets. */
63    uint8_t id_byte;
64    uint8_t msb;
65    uint8_t lsb;
66
67    /* Enter Main Loop */
68    while(1) {
69      /*
70       * This main loop does nothing but read in data packets
71       * from the serial port and update the waveforms accordingly.
72       */
73
74      // Get first byte (ID byte):
75      id_byte = getIncomingData();
76
77      // Execute response depending on ID byte:
78      if (id_byte == 'f') { // Frequency Change
79        msb = getIncomingData();
80        lsb = getIncomingData();
81        carrier_frequency = lsb + (msb << 8);
82        // Restart waveforms with new parameters:
83        updateOCModules();
84        updateOCModules();
85      }
86
87      else if (id_byte == 'c') { // Carrier Reference Phase Change
88        msb = getIncomingData();
89        lsb = getIncomingData();
```

```
      carrier_ref_phase = lsb + (msb << 8);
      // Restart waveforms with new parameters:
      updateOCModules();
      updateOCModules();
    }

    else if (id_byte == 'm') { // Mixer Phase Change
      msb = getIncomingData();
      lsb = getIncomingData();
      mixer_phase = lsb + (msb << 8);
      // Restart waveforms with new parameters:
      updateOCModules();
      updateOCModules();
    }

    else if (id_byte == 'd') { // Shoot-Thru Delay Change
      msb = getIncomingData();
      lsb = getIncomingData();
      shoot_thru_delay = lsb + (msb << 8);
      // Restart waveforms with new parameters:
      updateOCModules();
      updateOCModules();
    }

    else if (id_byte == 'a') { // Auto-Calibrate Mixer Phase
      // Run auto-calibration algorithm once on low resolution (for speed)
      // and again at high-resolution (for precision)
      autoCalPhase(20); // First pass
      autoCalPhase(2);  // Second pass
    }

    else { // Unknown ID byte
      // Forget about it.
    }
  }
}
```

adc.h

```
1  /*** adc.h ***/
2
3  /* Function Definitions */
4  void initADC(void);
5  uint16_t getADCData(void);
```

adc.c

```
/*** adc.c ***/
/*
 *  Utility functions for interfacing with the ADC(s).
 */

#include "main.h"
#include "adc.h"
#include "oc_control.h"

/*** ADC Configuration Recipe (From the dsPIC33 Family Reference):

1. Select 10-bit or 12-bit mode (ADxCON1<10>)
2. Select voltage reference source to match expected range on analog inputs (ADxCON2<15:13>)
3. Select the analog conversion clock to match desired data rate with processor clock (ADxCON3<7:0>)
4. Select port pins as analog inputs (ADxPCFGH<15:0> and ADxPCFGL<15:0>)
5. Determine how inputs will be allocated to Sample/Hold channels (ADxCHS0<15:0> and ADxCHS123<15:0>)
6. Determine how many Sample/Hold channels will be used (ADxCON2<9:8>, ADxPCFGH<15:0> and ADxPCFGL<15:0>)
7. Determine how sampling will occur (ADxCON1<3>, ADxCSSH<15:0> and ADxCSSL<15:0>)
8. Select Manual or Auto Sampling
9. Select conversion trigger and sampling time.
10. Select how conversion results are stored in the buffer (ADxCON1<9:8>)
11. Select interrupt rate or DMA buffer pointer increment rate (ADxCON2<9:5>)
12. Select the number of samples in DMA buffer for each ADC module input (ADxCON4<2:0>)
13. Select the data format
14. Configure ADC interrupt (if required):
   Clear ADxIF bit
   Select interrupt priority (ADxIP<2:0)
   Set ADxIE bit
15. Configure DMA channel (if needed)
16. Turn on ADC module (ADxCON1<15>)

***/

void initADC(void) {
  /*
     - Initialize ADC Module -

     Configures ADC to use CH0 connected to input AN1 (Input RB1, Pin 24)
     Uses 10-bit Mode.
     AVdd (3.3V) and AVss (GND) are references for the ADC.
     The ADC is triggered manually from code.  No interrupts.
     The ADC automatically samples for 960ns (8 ADC clock periods) before beginning conversion.
  */

```

```
45    AD1CON1bits.AD12B = 0;    // 10-bit mode
46    AD1CON2bits.VCFG = 0;     // Use Avdd and Avss as high and low voltage references
47    AD1CON3bits.ADCS = 2;     // Analog Module Clock Period TAD = (ADCS+1)*TCY = 120ns
48    AD1CHS0bits.CH0SA = 1;     // Use AN1 for positive analog input on CH0
49    AD1CHS0bits.CH0NA = 0;     // Use Vref- (GND) for negative analog input on CH0
50    AD1CON1bits.SSRC = 0;
51
52    IFS0bits.AD1IF = 0;       // Clear the A/D interrupt flag bit
53    IEC0bits.AD1IE = 0;       // Do Not Enable A/D interrupt
54
55    AD1CON1bits.ADON = 1;     // Turn on the A/D converter
56  }
57
58  uint16_t getADCData(void) {
59    /*
60      Run ADC for one sample.
61      Return the sample.
62    */
63
64    uint16_t adc_value;
65
66    // Start Sampling:
67    AD1CON1bits.SAMP = 1;
68    // Wait 2us to collect sample on input capacitor:
69    delay_us(2);
70    // Stop sampling and begin A/D conversion:
71    AD1CON1bits.SAMP = 0;
72
73    // Wait until A/D conversion finishes:
74    while (!AD1CON1bits.DONE);
75
76    // Return data from ADC buffer:
77    adc_value = ADC1BUF0;
78    return adc_value;
79  }
```

autocal.h

```
/*** autocal.h ***/

/* Function Definitions */
void autoCalPhase(uint8_t phase_res);
```

autocal.c

```
/*** autocal.c ***/
/*
 *  Sample LPF'd, demodulated signal at ADC.
 *  Use it as a heuristic to set mixer reference phase via hill-climbing.
 */

#include "main.h"
#include "adc.h"
#include "oc_control.h"
#include "serial.h"
#include "autocal.h"
#include "leds.h"

// Macros for hill-climbing directions (left or right phase shift):
#define LEFT -1
#define RIGHT 1

// This function is intended for use only by autoCalPhase():
void shiftRefPhase(int8_t phase_delta);

void autoCalPhase(uint8_t phase_res) {
  /*
    Uses the DC output of the differential low-pass filter as a metric to
    match the carrier reference phase with the incoming modulated signal.

    In each iteration, this function samples the DC level from the ADC at
    one PHASE_RES unit above and below the current phase.  It then "hill-climbs"
    or shifts the phase in the direction of increasing DC level until a
    maximum is found.
   */

  int8_t climb_direction;   // Phase Hill-Climbing Direction
  uint16_t adc_samples[3];  // ADC Sample Data

  while(1) {
    // Get ADC samples at phase, phase+1, and phase-1:
    shiftRefPhase(-phase_res); // Step back to phase-1
    adc_samples[0] = getADCData();

    shiftRefPhase(phase_res); // Step forward to current phase
    adc_samples[1] = getADCData();

    shiftRefPhase(phase_res); // Step forward to phase+1
    adc_samples[2] = getADCData();
```

```
45
46      shiftRefPhase(-phase_res); // Step back to current phase
47
48      // Find the phase direction in which ADC samples increase:
49      if (adc_samples[2] > adc_samples[1])
50        climb_direction = RIGHT;
51
52      else if (adc_samples[0] > adc_samples[1])
53        climb_direction = LEFT;
54
55      // Return when we find ourselves at a maximum:
56      else return;
57
58      // Move phase in the direction of increasing ADC samples:
59      shiftRefPhase(climb_direction * phase_res);
60    }
61  }
62
63  void shiftRefPhase(int8_t phase_delta) {
64    /*
65      Shifts the phase of the mixer reference signal by phase_delta.
66    */
67
68    // Account for 359-0 degree wraparounds:
69    if (mixer_phase + phase_delta < 0)
70      mixer_phase = mixer_phase + phase_delta + 360;
71    else if (mixer_phase + phase_delta > 359)
72      mixer_phase = mixer_phase + phase_delta - 360;
73    else
74      mixer_phase = mixer_phase + phase_delta;
75
76    // Reset and reconfigure timers to run with new phase setting:
77    updateOCModules();
78    updateOCModules(); // Why this needs to be run twice is a mystery to me.
79
80    // Wait for things to settle before we do anything else:
81    delay_ms(10);
82
83    return;
84  }
```

leds.h

```
1  /*** leds.h ***/
2
3  /* Function Definitions */
4  void initLEDs (void);
5  void setLED (uint8_t led, uint8_t new_state);
6  void toggleLED (uint8_t led);
```

leds.c

```
/*** leds.c ***/
/*
 *  Control debug LEDs
 */

#include "main.h"
#include "leds.h"

uint8_t led_state = 0x00;

void initLEDs (void) {
  // Set all Port E pins as outputs, keep LEDs off (output high):
  TRISE = 0x00;
  PORTE = 0xFF;
}

void setLED (uint8_t led, uint8_t new_state) {
  // Select bit in PORTE byte to change:
  uint8_t state_change = 0x01;
  while (led-- != 0)
    state_change = state_change << 1;

  // Use AND to zero an active bit, use OR to activate a zeroed bit:
  if (new_state == 0)
    led_state = !(state_change | !led_state);
  else
    led_state = state_change | led_state;

  // Reset PORTE register with new state:
  PORTE = led_state ^ 0xFF;
  return;
}

void toggleLED (uint8_t led) {
  // Select bit in PORTE byte to change:
  uint8_t state_change = 0x01;
  while (led-- != 0)
    state_change = state_change << 1;

  led_state ^= state_change;

  // Reset PORTE register with new state:
  PORTE = led_state ^ 0xFF;
  return;
```

```
45 }
```

oc_control.h

```
/*** oc_control.h ***/

#define FOSC     50000000LL  // clock frequency in Hz
#define FCY      (FOSC/2)    // MCU is running at FCY IPS

/* Function Definitions */
void initTimers(void);
void initOCModules(void);
void updateOCModules(void);

/* Global Variable Declarations */
// Coil drive frequency in kHz:
extern uint16_t carrier_frequency;
// Carrier supression reference phase (0-359):
extern uint16_t carrier_ref_phase;
// Mixer LO phase (0-359):
extern int16_t mixer_phase;
// Delay time between half-bridge gate signals (nanoseconds):
extern uint16_t shoot_thru_delay;
```

oc_control.c

```
/*** oc_control.c ***/
/*
 *  Adjust frequency and phase of the carrier,
 *  the carrier-surpression reference,
 *  and mixer control signals.
 */

#include "main.h"
#include "oc_control.h"
#include "leds.h"

/* GLOBALS */
uint16_t carrier_frequency;  // Coil drive frequency in kHz
uint16_t carrier_ref_phase;  // Carrier-supression reference phase (0-359)
int16_t mixer_phase;         // Mixer LO phase (0-359)
uint16_t shoot_thru_delay;   // Delay time between half-bridge gate signals (ns)

void initTimers(void) {
  /*
   *   Boilerplate code to set up all the configuration bits
   *   for the timers used by the OC modules.
   */

  /* Configure Timers: */
  // Disable Timer:
  T2CONbits.TON = 0;
  // Select Internal Instruction Cycle Clock (Fcy = 25MHz):
  T2CONbits.TCS = 0;
  // Disable Gated Timer Mode:
  T2CONbits.TGATE = 0;
  // Select 1:1 Prescaler:
  T2CONbits.TCKPS = 0b00;
  // Clear Timer Register:
  TMR2 = 0x00;

  /* Using Timer3 at switch frequency */
  // Disable Timer:
  T3CONbits.TON = 0;
  // Select Internal Instruction Cycle Clock (Fcy = 25MHz):
  T3CONbits.TCS = 0;
  // Disable Gated Timer Mode:
  T3CONbits.TGATE = 0;
  // Select 1:1 Prescaler:
  T3CONbits.TCKPS = 0b00;
```

```
45    // Clear Timer Register:
46    TMR3 = 0x00;
47  }
48
49  void initOCModules (void) {
50    /*
51     *   Boilerplate code to set up configuration bits
52     *   for the OC modules we use.
53     *
54     *   OC1 = High-Side Coil Drive
55     *   OC2 = Low-Side Coil Drive
56     *   OC3 = Mixer Reference
57     *   OC4 = Mixer Reference (Inverse)
58     *   OC5 = Carrier Reference For Active Carrier Supression
59     *
60     */
61
62    // Disable Output Compare Modules:
63    OC1CONbits.OCM = 0b000;
64    OC2CONbits.OCM = 0b000;
65    OC3CONbits.OCM = 0b000;
66    OC4CONbits.OCM = 0b000;
67    OC5CONbits.OCM = 0b000;
68    // Select Timer3 as Output Compare Time Base for Coil Drive:
69    OC1CONbits.OCTSEL = 1;
70    OC2CONbits.OCTSEL = 1;
71    // Select Timer2 as Output Compare Time Base for Reference Signals:
72    OC3CONbits.OCTSEL = 0;
73    OC4CONbits.OCTSEL = 0;
74    OC5CONbits.OCTSEL = 0;
75
76    return;
77  }
78
79  void updateOCModules(void) {
80    /*
81     *   Behavior:
82     *     Shuts down and restarts timer and OC circuits
83     *     with new frequency/phase/delay parameters from globals.
84     */
85
86    /* Calculate timer period that corresponds to new frequency (in kHz) */
87    uint16_t timer2_period = (12500 / carrier_frequency) - 1;
88    uint16_t timer3_period = (2 * timer2_period) + 1;
89    /* Calculate new mixer output compare match value */
```

```
90    uint16_t mixer_match =
91      (((uint32_t)mixer_phase * (uint32_t)timer2_period) / 359) * 2;
92    /* Calculate new carrier reference compare match value */
93    uint16_t carrier_ref_match =
94      (((uint32_t)carrier_ref_phase * (uint32_t)timer2_period) / 359) * 2;
95
96    /* Stop and restart timer with new OC parameters: */
97    // Turn Timers Off:
98    T2CONbits.TON = 0;
99    T3CONbits.TON = 0;
100
101   // Reset Timer Registers:
102   TMR2 = 0x00;
103   TMR3 = 0x00;
104
105   // Set New Timer Periods:
106   PR2 = timer2_period;
107   PR3 = timer3_period;
108
109   // Disable Output Compare Modules:
110   OC1CONbits.OCM = 0b000;
111   OC2CONbits.OCM = 0b000;
112   OC3CONbits.OCM = 0b000;
113   OC4CONbits.OCM = 0b000;
114   OC5CONbits.OCM = 0b000;
115
116   // Define Initial State for Mixer Reference Pins:
117   if (mixer_match > timer2_period) {
118     mixer_match = mixer_match - timer2_period;
119     OC3CONbits.OCM = 0b010;   // HIGH
120     OC4CONbits.OCM = 0b001;   // LOW
121     if (mixer_match == 0) {
122       OC3CONbits.OCM = 0b001; // LOW
123       OC4CONbits.OCM = 0b010; // HIGH
124     }
125   }
126   else {
127     OC3CONbits.OCM = 0b001;   // LOW
128     OC4CONbits.OCM = 0b010;   // HIGH
129     if (mixer_match == 0) {
130       OC3CONbits.OCM = 0b010; // HIGH
131       OC4CONbits.OCM = 0b001; // LOW
132     }
133   }
134
```

```
135   // Define Initial State for Carrier Reference Pin:
136   if (carrier_ref_match > timer2_period) {
137     carrier_ref_match = carrier_ref_match - timer2_period;
138     if (carrier_ref_match == 0)
139       OC5CONbits.OCM = 0b001; // LOW
140     else
141       OC5CONbits.OCM = 0b010; // HIGH
142   }
143   else {
144     if (carrier_ref_match == 0)
145       OC5CONbits.OCM = 0b010; // HIGH
146     else
147       OC5CONbits.OCM = 0b001; // LOW
148   }
149
150
151   // Set Initial Output Compare Match Values:
152   OC1R  = 0;                                          // OC1R * 40ns = Shoot-thru delay time
153   OC1RS = (timer3_period / 2) - (shoot_thru_delay / 40);    // Gate drive should be 50% duty
154   OC2R  = OC1RS + (shoot_thru_delay / 40);                  // Add equal delay to low-side transition
155   OC2RS = timer3_period - (shoot_thru_delay / 40);          // Gate drive ends with timer rollover.
156   OC3R  = mixer_match;
157   OC4R  = mixer_match;
158   OC5R  = carrier_ref_match;
159
160   // Set Output Compare Modes:
161   OC1CONbits.OCM = 0b101; // Continuous Pulse
162   OC2CONbits.OCM = 0b101; // Continuous Pulse
163   OC3CONbits.OCM = 0b011; // Toggle
164   OC4CONbits.OCM = 0b011; // Toggle
165   OC5CONbits.OCM = 0b011; // Toggle
166
167   // Turn Timers On:
168   T3CONbits.TON = 1;
169   T2CONbits.TON = 1;
170
171   return;
172 }
```

serial.h

```
1  /*** serial.h ***/
2
3  /* Function Definitions */
4  void initUART1(void);
5  uint8_t getIncomingData (void);
6  void sendUARTData(uint8_t outgoing_byte);
```

serial.c

```
/*** serial.c ***/
/*
 *  Run the UART for computer-control.
 */

#include "main.h"
#include "oc_control.h"
#include "leds.h"

#define BAUDRATE 115200
#define BRGVAL   ((FCY/BAUDRATE)/16)-1

void initUART1 (void) {
  /* Configure Receive-Only Serial Port */

  // Configure Protocol:
  U1MODEbits.STSEL = 0; // 1 Stop-Bit
  U1MODEbits.PDSEL = 0; // No Parity, 8 Data-Bits
  U1MODEbits.ABAUD = 0; // Autobaud Disabled
  U1BRG = BRGVAL;       // Baud Rate @ 115200

  // Enable UART:
  U1MODEbits.UARTEN = 1;

  // Enable UART TX (For Debugging):
  U1STAbits.UTXEN = 1;
}

uint8_t getIncomingData (void) {
  uint8_t incoming_byte;

  // Wait for new data byte available in receive buffer:
  while (!U1STAbits.URXDA) continue;

  // Get new byte:
  incoming_byte = U1RXREG;

  // Fix any buffer overflows (can occur after spurious serial input):
  if (U1STAbits.OERR) U1STAbits.OERR = 0;

  return incoming_byte;
}

void sendUARTData(uint8_t outgoing_byte) {
```

```
45    // Wait until there is space in the TX buffer:
46    while(U1STAbits.UTXBF);
47
48    // Pop the outgoing data into the transmit buffer:
49    U1TXREG = outgoing_byte;
50
51    return;
52  }
```

E.1.2 Python Control Interface

homenilm_ctl.py

```
1  ####################################
2  # HomeNILM Revision 3              #
3  # Demodulator Board Control Script #
4  # Daniel Vickery - DRV@ALUM.MIT.EDU #
5  # 2011                             #
6  ####################################
7
8  import serial
9  import sys
10 import struct
11
12 if len(sys.argv) != 2:
13     sys.exit("Usage: homenilm_ctl.py serial_device")
14
15 try:
16     ser = serial.Serial(sys.argv[1], 115200, timeout=22)
17 except serial.SerialException:
18     sys.exit("That serial device was not OK.")
19
20 print("\nHomeNILM Revision 3\nDaniel Vickery, John Cooley, Steven Leeb\n2011")
21 print("\n\nOPTIONS:")
22 print("\n(f) Set carrier frequency.")
23 print("\n(c) Set carrier reference phase for active carrier supression.")
24 print("\n(m) Set mixer LO phase.")
25 print("\n(d) Set dead time for 1/2 bridge coil drive.")
26 print("\n(a) Auto-calibrate carrier reference phase.")
27 print("\n(q) Quit program.")
28 print("\n(?) Display this menu.")
29
30 while True:
31
32     command = raw_input("\nEnter command selection: ")
33
34     if command == "f":
35         while True:
36             freq = raw_input("Enter new frequency in kHz: ")
37             try:
38                 freq = int(freq)
39             except ValueError:
40                 print("Frequency must be a positive integer.")
41                 continue
42             if freq < 1 or freq > 1000:
```

```
43                print("Frequency out of range.")
44                continue
45            # construct packet, network byte order:
46            outgoing = struct.pack("!cH",command,freq)
47            try:
48                ser.write(outgoing)
49            except serial.SerialException:
50                ser.close()
51                sys.exit("Trouble writing to serial port.")
52            except serial.SerialTimeoutException:
53                ser.close()
54                sys.exit("Timeout occured when writing to serial port.")
55            break
56
57    elif command == "c":
58        while True:
59            phase = raw_input("Enter new phase in degrees (0-359): ")
60            try:
61                phase = int(phase)
62            except ValueError:
63                print("Phase must be a positive integer.")
64                continue
65            if phase < 0 or phase > 359:
66                print("Phase out of range.")
67                continue
68            # construct packet, network byte order:
69            outgoing = struct.pack("!cH",command,phase)
70            try:
71                ser.write(outgoing)
72            except serial.SerialException:
73                ser.close()
74                sys.exit("Trouble writing to serial port.")
75            except serial.SerialTimeoutException:
76                ser.close()
77                sys.exit("Timeout occured when writing to serial port.")
78            break
79
80    elif command == "m":
81        while True:
82            phase = raw_input("Enter new phase in degrees (0-359): ")
83            try:
84                phase = int(phase)
85            except ValueError:
86                print("Phase must be a positive integer.")
87                continue
```

```
88              if phase < 0 or phase > 359:
89                  print("Phase out of range.")
90                  continue
91              # construct packet, network byte order:
92              outgoing = struct.pack("!cH",command,phase)
93              try:
94                  ser.write(outgoing)
95              except serial.SerialException:
96                  ser.close()
97                  sys.exit("Trouble writing to serial port.")
98              except serial.SerialTimeoutException:
99                  ser.close()
100                 sys.exit("Timeout occured when writing to serial port.")
101             break
102
103     elif command == "d":
104         while True:
105             dtime = raw_input("Enter new dead time in multiples of 40ns: ")
106             try:
107                 dtime = int(dtime)
108             except ValueError:
109                 print("Dead time must be a positive integer.")
110                 continue
111             if dtime < 40:
112                 print("Dead time out of range.")
113                 continue
114             if dtime % 40 != 0:
115                 print("Dead time should be a multiple of 40 (nanoseconds).")
116                 continue
117             # construct packet, network byte order:
118             outgoing = struct.pack("!cH",command,dtime)
119             try:
120                 ser.write(outgoing)
121             except serial.SerialException:
122                 ser.close()
123                 sys.exit("Trouble writing to serial port.")
124             except serial.SerialTimeoutException:
125                 ser.close()
126                 sys.exit("Timeout occured when writing to serial port.")
127             break
128
129     elif command == "a":
130         while True:
131             # Send the command character:
132             outgoing = struct.pack("c",command)
```

```
            try:
                ser.write(outgoing)
            except serial.SerialException:
                ser.close()
                sys.exit("Trouble writing to serial port.")
            except serial.SerialTimeoutException:
                ser.close()
                sys.exit("Timeout occured when writing to serial port.")
            break

    elif command == "q":
        print("Goodbye.\n")
        ser.close()
        sys.exit(0)

    elif command == "?":
        print("\nOPTIONS:")
        print("\n(f) Set carrier frequency.")
        print("\n(c) Set carrier reference phase for active carrier supression.")
        print("\n(m) Set mixer LO phase.")
        print("\n(d) Set dead time for 1/2 bridge coil time.")
        print("\n(a) Auto-calibrate carrier reference phase.")
        print("\n(q) Quit program.")
        print("\n(?) Display this menu.\n")
        continue

    else:
        print("Invalid command.")

    continue
```

E.2 Modelling and Experiments in MATLAB®

E.2.1 Current-Sense Pickup Model Validation

pickup_validation.m

```
%%% Pickup Model Validation %%%
% We run the 2000-turn pickup at 50-5000Hz, 1Arms, look at output voltage
% gained by 5x under various resistive loads on the pickup.  We compensate
% for the 5x gain in the data here.

freq = logspace(log10(50),log10(5000),10);

% Data is a 4x10 matrix.  The four rows correspond to resistances.
% 1: 15ohm | 2: 100ohm | 3: 1.1kohm | 4: 36kohm
% Resistances were chosen for convenience with whatever was lying around,
% trying to step through a few decades.

% Numbers represent peak-peak voltages at the output.

% Original Data (mV):
data = [3.2 4.8 6.0 7.0 7.1 7.5 8.1 8.2 8.4 8.6
        13.7 22.2 30.5 41.4 44.4 48.2 53.2 53.2 55.2 56.6
        29.1 48.0 75.6 132 200 310 440 512 570 596
        32.4 53.4 85.0 155 250 436 792 1300 2250 3880];
% Compensate for Inst Amp Gain:
data = data * 0.2;
% Convert from pk-pk to RMS:
data = data * sqrt(2);

% Analytical model of pickup, filled with measured physical parameters:
ana_freq = logspace(log10(50),log10(5000),100);
s = tf('s');
Rl = [15 100 1.1e3 36e3];
Rs = 115;
L = 220e-3;
Lm = 70e-3;
Ll = L - Lm;
N = 2000;
for n = 1:length(Rl)
    H = (1/N) * s*Lm*Rl(n) / (Rl(n) + Rs + s*L);
    resp(n,:) = 1e3 * abs(squeeze(freqresp(H,2*pi()*ana_freq)));
end


```

```
% Plotting:
loglog(freq,data(1,:),'ko',freq,data(2,:),'kx',freq,data(3,:),...
    'k+',freq,data(4,:),'k*',ana_freq,resp(1,:),'k-',ana_freq,resp(2,:),...
    'k-',ana_freq,resp(3,:),'k-',ana_freq,resp(4,:),'k-');
grid on;
axis([50 5000 1e-1 1e3]);
xlabel('1A RMS Test Current Frequency (Hz)');
ylabel('Pickup Output Voltage (mV RMS)');
title('Pickup Frequency Response Under Various Loads');
legend('15\Omega','100\Omega','1.1k\Omega','36k\Omega','Model','Location','SouthEast');
```

E.2.2 Current-Sense Pickup Loading Analysis

pickup_xfrmr_loading_analysis.m

```
%%% Simulation of Pickup Loading
% In this simulation we're looking at what voltage we can expect at the
% output of the parallel-series connected MET-01 transformers when we hook
% many up to a pickup.  Depending on the inter-stage loading, we may do
% better or worse with more transformers or more turns, or less of either.

% This code is pretty ugly.  I made it a long time ago, and am
% reworking it a little now for the figures in my thesis.  Basically I am
% using our measured parameters for all the devices, normalizing to 35AWG
% that I use and finding ohm/m values for other gauges from wikipedia.

% It is
% run four times for four separate plots, each of which the numbers have
% been re-done for in order to make them more realistic (i.e. each plot
% goes up to the max number of turns that could possibly fit on the core,
% unlike the old script, which went way over.)

% 500 ohms is the approximate input impedance to a MET-01 at 60Hz.  This is
% all for 60Hz.  There are dynamics here that change stuff as we go up, but
% 60Hz is sort of worst-case, because the inductive impedances are lower.

% max_turns = 2000 * (35awg_area / other_awg_area)^2

%% 25 AWG:

Vout = ones(8,4);

for Xcount = 1:8
f = 60;
w = 2 * pi() * f;
N = [50, 100, 150, 200];
R = 0.0984 * 0.05 * N;
Al = 53.5e-9;
L = Al * N.^2;
Vin = 18.2e-6 * N;
Zx = 500/Xcount * ones(1,length(N));
Zo = R + w*L;
Vload = Vin .* (Zx ./ (Zx + Zo));
Vout(Xcount,:) = Xcount * 8 * Vload;
end

Xcount = 1:8;
```

```
plot(Xcount, Vout(:,1), 'ko', Xcount, Vout(:,2), 'kx', Xcount, Vout(:,3), 'k+', Xcount, Vout(:,4), 'k*');
grid on;
xlabel('Number of MET-01 transformers connected in parallel-series configuration')
ylabel('Voltage across transformer secondary');
title('Current-sense pickup optimization plot');
legend('50 Turns', '100 Turns', '150 Turns', '200 Turns');

%% 30 AWG:

Vout = ones(8,4);

for Xcount = 1:8
f = 60;
w = 2 * pi() * f;
N = [150, 300, 450, 600];
R = 0.3138 * 0.05 * N;
Al = 53.5e-9;
L = Al * N.^2;
Vin = 18.2e-6 * N;
Zx = 500/Xcount * ones(1,length(N));
Zo = R + w*L;
Vload = Vin .* (Zx ./ (Zx + Zo));
Vout(Xcount,:) = Xcount * 8 * Vload;
end

Xcount = 1:8;
plot(Xcount, Vout(:,1), 'ko', Xcount, Vout(:,2), 'kx', Xcount, Vout(:,3), 'k+', Xcount, Vout(:,4), 'k*');
grid on;
xlabel('Number of MET-01 transformers connected in parallel-series configuration')
ylabel('Voltage across transformer secondary');
title('Current-sense pickup optimization plot');
legend('150 Turns', '300 Turns', '450 Turns', '600 Turns');

%% 35 AWG:

Vout = ones(8,4);

for Xcount = 1:8
f = 60;
w = 2 * pi() * f;
N = [500, 1000, 1500, 2000];
R = 1.0 * 0.05 * N;
Al = 53.5e-9;
L = Al * N.^2;
Vin = 18.2e-6 * N;
```

```
Zx = 500/Xcount * ones(1,length(N));
Zo = R + w*L;
Vload = Vin .* (Zx ./ (Zx + Zo));
Vout(Xcount,:) = Xcount * 8 * Vload;
end

Xcount = 1:8;
plot(Xcount, Vout(:,1), 'ko', Xcount, Vout(:,2), 'kx', Xcount, Vout(:,3), 'k+', Xcount, Vout(:,4), 'k*');
grid on;
xlabel('Number of MET-01 transformers connected in parallel-series configuration')
ylabel('Voltage across transformer secondary');
title('Current-sense pickup optimization plot');
legend('500 Turns', '1000 Turns', '1500 Turns', '2000 Turns');

%% 40 AWG:

Vout = ones(8,4);

for Xcount = 1:8
f = 60;
w = 2 * pi() * f;
N = [1500, 3000, 4500, 6000];
R = 3.1891 * 0.05 * N;
Al = 53.5e-9;
L = Al * N.^2;
Vin = 18.2e-6 * N;
Zx = 500/Xcount * ones(1,length(N));
Zo = R + w*L;
Vload = Vin .* (Zx ./ (Zx + Zo));
Vout(Xcount,:) = Xcount * 8 * Vload;
end

Xcount = 1:8;
plot(Xcount, Vout(:,1), 'ko', Xcount, Vout(:,2), 'kx', Xcount, Vout(:,3), 'k+', Xcount, Vout(:,4), 'k*');
grid on;
xlabel('Number of MET-01 transformers connected in parallel-series configuration')
ylabel('Voltage across transformer secondary');
title('Current-sense pickup optimization plot');
legend('1500 Turns', '3000 Turns', '4500 Turns', '6000 Turns');
```

E.2.3 JFET Mixer Saturation Boundary

jfet_sat_boundary.m

```
%%% Calculating Saturation Point of J1 in JFET Mixer
% This a quick plotter to show where the point at which the top JFET of the
% JFET mixer enters the saturation.  The result is that as long as we keep
% both the carrier and signal voltages small, we should be perfectly fine.

% Transistor Parameters:
Vp = -1.2;
Idss = 57.6e-6;

% Set up Vs array:
Vs = -1.0:10e-3:1.0;

% Saturation Boundary Equation:
Vc = -sqrt(2) * (Vp - Vs);

plot(Vs,Vc)
grid on;
xlabel('Signal Voltage V_S');
ylabel('Carrier Voltage V_C');
title('Saturation Boundary V_{C_{SAT}} for J_1');
```

E.2.4 Parallel-To-Series Transformation of the Incremental Resistance of the JFET Modulator

jfet_selection.m

```
%%% JFET Selection Thoughts
% This script plots how the parallel-to-series transformation of the JFET
% modulator incremental resistance and the inner-resonator capacitor
% influences our design.  The plots assume a winding resistance of
% 100\Omega, sweep the JFET modulator resistance, and parameterized by
% various values of the resonant capacitor.

% Carrier Frequency:
f = 20e3;
w = 2*pi()*f;
% Sweep JFET Modulator Incremental Resistance:
RJ = logspace(1,6);
% Inner Resonator Capacitor:
CR2 = [100e-12 1e-9 10e-9 100e-9 1e-6];
% Inner Resonator Winding Resistance:
RL2 = 100;

for n = 1:length(CR2)
    % Calculate Q of R||C combination:
    QC2 = RJ * (w*CR2(n));
    % Use Q to perform parallel-to-series transformations:
    RJS(n,:) = RJ ./ (QC2.^2 + ones(1,length(QC2)));
    C2(n,:) = CR2(n) * (ones(1,length(QC2)) + QC2.^-2);
end

% Combine RJS with winding resistance to get effective R2:
R2 = RL2*ones(length(CR2),length(RJ)) + RJS;

figure(2);
loglog(RJ,R2(1,:), RJ,R2(2,:),  RJ,R2(3,:),  RJ,R2(4,:),  RJ,R2(5,:))
grid on;
title('Effective series resistance R_2 as a function of JFET incremental resistance R_J');
xlabel('JFET incremental resistance R_J (\Omega)');
ylabel('Effective series resistance R_2 (\Omega)');
legend('C_{R2} = 100pF', 'C_{R2} = 1nF', 'C_{R2} = 10nF', 'C_{R2} = 100nF',...
    'C_{R2} = 1\muF', 'Location', 'NorthWest');


figure(3);
loglog(RJ,C2(1,:), RJ,C2(2,:),  RJ,C2(3,:),  RJ,C2(4,:),  RJ,C2(5,:))
```

```
41 grid on;
42 title('Effective series capacitance C_2 as a function of JFET incremental resistance R_J');
43 xlabel('JFET incremental resistance R_J (\Omega)');
44 ylabel('Effective series capacitance C_2 (F)');
45 legend('C_{R2} = 100pF', 'C_{R2} = 1nF', 'C_{R2} = 10nF', 'C_{R2} = 100nF',...
46     'C_{R2} = 1\muF');
```

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