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A Wide-Dynamic-Range Compression Image Sensor With Negative-Feedback Resetting

Masayuki Ikebe and Keita Saito

Abstract—A CMOS image sensor capable of wide-dynamic-range compression is proposed. This sensor has two main features. It uses a negative-feedback technique to set any intermediate voltage into photodiode (PD) capacitance in the pixel circuit. It also uses a quasi-holding function by resetting the pixel-output voltage into PD capacitance. Dynamic range compression is achieved by individually selecting pixels and by setting an intermediate voltage or performing quasi-holding with respect to each pixel. Output data has a polygon-like form corresponding to a change from high sensitivity to low sensitivity as optical intensity becomes stronger. Experimental results obtained with a chip fabricated using a 0.25-μm CMOS process demonstrate dynamic range compression.

Index Terms—CMOS image sensor, dynamic range compression, individual reset, negative-feedback reset.

I. INTRODUCTION

THE FIELD OF broadband communications has been developing rapidly in recent years as the information society continues to expand. Relatively large amounts of data can now be handled with ease and the exchange of image data has become commonplace. Digital cameras are widely used and almost all cell phones have a camera function. The heart of a digital camera is either a charge-coupled device (CCDs) or CMOS image sensor, both of which are being aggressively developed for a wide range of applications including cell phones, monitors, and on-vehicle equipment. Image sensors of the CMOS type are especially good at integrating peripheral CMOS circuits and thereby enabling various types of image-processing functions to be included on the same chip, an extremely convenient feature. Although noise (both thermal noise and the fixed-pattern noise due to device variation) is a greater problem in CMOS image sensors than in CCDs, improvements in the manufacturing process and the use of noise-elimination techniques such as correlated double sampling (CDS) have reduced the noise levels of CMOS image sensors almost to those of CCDs.

We recently proposed a negative-feedback reset as a noise cancellation technique and showed that it can obtain intermediate image data during the charge-accumulation process [1].

The availability of intermediate image data makes it possible to read the change in luminosity during charge accumulation, and we expect this capability to be exploited in a variety of applications [2]. In this paper, we show how a CMOS image sensor with a wide-dynamic-range can be obtained by using a negative-feedback reset to modulate photodiode (PD) capacitance. The proposed technique enables a pixel circuit with a minimum configuration to be individually reset and for the same pixel to exhibit both low-sensitivity and high-sensitivity characteristics.

The remainder of this paper is organized as follows. Section II describes the wide-dynamic-range compression algorithm. Section III presents the results of system simulations based on the results given in Section II. Section IV describes a technique for performing a negative-feedback reset at any voltage and performing quasi-holding of the pixel state, and it also describes a circuit implementing that technique. Section V describes the results of circuit simulations, and Section VI evaluates trial chip.

II. OBTAINING A WIDE-DYNAMIC-RANGE

A. Dealing With Optical Intensity

Conventional CCDs and CMOS image sensors are able to pick up images under various levels of optical intensity by adjusting exposure time. In a CCD, this is done by resetting through the unloading of accumulated charge, and in a CMOS image sensor, it is done by switching a reset MOSFET. However, since the output range of pixel circuits is fixed, making the same adjustment to exposure time for all pixels in the device would cause pixels subjected to high luminance to be overexposed and pixels subjected to low luminance to be underexposed. This phenomenon can be dealt with by simulating an image pickup ability above the actual output range of pixel circuits, but that requires an algorithm for that purpose, as well as circuit modifications. There are other ways a wide-dynamic-range can be obtained. In a CCD, two images having different exposure times can be combined or pickup elements of different sensitivities can be integrated. In a CMOS image sensor, a variety of techniques can be used. These include combining multiple images having different exposure times [4], installing a logarithmic conversion circuit in each pixel [5], [6], adjusting pixel exposure time by conditional resets [7], switching between pixel circuit configurations [8], and changing saturation characteristics by modulating PD capacitance to [9]. In this paper, we show how to achieve a wide-dynamic-range by using negative-feedback resets to modulate the PD capacitance of each pixel individually.
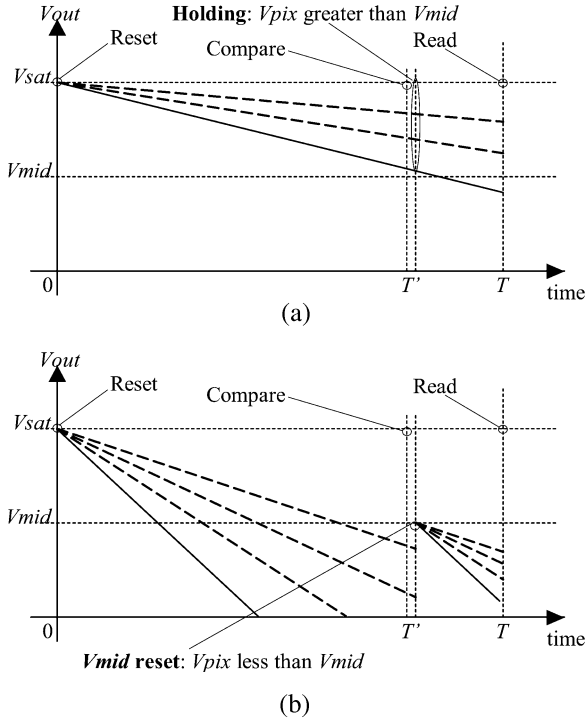
Fig. 1.   Timing diagrams and characteristics of proposed image sensor. (a) Setting for low luminance. (b) Setting for high luminance.

B. PD-Capacitance Control and Expanding of Dynamic Range

Here, we describe the approach for setting reset timing. Fig. 1(a) and (b) shows timing diagrams for two types of settings. It is assumed here that each pixel circuit performs output at fixed intervals corresponding to frame period T. The pixel output range is denoted $Vsat$.

The system first performs an initial reset on the pixel circuit. This reset cancels out circuit dispersion error by negative-feedback. The negative-feedback reset is described in detail in Section IV. Then, at time T', the system performs an intermediate image readout and detects whether the pixel output $Vpix$ is greater than or less than $Vmid$. When luminance is higher, light current is larger and $Vpix$ falls faster. The $Vpix$ value may, therefore, be saturated under very high luminance. If $Vpix$ is greater than $Vmid$ (luminance is low), the system does nothing [Fig. 1(a)]. If $Vpix$ is less than $Vmid$ (luminance is high), the system supplies a current resetting $Vpix$ to $Vmid$ [Fig. 1(b)]. In both cases, the exposure and charge accumulation continue until time T. In the high-luminance case, the range of output $Vpix$ values at time T is compressed because of the reset at exposure time $T - T'$. Optical-intensity characteristics can be changed by the adjusting the time T' and the value of $Vmid$, but the output range $Vsat$ does not change.

C. Image Output Format

Fig. 2(a) shows output characteristics versus optical intensity. The system exhibits usual exposure characteristics up to a certain value of optical intensity, at which point the output characteristics change abruptly. At higher optical intensities, the sensitivity is reduced and even strong light will result in an unsaturated output value. This means that a single pixel can have both a high-sensitivity state and a low-sensitivity state. Furthermore,
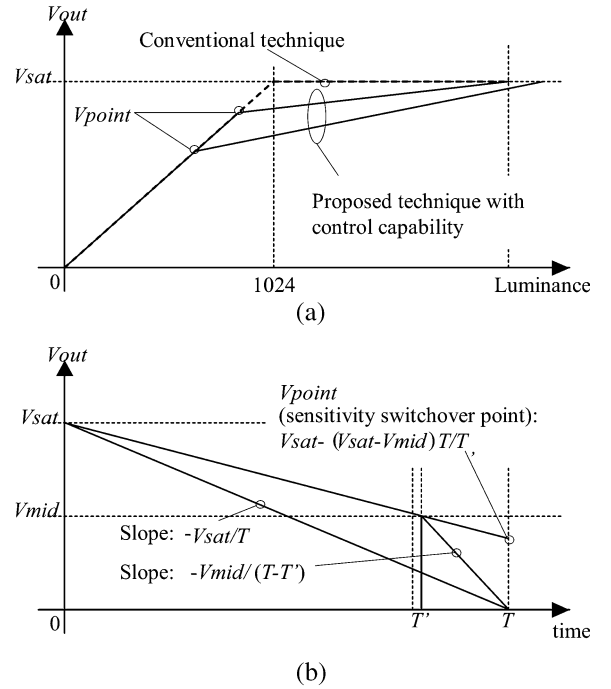

Fig. 2.   Output form of proposed image sensor. (a) Optical intensity characteristics of proposed image sensor. (b) Output characteristics of proposed image sensor.
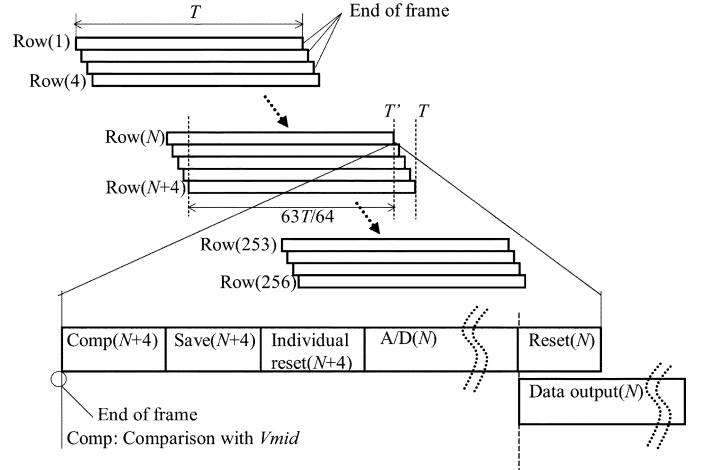

Fig. 3.   Timing of pixel array operation.

as the values of T', $Vmid$, and $Vsat$ described in Section II-B correspond to the switchover point and the low-sensitivity slope, it becomes quite easy to change characteristics to accommodate various types of picture-taking scenarios. Referring to Fig. 2(b), the ratio of the low-sensitivity slope to the high-sensitivity can be given as $(T - T')/Vmid : T/Vsat$ and $Vpoint$ can be given as $Vsat - (Vsat - Vmid) \cdot (T/T')$. For example, when $T' = T/128$ and $Vmid = Vsat/2$, a dynamic range of 36 dB greater can be obtained within the output data range.

D. Timing of Operation for Focal Plane Shutter

The timing of a 256×256-pixel array with column-parallel driving by a focal plane shutter is shown in Fig. 3. Since the operations for each row are performed sequentially, the reset time of each row produces delay. Therefore, the timings of
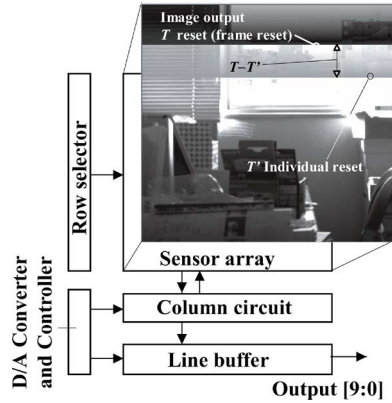
Fig. 4. Overview of system simulation.

Fig. 5. Simulation results (left: conventional; right: proposed).

voltage comparison and individual resets are synchronized with the frame end of a certain specific row, and the abovementioned operations are performed at the time of the frame end for every row. An operation order in Nth row is as follows (referred to as example $T' = 63T/64$).

After the frame operations of $N - 1$th row are completed:
1) the intermediate readout and the comparison of the $N+4$th row ($T' = 63T/64$, $N + 4$);
2) the intermediate readout and the saving pixel outputs of the $N + 4$th row;
3) the individual reset of the $N + 4$th row;
4) the readout and ADC of the Nth row;
5) the frame reset of the Nth row are executed.

Next, the frame-operations of $N + 1$th row start. Frame processing for focal plane shutter can be achieved by performing these operations continuously.

III. System Simulation and Evaluation

Fig. 4 shows a block diagram of the entire system consisting of a sensor array (capable of individual pixel reset), a row selector, a column circuit performing comparison and negative-feedback reset, a line buffer for column A/D, and a D/A converter and controller that generates reference voltages and controls the column circuit. The above modules were described in SystemC and system simulation was performed. External optical information was obtained by combining multiple pictures taken with different exposure times from an indoor location when the weather was fair. To achieve virtual charge accumulation here, the sensor-array module was made to integrate optical information every unit time period, and to simulate a focal plane shutter, a reset was performed for each row using the above unit time period for integration by the sensor array. In this way, the controller could express the parameter T' in terms of number of rows (as in ordinary CMOS image sensors). The $Vmid$ voltage was assigned a value from 0 to 255 corresponding to the range from the minimum value to the maximum value of the image display. The total number of rows (resolution in the Y-direction) was 256.

Proceeding one row at a time from top to bottom, the system performed charge-accumulation operations while shifting timing. The controller module generated control signals for each of the operations of Section II-B in accordance with T and T'. The comparison results stored in each column's 1 bit

state-holding memory was only used for the next process step, making it possible to omit long-term memory such as for flags. This system was found to operate smoothly despite the absence of long-term memory. Fig. 5 shows simulation results. The left-hand image shows that high-luminance pixels resulted in overexposure of a picture output by the conventional technique, while the right-hand image shows that the image conversion by the proposed technique captured the outdoor scene, while maintaining most of the luminance of the indoor scene.

IV. Pixel Circuit Performing Negative-Feedback Reset

A. Configuration of Proposed Circuit

Fig. 6(a) shows the configuration of the circuit we designed for performing negative-feedback reset at any voltage and quasi-holding of the pixel state. The format of the pixel portion of this circuit is that of a conventional three-transistor active pixel sensor (APS). A signal line is laid vertically from the upper electrode of nMOSFET M1, and the Va point of the gate electrode of nMOSFET M2 connects to the upper end of the PD. The Rst label indicates the reset signal of the pixel circuit and Sel is the select signal. The Vb point is output of the pixel circuit. The Vb value is equivalent to $Vpix$ in Section II-B. The common portion of this circuit for each column consists of a current source for the source follower, a differential amplifier, switches SW1-SW4 to change wiring connections, and a 1-bit state-holding memory. The voltage $Vref$ from DAC provides noninverting input to the differential amplifier. It can be set to various values to perform the operations described in Section IV-B.

The circuit of the differential amplifier is shown in Fig. 6(b), where both the Vc and Vd outputs are the outputs of a single-end amplifier. The output to use is selected by $Vctrl$, which changes only the input electrode $(+/-)$ and leaves the input connection unchanged.

B. Operation of Proposed Circuit

The proposed circuit performs operations in the following five modes corresponding to specific wiring connections and control signals.
1) Reset mode.
2) Comparator mode.
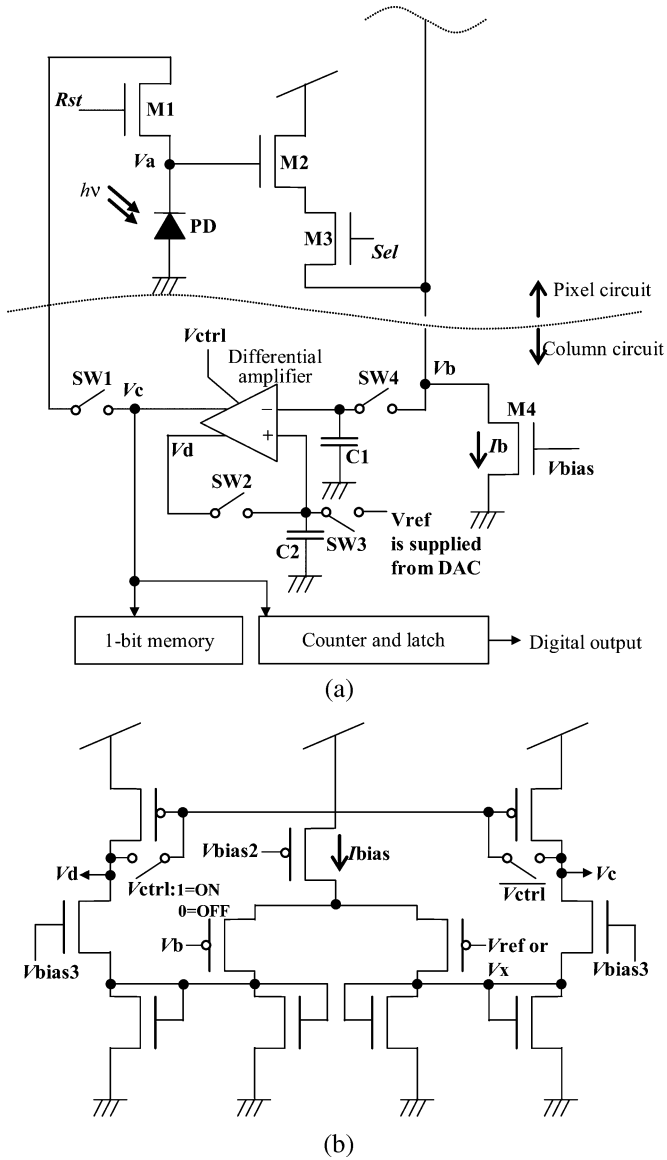3) Signal-save mode.
4) Refresh mode.
5) Signal-output mode.

Fig. 6.   Proposed configuration of image sensor. (a) Proposed circuit configuration. (b) Circuit configuration of differential amplifier.
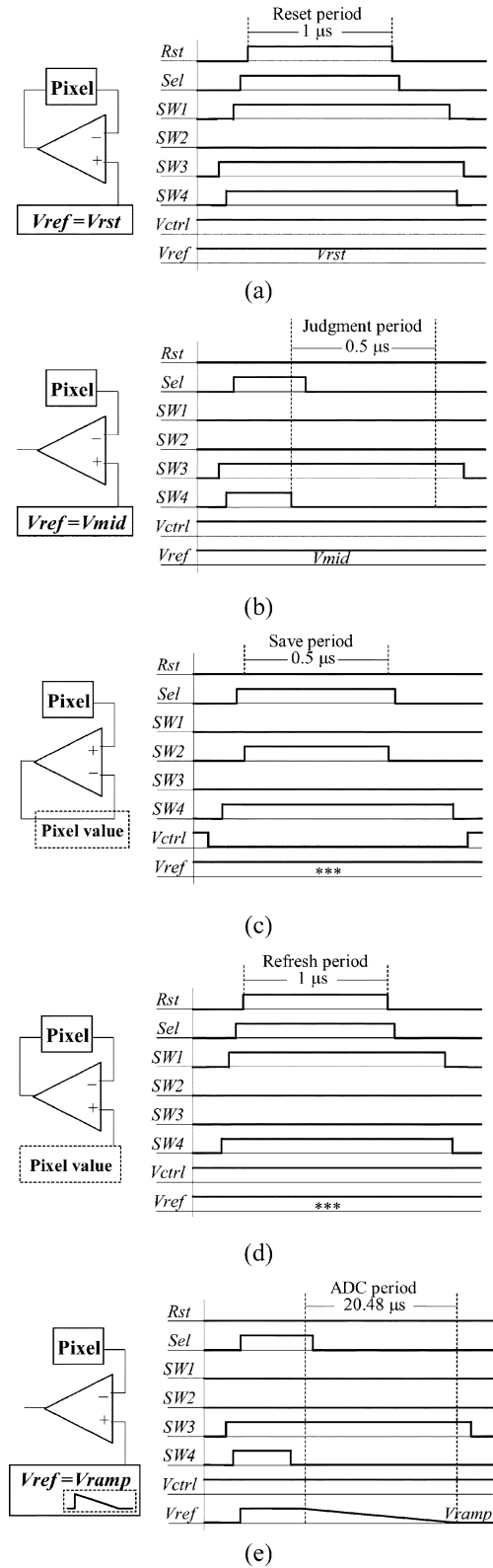

Fig. 7.   Timing chart and wiring connection of each mode. (a) Reset mode. (b) Comparator mode. (c) Signal-save mode. (d) Refresh mode. (e) Signal-output mode.

Fig. 7 shows the timing charts and wiring connections of operations. In mode 1 [Fig. 7(a)], at the beginning of the image pickup cycle, M1 is set to ON by the Rst signal so as to reset the PD. We specified the reset period as 1 μs. At the same time, M3 is set ON by the Sel signal to form a negative-feedback loop between the pixel circuit and the output amplifier. Here, we denote the transconductance, threshold, and threshold variation of M2 as β, Vth, and ΔVth; the current flowing through M4 as Ib; the gain of the differential amplifier as A; noninverting input as $Vrst$; inverting input as Vb; and the gain of the source-follower due to M2 and M4 as $H = 0.8$ (constant value). The offset component $Dout$ on the negative-feedback loop can then be given by (1) and the transfer characteristic of the closed-loop by (2). We see from (2) that $A \gg 1$ in the state corresponding to the formation of a negative-feedback loop and that the potential of the output line is reset so that (2) is always satisfied. In other words, at any voltage the system performs a reset based on the

value of $Vrst$. Another reset system using negative-feedback has been reported [3], but the pixel circuit for that system has more nMOSFETs than does the pixel circuit in the system presented here. Furthermore, because the circuit in that report has a
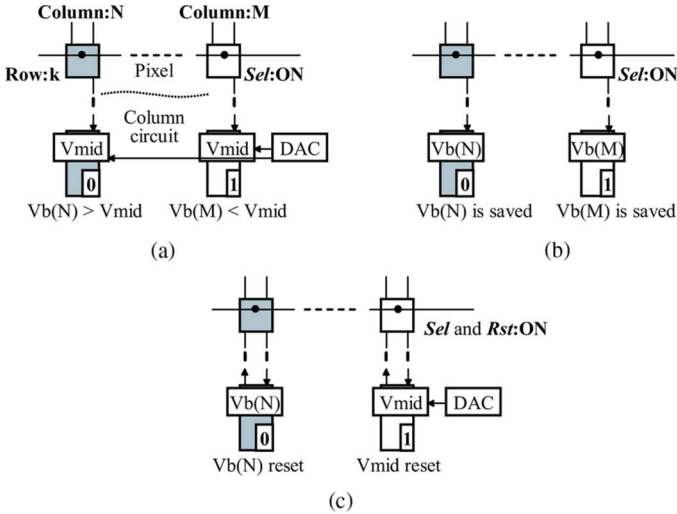
Fig. 8. Individual resetting mechanism. (a) Comparator mode phase. (b) Signal-save mode phase. (c) Refresh and reset mode phase.

configuration by which a nMOSFET interconnects column-circuit output and the gate of the reset nMOSFET, the reset voltage drops exactly by the threshold value of that nMOSFET and, thus, results in a smaller dynamic range

$$Dout = -\left(Vth + \Delta Vth + \sqrt{\frac{Ib}{\beta}}\right) \tag{1}$$

$$Vb = Vrst\frac{AH}{1+AH} + Dout\frac{H}{1+AH}. \tag{2}$$

In mode 2 [Fig. 7(b)], the differential amplifier operates as a comparator with respect to signal output Vb (with the result that differential-amplifier output is set to a logical 1 or 0). We specified the judgment period as 0.5 μs. In mode 3 [Fig. 7(c)], the differential amplifier acts as an elemental voltage follower whereby SW2 can be controlled to save the value of Vb in capacitor C2. We specified the save period as 0.5 μs. Since there are small parasitic elements in the save mode connection, convergence becomes quick. In mode 4 [Fig. 7(d)], the completion of mode 3 results in a reset operation similar to mode 1 but based on the signal value saved in capacitor C2. We specified the reset period as 1 μs. Finally, in mode 5 [Fig. 7(e)], the system outputs a pulsewidth modulation (PWM) signal. A circuit is configured as a comparator like mode (2). The PWM signal according to the value of Vb can be obtained by comparing Vb with the RAMP signal $Vramp$. This mode is used for single-slope ADC. Since the single-slope ADC is 10-bit accuracy, 1024 clock cycles are required. Therefore, the ADC period is 20.48 μs at 50 MHz clock.

C. Individual Reset

Pixels can be reset individually by making use of the modes described in Section IV-B. Fig. 8 shows the mechanism of individual resetting. First, using the comparator mode, the result of comparison is stored in the 1-bit state-holding memory. Next, using the signal-save mode, the current pixel value is saved to C2. Our system can selects the wire connection of column circuits according to the data stored in the 1-bit memory. If the stored data is "0," the connection for refresh mode is selected.

If the stored data is "1," the connection for reset mode is selected. The reset value is $Vref = Vmid$ supplied from DAC. At that time, if the negative-feedback loop is formed by Rst and Sel turning on, the current pixel value is reset to the pixel circuit with refresh connection of column circuit and the $Vref$ ($= Vmid$ supplied by DAC) value is reset to the pixel circuit with the reset connection of the column circuit. In other words, Rst can be ON for all columns on a certain row k simultaneously and the pixel at coordinates (M, k) can be reset, while the value of the pixel at (N, k) can be saved. The significance of this is that each pixel can be reset individually without having to increase the number of transistors in the standard three-transistor APS configuration in the pixel section of the circuit.

D. Compensation of Mismatch Voltage in the Differential Amplifier

Denoting the mismatch in the differential amplifier as $Vmiss$ and noting that $Vmid$ appears as $Vmid+Vmiss$, Vb at the time of reset can be expressed by (3). If A $\gg$ 1, reset for Vb is performed so that the mismatch compensation component is added to $Vmid$. That is, the mismatch component appearing in Vc can be decreased by approximately the inverse of the gain. At the time of signal saving, the polarity of the differential amplifier reverses, resulting in (4). Here, the added mismatch voltage is cancels out. In addition, $Vmisstotal$, the mismatch affecting the save voltage, is approximately the inverse of the gain, which means that it can be used instead of $Vmid$ at the time of resetting

$$Vb = (Vrst + Vmiss)\frac{AH}{1+AH}$$
$$+ Dout\frac{H}{1+AH} \tag{3}$$

$$Vd = (Vb - Vmiss)\frac{A}{1+A} \tag{4}$$

$$Vmisstotal = -\left(Vmiss\frac{1}{1+AH}\right)\frac{A}{1+A}. \tag{5}$$

During A/D conversion and comparison operations, the mismatch component appearing in Vc is approximately the inverse of the gain but the gain effect decreases according to the slope of $Vramp$. Accuracy can be improved by implementing the offset canceller after the differential amplifier. In this work, we adopted the offset canceller to each column.

V. Circuit Design

A. Design Considerations of Basic Circuit

The circuitry of differential amplifier, in Fig. 6(b) is important for stability of the reset operation. In using two-stage configurations for the amplifier, a large phase-compensation capacitance is need for stability. Therefore, the slew rate becomes low and the settling time becomes slow. In this work, a single-stage configuration was used and stability was obtained without phase-compensation capacitance. The gain of the amplifier was compensated with cascode connection of the output portion.

We specified reset within 1 μs in the signal range 1V, so a signal rising time under 0.25 μs was needed. In this case, a power bandwidth greater than 640 kHz was required in using the amplifier as a unity-gain buffer. Because the circuitry we used

did not have phase-compensation capacitance, slew rate is defined by parasitic elements and the current of the output portion. However, a secondary pole is produced by a parasitic element and the delay of the settling time by dumping can be considered. Then, because one of our top priorities was a DC gain of 60 dB, the output portion was designed for to provide a settling time $< 0.5\ \mu s$ under the conditions of a slew rate $> 4\ V/\mu s$.

We adopted the differential amplifier as single-end use. Therefore, possibility of a common-mode-noise problem was considered. Then, we suppressed noise generating of the digital part which was the key factor of a common mode noise as much as possible. The taken measures were as follows.

1) Two or more switching is not performed simultaneously within a column circuit.
2) The digital circuit stops during analog circuitry operation without digital data output.
3) Powerful guard ring is arranged in the boundary of a digital part and an analog part.
4) The digital output lines are protected with a shield.
5) Gray code is used to the counter circuit for single-slope ADC. Since it is 1-bit change at a time, gray code can suppress the noise of the counter.
6) A low-pass filter is put into a DAC output.

The DAC may become noise source with the output change by bit change at the time of RAMP waveform generation. Therefore, we put valid LPF into the DAC output.

When we use the differential amplifier, although the kTC noise is not eliminated, the kTC noise in the band of the closed-loop becomes a fraction of amplifier gain.

B. Layout Design of Basic Circuit

We designed a trial version of a basic circuit using a 0.25-μm CMOS process. In the pixel circuit, a negative-feedback bus from the readout circuit connects to a traditional three-transistor configuration. The pixel circuit including this negative-feedback bus was designed to be 5 μm square with a fill-factor ratio of 40%. Moreover, the circuits without PDs are shaded by metal and black polymer.

The column circuit was designed to have a width of 5 μm to facilitate connection with the pixel circuit (assuming one circuit per column). Fig. 9 shows the layout of the analog portion of the column circuit. The size of the differential amplifier was 5 $\mu m \times 100\ \mu m$. The values of capacitors C1 and C2 in Fig. 2(a) were both 100 fF.

C. Main Circuit Simulation

We did a simulation of a column circuit and a pixel circuit, and the loop characteristics of the column circuit and the pixel circuit are shown in Fig. 10. Parasitic capacitance and resistance, 1 pF and 400 Ω, were added to reset line and readout line. The circuit had an open-loop DC gain of 58 dB and a phase margin of 42°. The closed-loop characteristics are shown in Fig. 10. We confirmed that the circuit operated as a unity gain buffer.

The amplifier does not change in the loop characteristic until the light current of the PD exceeds 50 nA. Although the gain decreases and the phase characteristic changes over 50 nA, the stability is satisfactory (phase margin =: 40°). 50 nA is equivalent to about 3 000 000 lux in this process.
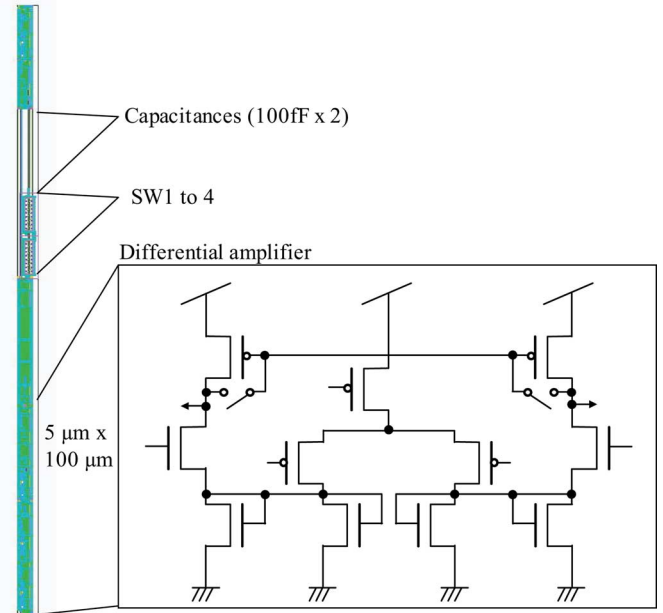

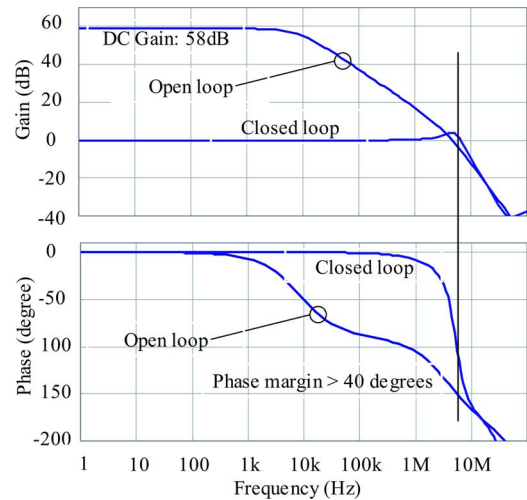Fig. 9. Basic layout of trial circuit.

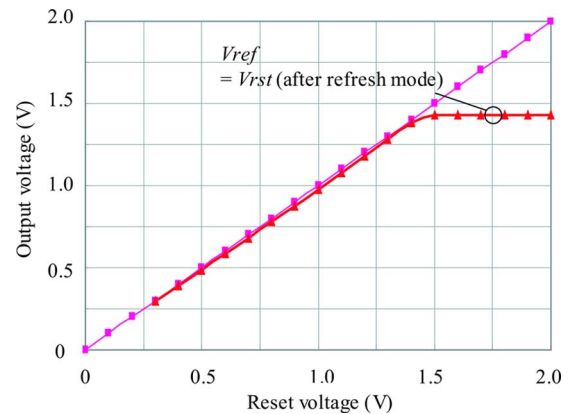Fig. 10. Loop characteristics of designed circuit.

Fig. 11. Characteristics of refresh operation.

We examined the characteristics of refresh operation through simulation. Fig. 11 shows readout values in signal-save mode (voltage follower) immediately after performing refresh mode. The light current of the pixel circuit was set to be 0 nA. The plots

TABLE I
INSTRUCTION SET OF PROGRAMMABLE SEQUENCER

Command name	Function	Number of words
WAIT	Waiting time to the next command execution is defined.	1
LINE_CNT	Line (row) selection is controlled	1
SW_OPA	Differential amplifier switching are controlled.	1
SW_MISC	Pixel-circuit switching are controlled.	1
SW_AR	Test-circuit switching are controlled.	1
SET_LOOP	Loop operation are controlled.	1
JMPL	Loop operation are controlled.	1
WREG	Writing value to control registers for DAC and ADC.	2

One word consists of 3 bit header and 9 bit body.
Two words consist of 3 bit header and 21 bit body.

TABLE II
PROPOSED IMAGE SENSOR PERFORMANCE

Process	0.25 μm CMOS 1P4M
Supply voltage	2.5V for logic, 3.3V for analog
Resolution	320×240 (QVGA)
Pixel size	5μm × 5μm
Fill factor	40% (w/o μlens)
Transistors per pixel	3Tr./pixel
Sensitivity	0.6V/Lux*sec (with μlens)
Power consumption of column circuit	100μW/column
ADC	10bit
DAC	11bit (+ offset 8bit)
frame rate	60frame/s@50MHz
Extended dynamic range	+42dB

Fig. 12. Layout of the trial chip.

shown were obtained while varying $Vrst$ with $Vref = Vrst$. We confirmed that the circuit operated saving and rewriting the pixel value.

D. Controller Design

The architecture of the controller is that of a programmable sequencer (PS) that has eight instructions that consist of 12-bit words. The list of instructions is shown in Table I. The WAIT commands controls waiting time to next command operation. The LINE_CNT commands controls row selecting. The SW_OPA, SW_MISC, and SW_AR commands control switches. Using these commands, a certain switch is selected and on/off controlled at a cycle. The SET_LOOP and JMPL commands are used for repeat operations. The WREG command has double word, and set control value such as voltage code, voltage-offset code and delay-code to control register of DAC and ADC. When a command sequence for dynamic range compression is written to the 128-word instruction memory and is executed, the function is realized.

VI. EXPERIMENTAL RESULTS

We fabricated the new wide-dynamic-range compression image sensor by using a 4-metal 0.25-μm CMOS process. Table II shows the specification for the proposed image sensor. Fig. 12 shows the layout of the trial chip, and Figs. 13 and 14 show examples of images obtained using the trial chip. The feedback reset was performed under fine weather (100 000 lux) and directly under the parallel light source (5000 lux). Fig. 13 shows the results of feedback reset under the high-luminance environment. These were read out immediately after negative-feedback reset. The characteristics of negative-feedback reset were not changed under these conditions. Fig. 14(a) is the conventional image and Fig. 14(b) is the proposal image
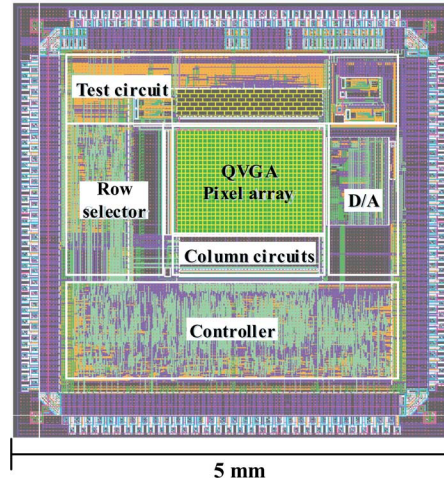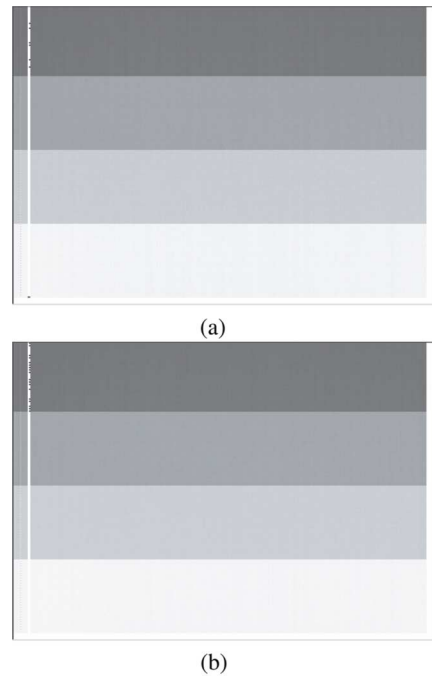

(a)

(b)

Fig. 13. Characteristics of negative-feedback resetting under high luminance environment. (a) Under 5000 lux. (b) Under 100 000 lux.
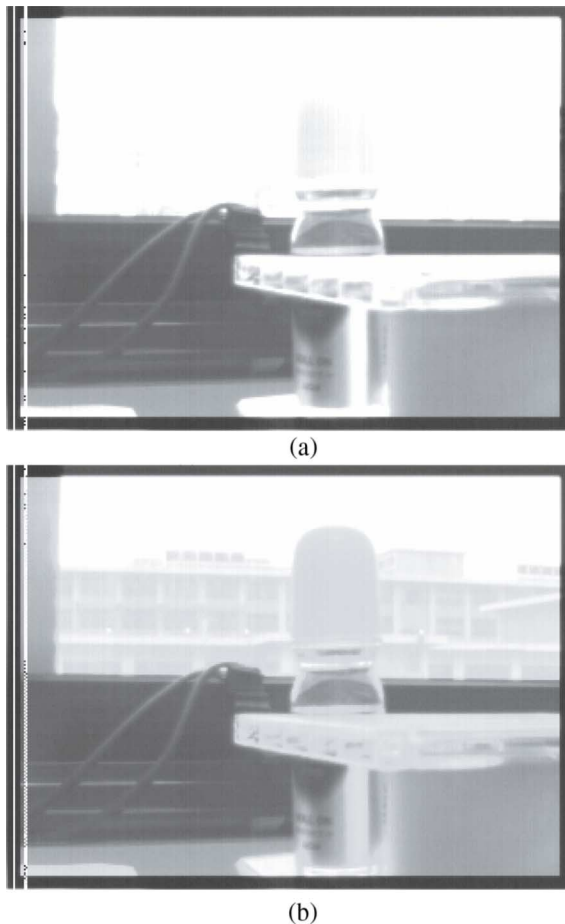
(a)

(b)

Fig. 14. Images captured by the proposal image sensor. (a) Conventional method. (b) Proposal method.

obtained with $T' = T/16$ and $Vmid = 0.6Vrst$. In Fig. 14(b), the outdoor scene is evident because of the extended dynamic range.

VII. CONCLUSION

We developed an image-sensor circuit that can perform a reset at any intermediate voltage by using negative-feedback. This circuit enables pixels to be individually reset by an intermediate voltage without having to add a selection transistor. Using this reset scheme, we developed a technique for modulating PD capacitance in a CMOS image sensor to give it a wide-dynamic-range. We also described the characteristics of a prototype image sensor array.

ACKNOWLEDGMENT

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Masayuki Ikebe received the B.S., M.S., and Ph.D. degrees in electrical engineering from Hokkaido University, Hokkaido, Japan, in 1995, 1997, and 2000, respectively.

During 2000–2004, he was with the Electronic Device Laboratory, Dai Nippon Printing Corporation, Akabane, Japan, where he was engaged in the research and development of wireless communication system and image processing system. Presently, he is an Associate Professor at the Graduate School of Information Science and Technology, Hokkaido University. His current research includes CMOS-image sensor and analog circuits.
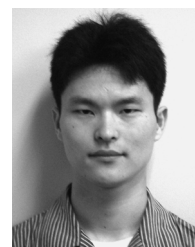
Keita Saito received the B.S. degree in electrical engineering from Hokkaido University, Hokkaido, Japan, in 2006.

His current research is image processing systems and analog circuits.