[15] M. J. Lombardi, "Bayesian inference for alpha-stable distributions: A random walk MCMC approach," *Comput. Stat. Data Anal.*, vol. 51, no. 5, pp. 2688–2700, Feb. 2007.
[16] C. Menn and S. T. Rachev, "Calibrated FFT-based density approximations for stable distribution," *Comput. Stat. Data Anal.*, vol. 50, no. 8, pp. 1891–1904, Apr. 2006.
[17] C. J. Geyer, "Markov chain Monte Carlo maximum likelihood," in *Proc. 23rd Symp. Interface—Comput. Sci. Statist.*, 1991, pp. 156–163.
[18] M. A. Suchard, "Understanding GPU programming for statistical computation: Studies in massively parallel massive mixtures," *J. Comput. Graph. Stat.*, vol. 19, no. 2, pp. 419–438, Jun. 2010.
[19] A. Lee, C. Yau, M. B. Giles, A. Doucet, and C. C. Holmes, "On the utility of graphics cards to perform massively parallel simulation of advanced Monte Carlo methods," *J. Comput. Graph. Stat.*, vol. 19, no. 4, pp. 769–789, Dec. 2010.

Fast Antijamming Timing Acquisition Using Multilayer Synchronization Sequence

Jiaqi Zhang, Ning Ge, *Member, IEEE*, Zhaocheng Wang, *Senior Member, IEEE*, and Sheng Chen, *Fellow, IEEE*

***Abstract*—Pseudonoise (PN) sequences are widely used as preamble sequences to establish timing synchronization in military wireless communication systems. At the receiver, searching and detection techniques, such as the full parallel search (FPS) and the serial search (SS), are usually adopted to acquire correct timing position. However, the synchronization sequence has to be very long to combat jamming that reduces the signal-to-noise ratio (SNR) to an extremely low level. In this adverse scenario, the FPS scheme becomes too complex to implement, whereas the SS method suffers from the drawback of long mean acquisition time (MAT). In this paper, a fast timing acquisition method is proposed, using the multilayer synchronization sequence based on cyclical codes. Specifically, the transmitted preamble is the Kronecker product of Bose–Chaudhuri–Hocquenghem (BCH) codewords and PN sequences. At the receiver, the cyclical nature of BCH codes is exploited to test only a part of the entire sequence, resulting in shorter acquisition time. The algorithm is evaluated using the metrics of MAT and detection probability (DP). Theoretical expressions of MAT and DP are derived from the constant false-alarm rate (CFAR) criterion. Theoretical analysis and simulation results show that our proposed scheme dramatically reduces the acquisition time while achieving similar DP performance and maintaining a reasonably low real-time hardware implementation complexity, in comparison with the SS scheme.**

***Index Terms*—Bose–Chaudhuri–Hocquenghem (BCH) code, code acquisition, hierarchical preamble, pseudonoise (PN) sequence, timing synchronization.**

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J. Zhang, N. Ge, and Z. Wang are with the Tsinghua National Laboratory for Information Science and Technology and Co-innovation Laboratory of Aerospace Broadband Network Technology, Tsinghua University, Beijing 100084, China (e-mail: zhangjq06@mails.tsinghua.edu.cn; gening@tsinghua.edu.cn; zcwang@tsinghua.edu.cn).

S. Chen is with the Electronics and Computer Science, University of Southampton, Southampton SO17 1BJ, U.K., and also with the Faculty of Engineering, King Abdulaziz University, Jeddah 21589, Saudi Arabia (e-mail: sqc@ecs.soton.ac.uk).

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I. Introduction

For a wireless communication system, timing synchronization is the first key operation at the receiver. To combat with the situations of extremely low SNR caused by adverse jamming, such as in military wireless systems, very long pseudonoise (PN) sequences are usually used as preamble sequences because of their good correlation property [1]. At the receiver, correlation and search are performed to acquire the phase of the incoming sequence. This is often accomplished in two stages: acquisition and tracking. At the acquisition stage, a coarse timing alignment of the locally generated replica with the received signal is performed to guarantee that the phase of the incoming sequence is within the locking range of the tracking stage. In this paper, we focus on the first stage, i.e., the acquisition problem.

Conventional acquisition methods include full parallel search (FPS), serial search (SS), and hybrid search (HS). FPS is not suitable for antijamming communication applications due to its excessive real-time hardware implementation complexity [2]. On the other hand, SS is simple to implement but suffers from the drawback of long mean acquisition time (MAT) [3], [4]. The difficulty associated with SS becomes intolerable when the synchronization sequence is very long [5]. An HS scheme may be viewed as a search method that attempts to strike a compromise between the FPS and SS, in terms of a tradeoff between hardware complexity and MAT performance [6].

To improve the MAT performance, in [7] and [8], acquisition schemes in which the preamble sequences are viewed as codewords are proposed, and the acquisition problem is reformulated as a decoding problem. An iterative message passing (IMP) algorithm or a soft-in–soft-output decoding algorithm can be then used to decode the information bits from the received sequence. The problem associated with this approach is that the IMP method is usually stuck at the local optima because of the cyclical and regular nature of the constructed tanner graph. The real-time hardware implementation complexity of this approach is also extremely high because iterative soft decoding has to be implemented [9].

In this paper, a fast and low-complexity code-acquisition method is proposed. The proposed method is well suited for military systems, but it is equally applicable to other communication systems where a long PN code is needed and where fast acquisition is required. Instead of using PN sequences, a multilayer preamble code design is advocated. The proposed code is the Kronecker product of a Bose–Chaudhuri–Hocquenghem (BCH) code and a PN sequence. The initial phase of the received sequence can be computed by partial correlation and hard-decision decoding. Consequently, the acquisition time of our algorithm is greatly reduced, compared with the conventional SS algorithm, whereas our algorithm achieves a significantly lower real-time hardware implementation complexity, in comparison with the HS algorithm. The proposed method is also different from the one used in the Third Generation Partnership Project [10], where the acquisition is based on hierarchical matched filtering. In our proposed acquisition method, instead of searching for the maximum peak in all the correlation values, hard-decision decoding is used to compute the initial phase of the received sequence. Taking advantage of the cyclical characteristic of BCH codes, only a part of the positions needs to be tested, and this results in low-complexity implementation of timing acquisition.

The rest of this paper is organized as follows. Section II describes our proposed preamble design and timing acquisition algorithm, whereas Section III provides the detailed performance analysis of our acquisition algorithm. Section IV presents the performance evaluation of our proposed design using simulation, whereas our conclusions are summarized in Section V.

II. Proposed Design

A. Synchronization Sequence

The generation of the synchronization sequence includes two steps. First, a $(n,\ k)$ BCH codeword is selected, which is known to both the transmitter and the receiver. Denote the generator matrix of this BCH code as $\mathbf{G}$. The transmitted codeword can be written as $\mathbf{c_t} = \mathbf{x_t}\mathbf{G}$, where $\mathbf{x_t} = [x_0,\ x_1, \ldots,\ x_{k-1}]$, $x_i \in GF(2)$ for $0 \le i \le k-1$, and $\mathbf{c_t} = [c_0,\ c_1,\ \ldots,\ c_{n-1}]$. The binary phase-shift keying (BPSK) modulated sequence of $\mathbf{c_t}$ is denoted by

$$\mathbf{s_t} = [s_0,\ s_1,\ \ldots,\ s_{n-1}] \tag{1}$$

with $s_i = (-1)^{c_i}, 0 \le i \le n-1$. The second step is to spread the modulated symbols with a PN sequence. We use a maximum-length feedback shift register generated sequence (m-sequence) as the spreading sequence, which can be written as $\mathbf{w} = [w_0,\ w_1,\ \ldots,\ w_{M-1}]$ with $w_i \in \{-1, 1\}$ for $0 \le i \le M-1$. The synchronization sequence can therefore be written as $K(\mathbf{s_t}, \mathbf{w})$, where $K(\cdot)$ denotes the Kronecker product operator. It can be seen that this synchronization sequence has a length of $L = nM$.

Assuming that the synchronization sequence is repeatedly sent, the transmitted synchronization sequence signal can be written as [11]

$$s(t) = \sum_{j=0}^{\infty}\sum_{i=0}^{n-1}\sqrt{E_c}s_i\sum_{k=0}^{M-1}w_k g_c(t - iMT_c - kT_c - jnMT_c) \tag{2}$$

where w_k is the kth chip of the m-sequence, E_c is the chip power, T_c is the chip period, and $g_c(t)$ is the chip shaping pulse. It can be seen that the preamble signal $s(t)$ is periodic with period LT_c, where $L = nM$. If the communication link can be modeled as an additive white Gaussian noise (AWGN) channel, the received preamble signal can be written as

$$r(t) = s(t-\tau) + \varepsilon(t) \tag{3}$$

where τ is the time delay to be estimated, and $\varepsilon(t)$ is the channel's AWGN with power spectral density $N_0/2$. When jamming is present in the link, the received jamming signal can be also modeled as Gaussian noise as the jamming signal will be despread to the whole frequency band after the correlation process [1], [11], [12].

The sampling period at the receiver is assumed to be $T_s = T_c/N$, where N indicates the oversampling rate. At the acquisition stage, however, the receiver observes the received signal at a time interval of T_c with the step of T_s, i.e., sampling $r(t)$ at period T_c and when the acquisition fails, shifting the sampling position by T_s. As the locking range of the tracking loop is usually $T_c/2$, a successful acquisition can be declared if the estimated time delay $\widehat{\tau}$ satisfies $|\widehat{\tau} - \tau| \le T_c/2$. The perfect sampling position can be estimated at the tracking stage, provided that there is a sufficient number of samples per chip, i.e., N is sufficiently large [13]. Therefore, it is reasonable to assume that the sampling position is perfect in the acquisition stage to simplify the analysis.

Assuming that the time delay is $\tau = dT_c$, and letting $p = \lfloor (d/M) \rfloor$ and $q = d - pM$, the observed sequence has the form of

$$\begin{aligned}\mathbf{r_i} = [&r(iLT_c),\ r((iL+1)T_c), \ldots, r((iL+M-1)T_c)\\ &r((iL+M)T_c), \ldots, r((iL+L-1)T_c)]\\ = [&\mathbf{a}_0,\ \mathbf{a}_1, \ldots, \mathbf{a}_{n-1}]\end{aligned} \tag{4}$$

where $\mathbf{a}_l$, $0 \le l \le n-1$ is the vector of length M given by

$$\begin{aligned}\mathbf{a}_l = [&r((iL+lM)T_c),\ r((iL+lM+1)T_c)\\ &\ldots, r((iL+lM+M-1)T_c)].\end{aligned} \tag{5}$$

Since $r(t) = s(t-\tau) + n(t)$ and $s(t)$ is periodic with the period LT_c, we have

$$\begin{aligned}\mathbf{a}_l &= [s((lM-d)T_c),\ s((lM+1-d)T_c)\\ &\qquad \ldots, s(((l+1)M-(d+1))T_c)]\\ &\quad + [\varepsilon(lMT_c),\ \varepsilon((lM+1)T_c),\\ &\qquad \ldots, \varepsilon(((l+1)M-1)T_c)]\\ &= \mathbf{s}_l + \boldsymbol{\varepsilon}_l\end{aligned} \tag{6}$$

where

$$\begin{aligned}\mathbf{s}_l = E_c[&s_{l-p}w_q, s_{l-p}w_{q+1}, \ldots, s_{l-p}w_{M-1}, s_{l-p+1}w_0\\ &s_{l-p+1}w_1, \ldots, s_{l-p+1}w_{q-1}].\end{aligned} \tag{7}$$

B. Acquisition Algorithm

As we aim for a rapid timing acquisition, a coherent detection approach is assumed for simplicity [14]. The diagram of the proposed synchronization scheme is shown in Fig. 1. The key idea of our design is to break up the filtering computation into partial correlation. Unlike the design used in [10], the second-layer sequence of our design is the BCH code. Therefore, the BCH decoder is adopted, instead of a second-layer matched filter, as used in [10]. Due to the cyclical property of BCH codes, the decoding will be successful once the first layer sequence is aligned.

The decision variable for each symbol is generated by correlating $\mathbf{a}_l$ with $\mathbf{w}$. Denote the decision variable for the lth symbol as v_l, where $0 \le l \le n-1$. We have

$$v_l = \mathbf{a}_l\mathbf{w}^T = \mathbf{s}_l\mathbf{w}^T + z_l \tag{8}$$

where $(\cdot)^T$ denotes the transposition operator, and $z_l = \boldsymbol{\varepsilon}_l\mathbf{w}^T$ is a Gaussian-distributed random variable with zero mean and variance MN_0. The decision variables for $\mathbf{r_i}$ can be written as $\mathbf{v} = [v_0,\ v_1, \ldots,\ v_{n-1}]$. Substituting (7) into (8) leads to

$$\begin{aligned}v_l = &\sqrt{E_c}\sum_{k=0}^{M-q-1}s_{l-p}w_{k+q}w_k\\ &+\sqrt{E_c}\sum_{k=M-q}^{M-1}s_{l-p+1}w_{k-M+q}w_k + z_l.\end{aligned} \tag{9}$$

Noting that $\tau = dT_c$ and $q = d - pM$, and utilizing the autocorrelation property of $\mathbf{w}$, we have

$$v_l = \begin{cases} M\sqrt{E_c}s_{l-p} + z_l, & \tau = pMT_c\\ B_M\sqrt{E_c} + z_l, & \text{otherwise.}\end{cases} \tag{10}$$

B_M is a binomial-distributed random variable, whose probability mass function is

$$P(B_M = M - 2i) = \binom{M}{i}\left(\frac{1}{2}\right)^M,\ i \in \{0, 1, \ldots, M\} \tag{11}$$

where $\binom{M}{i}$ denotes the number of combinations when selecting i elements from a set of M. We use $P(\cdot)$ to denote the probability density function for a continuous random variable and the probability mass function for a discrete random variable.

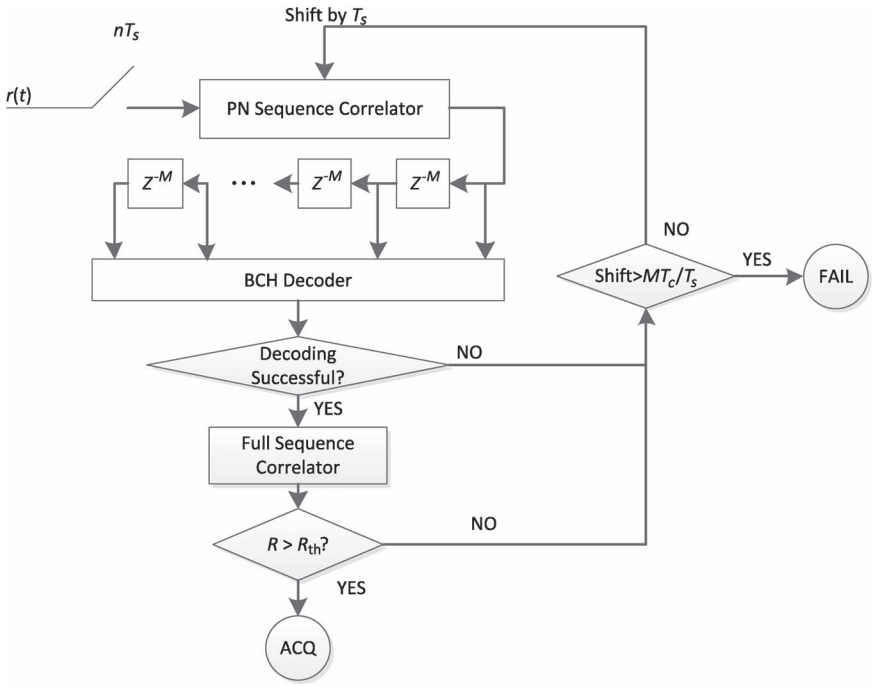

Fig. 1. System diagram of the proposed timing acquisition algorithm at receiver.

Note that the discrete binomial-distributed random variable B_M can be approximated by a continuous random variable with normal distribution [15] when M is sufficiently large, e.g., $M \geq 20$. From (9), it can be seen that the mean value of $B_M\sqrt{E_c}$ is 0, and its variance is ME_c. When the testing cell satisfies condition $\tau = pMT_c$, i.e., $q = 0$, it is referred to as an in-phase cell; otherwise, it is called an out-of-phase cell.

Denote $\mathbf{c_r} = [\widehat{c}_0, \widehat{c}_1, \ldots, \widehat{c}_{n-1}]$, where $\widehat{c}_l$ is the hard-decision bit estimated according to

$$\hat{c}_l = \begin{cases} 0, & v_l > 0 \\ 1, & \text{otherwise.} \end{cases} \tag{12}$$

It is easily seen that $\mathbf{c_r}$ takes the form of

$$\mathbf{c_r} = [c_{n-p}, c_{n-p+1}, \ldots, c_{n-1}, c_0, c_1, \ldots, c_{n-p-1}] + [e_0, e_1, \ldots, e_{n-1}]. \tag{13}$$

The first part of $\mathbf{c_r}$ is a cyclically shifted version of $\mathbf{c_t}$ given by

$$\rho(\mathbf{c_t}, p) = [c_{n-p}, c_{n-p+1}, \ldots, c_{n-1}, c_0, c_1, \ldots, c_{n-p-1}]. \tag{14}$$

According to the cyclical properties of BCH codes, $\rho(\mathbf{c_t}, p)$ is also a legal codeword of the chosen (n, k) BCH code. The second part of $\mathbf{c_r}$ is an error pattern. The number of nonzero elements in $\mathbf{e} = [e_0, e_1, \ldots, e_{n-1}]$ is the number of the errors occurred, which is denoted by N_e. Let the number of correctable errors for the chosen BCH code be N_c. All the errors in $\mathbf{c_r}$ can be corrected, as long as $N_e \leq N_c$. Denote the BCH decoded codeword by $\mathbf{c_d} = [\widetilde{c}_0, \widetilde{c}_1, \ldots, \widetilde{c}_{n-1}]$. Suppose that the testing cell is an in-phase cell and that the BCH decoding succeeds. Then, we have $\mathbf{c_d} = \rho(\mathbf{c_t}, p)$.

There are two ways to estimate p if the transmitted codeword is known to the receiver. The basic idea is to locate $\mathbf{x_t}$ in $\mathbf{c_d} = \rho(\mathbf{c_t}, p)$. Once $\mathbf{x_t}$ is located, p can be determined according to (14). For a systematic BCH code, $\mathbf{x_t} = [c_0, \ c_1, \ldots, c_{k-1}]$, and the first kth symbol in $\rho(\mathbf{c_t}, p)$ uniquely indicates p. Therefore, the position of p can be simply determined by shifting and comparison. The other method is to use a lookup table (LUT). The first method is simple but requires a small amount of processing time that will not exceed nT_c. The second method does not need extra processing time, but ROM is required to implement the LUT. However, since only n positions need to be looked into, the size of this ROM is negligible. Therefore, the LUT approach may be favorable when rapid synchronization is required.

To confirm that there is a preamble signal, the correlation between the decoded signal and the received signal is calculated. The local template is generated as $\mathbf{y} = K(\mathbf{s_d}, \mathbf{w})$, where $\mathbf{s_d} = [\widetilde{s}_0, \widetilde{s}_1, \ldots, \widetilde{s}_{n-1}]$ with $\widetilde{s}_i = (-1)^{\widetilde{c}_i}$ for $0 \leq i \leq n-1$. The correlation value between $\mathbf{y}$ and $\mathbf{r}_i$ is given by

$$R = \mathbf{r_i}\mathbf{y}^T. \tag{15}$$

The state of acquisition is declared when the following condition is met:

$$R > R_{\text{th}} \tag{16}$$

where R_{th} is the threshold value calculated according to the required constant false-alarm rate (CFAR). When the testing cell is an in-phase cell and $\mathbf{c_d}$ is correctly decoded, this is a true acquisition. However, when the testing cell is an out-of-phase cell, each element in $\mathbf{s_d}$ randomly takes the value from $\{-1, 1\}$. Then, condition (16) gives a false confirmation of acquisition. We will further address the FAR, the probability of detection, and the choice of the threshold value R_{th} in the following.

If the decoding process fails or the confirmation of preamble signal fails, the observed sequence will be cyclically shifted by T_s, and the decoding process or the correlation is repeated. If the incoming sequence is a preamble sequence, a successful timing acquisition should be declared with at most MT_c/T_s shifts. Therefore, if no acquisition can be declared after MT_c/T_s shifts, it is considered as a failed acquisition.

III. Performance Analysis

Here, the detection probability (DP) and the FAR of the proposed timing acquisition scheme are analyzed based on the Neyman–Pearson

criterion [16]. We will also derive the MAT and complexity of our algorithm and discuss the choice of the threshold value $R_{\rm th}$ in the acquisition confirmation.

A. FAR and DP

The false alarm happens when the testing cell is out of phase but is mistaken as an in-phase cell. In this case, the decision variable v_l for the lth symbol takes the form of

$$v_l = \overline{B}_M + z_l \tag{17}$$

where $\overline{B}_M$ can be modeled as a Gaussian random variable with zero mean and variance ME_c. Therefore, v_l can be modeled by a Gaussian random variable with zero mean and variance of $ME_c + MN_0$. The hard decision $\widetilde{s}_l$ for the lth symbol has the probability mass function of

$$P(\tilde{s}_l = -1) = P(\tilde{s}_l = 1) = P(v_l > 0) = \frac{1}{2} \tag{18}$$

since $\widetilde{s}_l$ takes the value randomly from $\{-1, 1\}$. Therefore, the false alarm happens when this random sequence $\mathbf{v}$ is decoded as $\mathbf{c_t}$ or $\rho(\mathbf{c_t}, j)$, and the condition $R > R_{\rm th}$ holds. The FAR for the first part is given as

$$P_{\rm fd} = 2^{k-n} \sum_{i=0}^{N_c} \binom{n}{i} \tag{19}$$

where N_c is the number of errors that can be corrected by the BCH decoding. According to the central limit theorem, R can be modeled as a Gaussian random variable with zero mean and variance $\sigma^2 = LE_c + LN_0$. Therefore, under the assumption that the two events, i.e., $\mathbf{v}$ is decoded as $\rho(\mathbf{c_t}, j)$ and $R > R_{\rm th}$ holds, are independent, the overall FAR is given by

$$\begin{aligned} P_{\rm fa} &= P_{\rm fd} \int_{R_{\rm th}}^{\infty} \frac{1}{\sqrt{2\pi\sigma^2}} \exp\left(-\frac{x^2}{2\sigma^2}\right) dx \\ &= P_{\rm fd} \cdot \frac{1}{2} {\rm erfc}\left(\frac{R_{\rm th}}{\sqrt{2(LE_c + LN_0)}}\right) \end{aligned} \tag{20}$$

where the complementary error function ${\rm erfc}(x)$ is defined by

$${\rm erfc}(x) = \frac{2}{\sqrt{\pi}} \int_{x}^{\infty} e^{-\tau^2} d\tau. \tag{21}$$

It is important to point out that, in the CFAR scenario, it is required that $P_{\rm fa} < C_{\rm fa}$, where $C_{\rm fa}$ is a very small constant (e.g., 10^{-5}). In this case, when $P_{\rm fd} < C_{\rm fa}$, there is no need to confirm by correlation as it is guaranteed that $P_{\rm fa} \le P_{\rm fd} < C_{\rm fa}$.

On the other hand, a successful detection will happen only when the decoding succeeds and the correlation test $R > R_{\rm th}$ is true. In this case, we have $\mathbf{r_i} = \mathbf{y} + \boldsymbol{\varepsilon_i}$, where $\boldsymbol{\varepsilon_i} = [\varepsilon_0, \varepsilon_1, \ldots, \varepsilon_{L-1}]$, and each element of $\boldsymbol{\varepsilon_i}$ is a white Gaussian random variable with variance N_0. As a result, we have $R = L\sqrt{E_c} + z_r$, where z_r is a Gaussian random variable with zero mean and variance LN_0. Therefore, the DP can be written as

$$\begin{aligned} P_d &= P_{\rm dec} \int_{R_{\rm th}}^{\infty} \frac{1}{\sqrt{2\pi LN_0}} \exp\left(-\frac{(x - L\sqrt{E_c})^2}{2LN_0}\right) dx \\ &= P_{\rm dec} \cdot \frac{1}{2} {\rm erfc}\left(\frac{R_{\rm th} - L\sqrt{E_c}}{\sqrt{2LN_0}}\right) \end{aligned} \tag{22}$$

where $P_{\rm dec}$ is the probability of successful BCH decoding. As decoding will succeed only when there are no more than N_c errors in $\mathbf{c_r}$, $P_{\rm dec}$ can be expressed as

$$P_{\rm dec} = \sum_{j=0}^{N_c} \binom{n}{j} (P_e)^j (1 - P_e)^{n-j} \tag{23}$$

where P_e is the symbol error rate (SER) in making the hard decision (12). As the modulation scheme (1) is the BPSK, the SER can be written as

$$P_e = \frac{1}{2} {\rm erfc}\left(\sqrt{\frac{ME_c}{N_0}}\right). \tag{24}$$

Under the CFAR requirement of $P_{\rm fd} < C_{\rm fa}$, the DP will be simplified as $P_d = P_{\rm dec}$.

Incidentally, the threshold value $R_{\rm th}$ is set or chosen according to the given CFAR. More specifically, given the required FAR $C_{\rm fa}$, $R_{\rm th}$ is simply chosen so that the overall FAR defined in (20) satisfies $P_{\rm fa} < C_{\rm fa}$.

B. MAT and Complexity

Noting that the channel-induced time delay τ in (3) can be view as a uniformly distributed random variable in $(0, nMT_c)$ and the proposed algorithm declares whether timing acquisition is successful or not with at most M operational steps, the MAT of the proposed algorithm can be derived as follows, based on the same analysis approach of [17]:

$$E\{T_{\rm acq}^{\rm Pro.}\} = \sum_{k=0}^{\infty} \left(knM + \sum_{i=1}^{M} \frac{M-i}{M}\right) P_d (1 - P_d)^k. \tag{25}$$

As a comparison, the operational procedure flowchart of the SS algorithm can be found in [4], and the MAT of the conventional SS algorithm is given by [4]

$$E\{T_{\rm acq}^{\rm SS}\} = \sum_{k=0}^{\infty} \left(kL + \sum_{i=1}^{L} \frac{L-i}{L}\right) P_d (1 - P_d)^k. \tag{26}$$

Considering the most optimistic case of $P_d = 1$, the MAT for our proposed algorithm is $M + 1/2$, and the acquisition time of the SS algorithm is $nM/2$, whereas the acquisition time of the FPS algorithm is of course 1 [7], but its implementation complexity can be excessive.

We evaluate the hardware implementation complexity of an acquisition algorithm by the number of required logic units, denoted by N_L, which includes all required two-input AND gates, two-input OR gates, and inverters. We further assume that an addition is implemented by eight-bit adder, which requires at least 40 logic units to construct, whereas a multiplication is implemented by a six-bit multiplier, which needs 180 logic units to construct [18]. We now detail the hardware implementation complexity for the proposed algorithm, the SS, the FPS using the fast Fourier transform (FFT), and the HS with $N_p = n$ parallel correlators.

1) *The proposed algorithm*. As shown in Fig. 1, the main required hardware modules for the proposed algorithm are the correlator and the BCH decoder, and the complexity of the other modules is negligible. All the operations of the correlator are additions as multiplying by ± 1 is equivalent to adding. Thus, this correlator of length nM requires nM adders, which needs 40 nM logic units to construct. According to [19], the upper bound of logic units needed in BCH decoder is $(45N_c^2 + 4N_c n)(\log_2 n)^2$, for (n, k) BCH codes. Therefore, the total complexity of the proposed algorithm is $N_L = 40nM + (45N_c^2 + 4N_c n)(\log_2 n)^2$.

TABLE I
COMPARISON OF ACQUISITION TIME, MAT, AND HARDWARE COMPLEXITY IN TERMS OF THE NUMBER OF LOGIC UNITS REQUIRED N_L. THE FFT USED IN THE FPS IS RADIX-8 512 FFT. THE NUMERICAL VALUES IN BRACKETS CORRESPOND TO THE TYPICAL VALUES IN THE CASE OF $n = 31$ AND $M = 15$, AND $N_c = 7$ IN THE $(n = 31, k = 6)$ BCH CODE

Algorithm	MAT/T_c	Hardware Complexity N_L
SS	$nM/2$ (232.5)	$40nM$ (18600)
FPS using FFT	1	$180nM + 2147040$ (2.23×10^6)
HS with $N_p = n$	$M/2$ (7.5)	$40n^2M$ (5.76×10^5)
Proposed	$M/2$ (7.5)	$40nM + (45N_c^2 + 4N_c n)(\log_2 n)^2$ (9.4×10^4)

2) *The SS*. The SS algorithm is implemented by the correlator of length nM; therefore, its complexity is simply given by $N_L = 40\,nM$.
3) *The FPS using FFT*. The algorithm requires two FFTs [one FFT and one inverse FFT (IFFT)] and one correlator of length nM (to multiply the FFT of the received signal with the FFT of the local template). As the numbers of adders and multipliers needed for implementing FFT depend on the size of FFT and how FFT is computed, we assume that the FFT implemented in the FPS algorithm is the Radix-8 512 FFT. According to [20], the number of adders required for Radix-8 512 FFT is 12°420, and the number of multipliers needed is 3204. Note that the correlator of the FPS requires nM multipliers and not nM adders. Therefore, the complexity of the FPS algorithm is given by $N_L = 180nM + 40 \times 2 \times 12\,420 + 180 \times 2 \times 3204$.
4) *The HS with* $N_p = n$. With the n parallel correlators, each having the length nM, the complexity of the HS algorithm is given by $N_L = 40\,n^2M$.

Table I compares the hardware implementation requirements of the four algorithms. The MAT of each algorithm normalized by the chip duration T_c is also summarized in Table I. We also present the typical values of the MAT and N_L of each algorithm corresponding to the case of $n = 31$ and $M = 15$ in brackets. The FPS algorithm can achieve timing acquisition within the single period of T_c. However, its hardware implementation complexity is too high. It is shown in Table I that the MAT of the SS scheme is unacceptably long, but its hardware implementation complexity is very favorable. Our proposed timing acquisition algorithm is n times faster than the SS algorithm while maintaining a reasonably low hardware implementation complexity. In comparison with the HS scheme that has a similar MAT, the proposed algorithm significantly reduces the hardware implementation complexity for timing acquisition.

IV. SIMULATION RESULTS

A simulation study is carried out to compare the achievable performance of the proposed timing acquisition algorithm with those of the SS algorithm presented in [3]. In the simulation, the SNR is defined as SNR $= 2E_c/N_0$. The MATs of the two schemes are compared in Fig. 2, where the proposed algorithm uses a (31, 5) BCH code, and the length of the spreading sequence is chosen to be $M = 15$ and 31, respectively, whereas the length of the preamble sequence used in the SS is set to 465 and 961, respectively, for fair comparison. The results of both theoretical analysis and numerical simulation are presented in Fig. 2, which confirm that the MAT obtained by simulation agrees with the theoretical analysis. Equations (25) and (26) indicate that, when $P_d = 1$ (the optimistic case), the acquisition time depends on the initial phase of the received sequence. Since the initial phase is uniformly

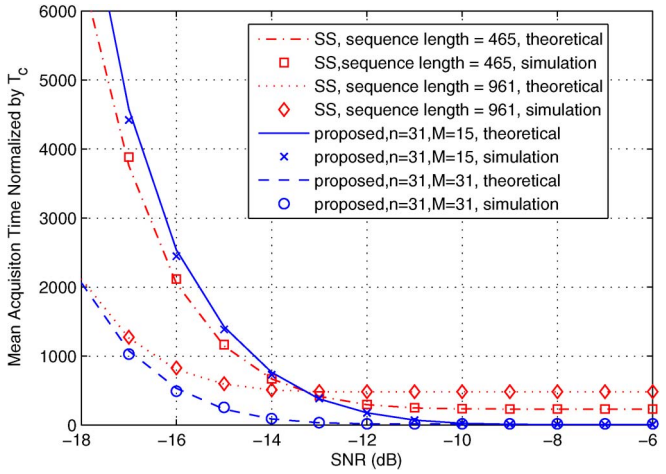

Fig. 2. Comparison of the MATs achieved by the proposed timing acquisition algorithm and the serial search algorithm, where $C_{\rm fa}$ is set to 10^{-5}. The length of the simulated preamble is set to 465 and 961, respectively, whereas the SNR is defined as SNR $= 2E_c/N_0$.

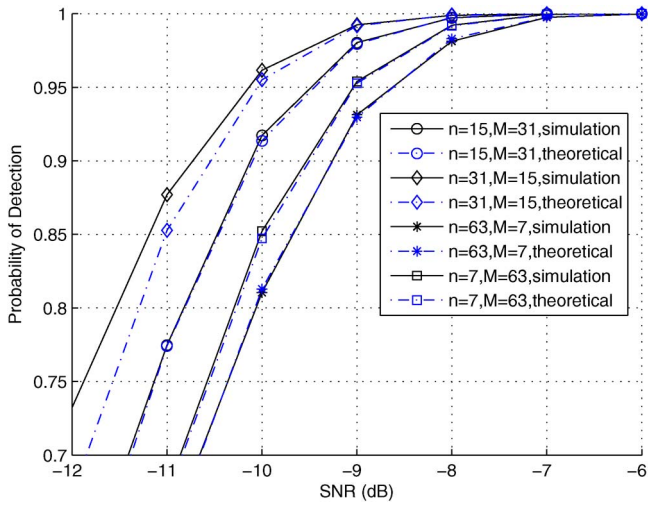

Fig. 3. Comparison of the theoretical DP and the DP obtained by the proposed algorithm in simulation with different choices of n and M for the given $L \approx 500$ (more precisely 465 and 441, respectively), where the SNR is defined as SNR $= 2E_c/N_0$.

distributed over $[0, nMT]$, for the SS acquisition, the MAT is $nM/2$ at the optimistic case. By contrast, the MAT of the proposed method is $M/2$ at the optimistic case. Both methods will converge to their respective optimistic MAT values, when the SNR becomes sufficiently large. In the case of the preamble sequence length $L = 456$, the proposed scheme has a longer MAT in comparison with the SS scheme for SNR ≤ -13 dB, whereas the MAT of our algorithm becomes shorter than that of the SS algorithm for SNR > -13 dB. In practice, it is required that $P_d > 90\%$. Otherwise, the bit error rate or throughput performance will be unsatisfactory because of an unacceptable number of packet losses. It can be shown that SNR ≤ -13 dB corresponds to the situation of $P_d \leq 0.9$, which is undesirable for a practical system to operate. For the preamble sequence length $L = 961$, our proposed algorithm achieves faster MAT than the SS algorithm over the range of SNR values SNR ≥ -18 dB tested, as shown in Fig. 2.

Figs. 3 and 4 show the DP achieved by the proposed algorithm with the preamble sequence length L set to approximately 500 and 1000, respectively, where $C_{\rm fa}$ is chosen to be 10^{-5}. Both the theoretical DP calculated using (22) and the DP obtained by the simulation are

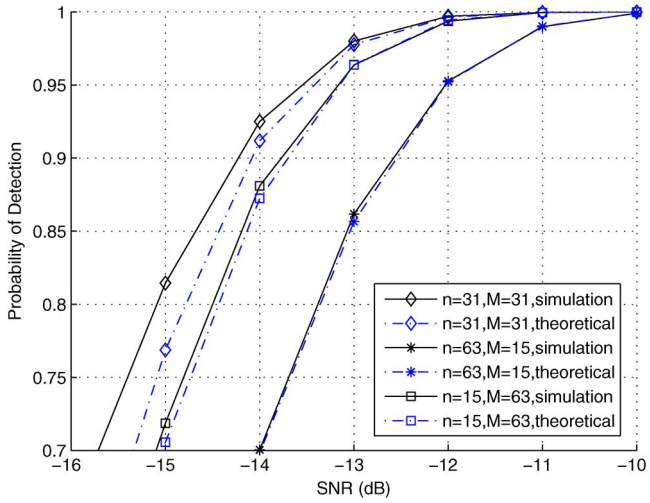

Fig. 4. Comparison of the theoretical DP and the DP obtained by the proposed algorithm in simulation with different choices of n and M for the given $L \approx 1000$ (more precisely 961 and 945, respectively), where the SNR is defined as $\text{SNR} = 2E_c/N_0$.

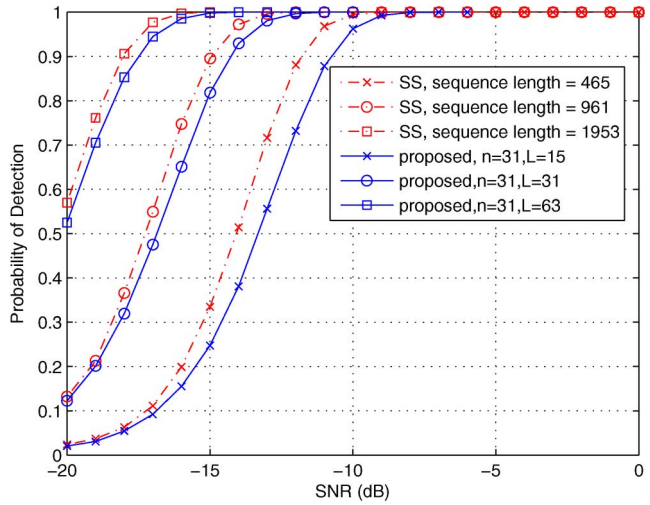

Fig. 5. Comparison of the DP performance of the proposed algorithm with the serial search algorithm, where the SNR is defined as $\text{SNR} = 2E_c/N_0$. The spreading sequence used in companion is a Zadoff–Chu sequence and not a PN sequence.

shown in Figs. 3 and 4, where it can be seen that the theoretical DP and the simulated DP agree with each other well. This confirms the accuracy of the theoretical performance analysis. For a given preamble sequence length L, there are several different combinations of the BCH codeword length n and the spreading sequence length M, which trade off error correction ability with spreading gain. In terms of DP performance, we observe in Figs. 3 and 4 that the optimal choice of n is $n = 31$ for both the cases of $L \approx 500$ and $L \approx 1000$.

Fig. 5 compares the DP performance of the proposed algorithm with that of the SS algorithm. The BCH code length in the proposed algorithm is set to $n = 31$. The spreading sequence used is a Zadoff–Chu sequence [21], which is a type of constant amplitude zero–autocorrelation waveforms. The simulation results show that the DP of the proposed algorithm is slightly worse than the SS algorithm, particularly in the case of the short preamble length of $L \approx 500$. Fig. 5 also shows that doubling the preamble sequence length results in a gain of approximately 3 dB in the SNR for the both algorithms. Moreover, the DP performance gap between the two algorithms reduces as the preamble sequence length increases, and the DP performance of the proposed algorithm becomes similar to that of the SS algorithm for long preamble sequence. Thus, by choosing appropriate code length and spreading sequence length, the proposed approach can attain a similar DP performance to the SS with the benefits of greatly reduced acquisition time.

V. Conclusion

A preamble design has been proposed, which adopts a novel multilayer sequence generated by the Kronecker product of the BCH code and the PN sequence as the synchronization sequence, for fast low-complexity timing acquisition under extremely low SNR environments. At the receiver, the channel time delay can be estimated by first partially correlating the received sequence with the local spreading sequence, followed by decoding using a simple hard-decision decoding algorithm. The cyclical property of BCH codes is exploited to accelerate the time acquisition process. Theoretical analysis and simulation investigation demonstrate that our proposed method dramatically reduces the acquisition time, while achieving a similar DP performance and maintaining low implementation complexity, compared with the widely used serial search timing acquisition scheme.

References

[1] R. A. Poisel, *Modern Communications Jamming: Principles and Techniques*, 2nd ed. Norwood, MA, USA: Artech House, 2011.
[2] E. A. Sourour and S. C. Gupta, "Direct-sequence spread-spectrum parallel acquisition in a fading mobile channel," *IEEE Trans. Commun.*, vol. 38, no. 7, pp. 992–998, Jul. 1990.
[3] H. Li, X. Cui, M. Lu, and Z. Feng, "Dual-folding based rapid search method for long PN code acquisition," *IEEE Trans. Wireless Commun.*, vol. 7, no. 12, pp. 5286–5296, Dec. 2008.
[4] A. Polydoros and C. Weber, "A unified approach to serial search spread-spectrum code acquisition-Part I: General theory," *IEEE Trans. Commun.*, vol. 32, no. 5, pp. 542–549, May 1984.
[5] J. G. R. Delva and I. Howitt, "PN acquisition for DS/SS using a preloop parallel binary search phase estimator and a closed-loop selective search subsystem," *IEEE Trans. Wireless Commun.*, vol. 3, no. 2, pp. 408–417, Mar. 2004.
[6] W. Zhuang, "Noncoherent hybrid parallel PN code acquisition for CDMA mobile communications," *IEEE Trans. Veh. Technol.*, vol. 45, no. 4, pp. 643–656, Nov. 1996.
[7] K. M. Chugg and M. Zhu, "A new approach to rapid PN code acquisition using iterative message passing techniques," *IEEE J. Sel. Areas Commun.*, vol. 23, no. 5, pp. 884–897, May 2005.
[8] L. L. Yang and L. Hanzo, "Acquisition of m-sequences using recursive soft sequential estimation," *IEEE Trans. Commun.*, vol. 52, no. 2, pp. 199–204, Feb. 2004.
[9] M. P. C. Fossorier, M. Mihaljevic, and H. Imai, "Reduced complexity iterative decoding of low-density parity check codes based on belief propagation," *IEEE Trans. Commun.*, vol. 47, no. 5, pp. 673–680, May 1999.
[10] S. Sriram, K. Brown, and A. Dabak, "Low-power correlator architectures for wideband CDMA code acquisition," in *Proc. 33rd Asilomar Conf. Signals, Syst., Comput.*, Pacific Grove, CA, USA, Oct. 24–27, 1999, vol. 1, pp. 125–129.
[11] M. K. Simon, J. K. Omura, R. A. Scholtz, and B. K. Levitt, *Spread Spectrum Communications Handbook*, Electronic ed. New York, NY, USA: McGraw-Hill, 2002.
[12] Y. Liu, P. Ning, H. Dai, and A. Liu, "Randomized differential DSSS: Jamming-resistant wireless broadcast communication," in *Proc. 29th IEEE INFOCOM*, San Diego, CA, USA, Mar. 14–19, 2010, pp. 1–9.
[13] D. L. Noneaker, A. R. Raghavan, and C. W. Baum, "The effect of automatic gain control on serial, matched-filter acquisition in direct-sequence packet radio communications," *IEEE Trans. Veh. Technol.*, vol. 50, no. 4, pp. 1140–1150, Jul. 2001.
[14] M. Chiani, "Noncoherent frame synchronization," *IEEE Trans. Commun.*, vol. 58, no. 5, pp. 1536–1545, May 2010.
[15] G. E. P. Box, W. J. Hunter, and J. S. Hunter, *Statistics for Experimenters: An Introduction to Design, Data Analysis and Model Building*. New York, NY, USA: Wiley, 1978.

[16] A. Papoulis and S. U. Pillai, *Probability, Random Variables and Stochastic Processes*, 4th ed. New York, NY, USA: McGraw-Hill, 2002.
[17] V. M. Jovanovic, "Analysis of strategies for serial-search spread-spectrum code acquisition-direct approach," *IEEE Trans. Commun.*, vol. 36, no. 11, pp. 1208–1220, Nov. 1988.
[18] M. M. Mano, *Digital Logic and Computer Design*. Englewood Cliffs, NJ, USA: Prentice-Hall, 1979.
[19] B. G. Bajoga and W. J. Walbesser, "Decoder complexity for BCH codes," *Proc. Inst. Elect. Eng.*, vol. 120, no. 4, pp. 429–431, Apr. 1973.
[20] P. Duhamel and H. Hollmann, "Split radix FFT algorithms," *Electron. Lett.*, vol. 20, no. 1, pp. 14–16, Jan. 1984.
[21] C. Chu, "Polyphase codes with good periodic correlation properties," *IEEE Trans. Inf. Theory*, vol. IT-18, no. 4, pp. 531–532, Jul. 1972.

Outage Analysis of Orthogonal Space–Time Block Code Transmission in Cognitive Relay Networks With Multiple Antennas

Xing Zhang, *Member, IEEE*, Jia Xing, and Wenbo Wang, *Member, IEEE*

***Abstract*—The outage performance of cognitive relay networks (CRNs) for a decode-and-forward (DF) protocol in a spectrum sharing scenario with orthogonal space–time block code (OSTBC) transmission is presented in this paper. Both the exact formulas of the outage probability and its approximation in a high-SNR region are derived over Rayleigh fading channels. The theoretical results are validated by simulations. It shows that there is an outage saturation phenomenon due to both the maximum transmit power limit and the interference power constraint, which is similar to CRNs with a single antenna. Meanwhile, our results also show that increasing the number of antennas may not improve the outage performance when the interference power constraint or the transmit power constraint is very small; however, it will significantly improve the outage performance when the number of antennas is large enough. Through the asymptotic analysis, it shows that the CRN where the source and the relay are both equipped with N antennas can achieve full degree of diversity, i.e., $2N$-order diversity.**

***Index Terms*—Cognitive relay networks (CRNs), orthogonal space–time block code (OSTBC), outage performance.**

I. Introduction

Cognitive radio is a promising technique to improve the utilization of the scarce radio spectrum [1]. In an underlay spectrum sharing scenario [2], secondary users (SUs) are allowed to access the licensed spectrum as long as the interference to primary users (PUs) is below a tolerable threshold (e.g., an underlay approach can be utilized).

Recently, cooperative communication has been also considered as an effective means to combat channel fading by providing cooperative diversity [3]. Inspired by cooperative relaying techniques, cognitive relay networks (CRNs) [5], [6] have been proposed to improve the SUs' transmission performance. In [7], the exact outage probability of the CRN that adopt the selection decode-and-forward (DF) protocol has been derived.

As another approach to combat fading, multiple-input–multiple-output technology has attracted much attention. It can offer antenna diversity without additional bandwidth or transmit power. Based on Alamouti's two-branch transmit diversity scheme [8], orthogonal space–time block codes (OSTBCs) for an arbitrary number of antennas have been proposed in [9]. OSTBC transmission is a simple way to obtain multiantenna diversity gain. It reduces the complexity of the receiver, at which only linear processing is needed. Up to now, to the best of our knowledge, there has been very little research into CRNs employing OSTBC transmission in a spectrum sharing scenario. Performance analysis for OSTBC transmission in a nonspectrum sharing scenario with a DF relay and with an amplify-and-forward (AF) relay has been presented in [10] and [11], respectively. In [4], the performance of distributed OSTBCs is analyzed in an AF cooperative cognitive networks.

In this paper, we investigate a DF CRN with OSTBC transmission under both the maximum transmit power limit and the interference power constraint in an underlay spectrum sharing scenario. We assume that the secondary source (SS) and the secondary relay (SR) are equipped with multiple antennas, whereas the secondary destination (SD) has only one antenna due to the size and cost limitations. This configuration corresponds to the scenario where the base station (i.e., SS) communicates with the user (i.e., SD) with the help of relay nodes (i.e., SR), and due to the size and complexity, the base station and relay nodes can have multiple antennas for better performance. Based on this scenario and our previous study [6], [7], [11], the exact outage probability of the secondary system is derived over Rayleigh fading channels. Asymptotic analysis in a high-SNR regime is also presented. Specifically, the major contributions of this paper are summarized as follows.

- Exact and approximated outage probabilities are derived over Rayleigh fading channels, which are validated through simulations.
- Similar to the single-antenna scenario in [7], an outage saturation phenomenon is also found due to both the maximum transmit power limit and the interference power constraint.
- Increasing the number of antennas will not improve the outage performance when the transmit power constraint and the interference power constraint are very small, whereas when the power constraint is large enough, the number of transmit antennas have a great impact on the outage performance.

The remainder of this paper is organized as follows. In Section II, we present the system model for the analysis of CRNs with multiple antennas. Then, based on this model, in Section III, the exact outage probability is derived over Rayleigh fading channels to study the performance with variant antennas. Meanwhile, the asymptotic outage probability for a large-system SNR is derived to study the diversity order in such a system. In Section IV, simulation results are given and compared. Finally, we conclude this paper in Section V.

II. System Model

The system model we considered in this paper is shown in Fig. 1. For the secondary system, the SS node SS is equipped with N_s antennas, the SR node SR is equipped with N_r antennas, and the SD node SD has only one antenna, which coexists with a PU in an underlay approach. The SR adopts a DF cooperative protocol to

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The authors are with the School of Information and Communication Engineering, Beijing University of Posts and Telecommunications, Beijing 100876, China (e-mail: hszhang@bupt.edu.cn; wbwang@bupt.edu.cn).

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