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Phase Detector with Minimal Blind Zone and Reset Time for GSamples/s DLLs

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Abstract A new phase detector for high-speed applications is proposed in this paper. Due to their long reset path, conventional phase detectors can work in lower frequencies. However, the proposed phase detector has lower reset path delay in which makes it suitable for high-speed phase locked loops (PLL) and delay locked loops (DLL). Moreover, this new phase detector uses a few transistors. The proposed circuit is designed based on TSMC 0.13 μm CMOS Technology. Simulations show lower reset path delay, blind zone and power consumption for proposed architecture in comparison with pervious related works. In addition, the circuit is able to detect phase offsets in about 80 ps and to work properly in frequencies near 3 GHz. Its blind zone is about 120 ps, while its reset path delay is about 80 ps. Furthermore, the power consumption of the proposed circuit at 128 MHz is found to be about 134 μW.

Keywords Phase detector · High speed · Reset time · Blind zone · Low Power

1 Introduction

Increasing advances in CMOS technology have led to boosting demands for high-speed and high-performance circuits. Delay locked loops (DLLs) and phased locked loops (PLLs) are widely used in clock synchronization circuits, frequency synthesizers [5], digital transceivers, DRAMs [13], SRAMs and clock and data recovery circuits. One of the main building blocks in both DLLs and PLLs is phase detector [6]. This fact has led to increasingly significant role of phase detector in high-speed communication.

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Conventional phase detectors suffer from low speed and small frequency range of working [2,10]. Therefore, the existing challenge is to design a high-speed phase detector which can correctly function in wide frequency range. One possible solution is to use transmission gates featuring the ability to transmit both logical ONE and logical ZERO [9]. Another approach to design high-speed phase detector is to decrease the reset path delay. Since phase detector is one of the important sources of jitter in DLLs and PLLs, reducing the reset path delay and blind zone may decrease the total jitter at the output of DLLs or PLLs [4,7].

Two techniques for designing high-speed PFD were proposed in [9]. The proposed circuits of [9] were designed in 0.25 μm, and the maximum reported operating frequency was 1.25 GHz. in addition, the two proposed PFDs [9] achieved a capture range of 1.7 and 1.4 times of the conventional design, respectively. In [3], a new phase-frequency detector with minimal blind zone was reported together with, a brief analysis of blind zones in latched-based PFDs. The measured blind zone of PFD was 61 ps [3], smaller than that of the existing topologies with almost 100 ps [3]. In addition, in [11] an all-digital phase-frequency detector design, capable of accepting an infinite range of input frequency differences, is reported. This phase-frequency detector had a very low dead zone and a high maximum operating frequency; however, its deficit was a capture range of about 2π. These attempts show that designing a high-speed PFDs is still significant.

In this paper, a new low-power and high-speed phase detector enjoying a decreased total reset path delay is introduced. This new architecture functions in high frequencies up to 3 GHz. In this circuit, the total number of used transistors is cut down. The proposed architecture is designed to detect the phase differences in positive edges of clock, and the changes needed for phase detector to detect phase differences at the negative edges of clock are introduced too. In addition, 50% duty cycle, needed for many cases of previous works, is not important for this proposed architecture.

The paper is organized as follows. The following section introduces the conventional phase detector and some of its limitations. Section 3 describes the proposed high-speed phase detector. Simulation and results are presented in Sect. 4.

2 Conventional Phase-Frequency Detector

Fig. 1 shows the conventional PFD architecture widely used in PLLs and DLLs. As can be seen in Fig. 1, conventional PFD has two D-flip-flops and one NAND gate. The D-flip-flops are triggered with two PFD inputs. In other words, the two inputs which their phase differences should be determined are connected to the clock of D-flip-flops. Up and DN signals are generated by these two D-flip-flops. These two signals switch the current of charge pump and are initially low. In the first rising edge of inputs, the corresponding D-flip-flop's output is high. The state is held until the rising edge of the other input arrives. At this time, the reset path is activated and both UP and DN equal zero.

The related waveforms of PFD for conventional DLL are shown in Fig. 2 for different cases. Plus, the gate level implementation of this conventional PFD with NAND-based latches as reported in [1] is shown in Fig. 3. As can be seen in this

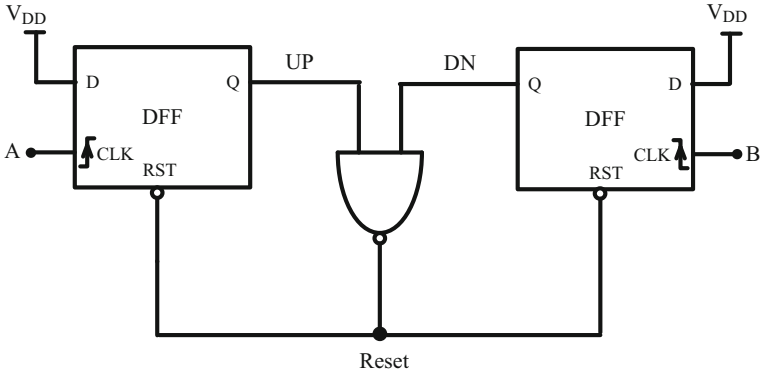


Fig. 1 Conventional PFD

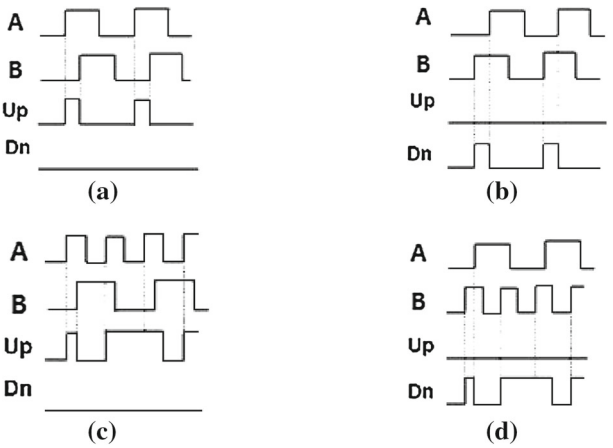


Fig. 2 Waveforms related to conventional PFDs: (**a**) when B is lagged from A, (**b**) when A is lagged from B, (**c**) when frequency of A is higher than B, and (**d**) when frequency of B is higher than A

figure, the reset path contains three two-inputs, one three-input and one four-inputs NAND gates. To have higher-speed PFDs, we need to minimize the reset path delay. In other words, the number of gates should be decreased in a reset path line. Another problem of this conventional PFD is its blind zone which increases the phase noise—in other words jitter—of DLLs or PLLs.

Considering these deficiencies, in this paper a new phase detector is proposed to remove the limitation of detecting phase offset in high-speed applications. The trick is to minimize reset path delay using new architecture for phase detectors. Minimized delay path makes a phase detector work at higher frequencies. Therefore, when it is used in PLL or DLL architecture, the whole PLL and DLL can operate at higher frequencies with a lower jitter contribution. In an ideal phase-frequency detector, the PFD's characteristics for the entire phase difference from -2π to 2π are as what is shown in Fig. 4. This figure shows that the characteristic of an ideal PFD is linear for all phase differences. In addition, when the inputs differ in frequency, the phase

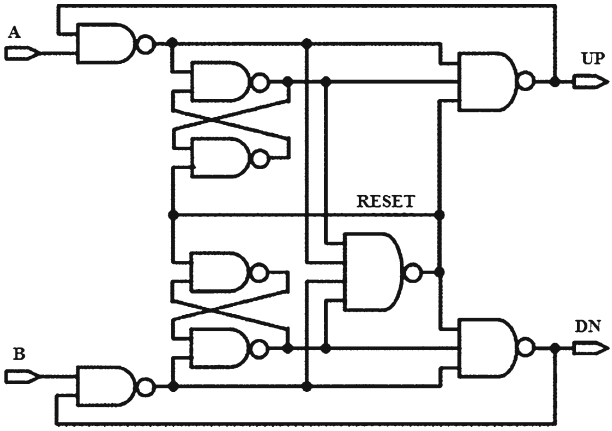
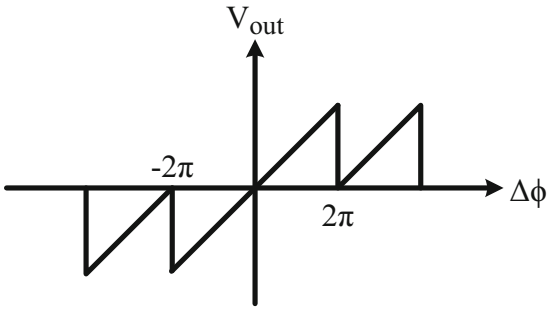


Fig. 3 Gate level implementation of conventional PFDs [1]

Fig. 4 Ideal PFD's characteristic



difference changes each cycle as follows (phase difference in radians refers to the slower clock frequency) [9]:

$$2\pi \left[\left(T_{\mathrm{CLK,Ref}} - T_{\mathrm{CLK,out}} \right) / \max \left(T_{\mathrm{CLK,Ref}}, T_{\mathrm{CLK,out}} \right) \right] \tag{1}$$

In (1), $T_{\mathrm{CLK,Ref}}$ and $T_{\mathrm{CLK,out}}$ are the periods of reference and output clocks in PLLs or DLLs (periods of the two inputs of PFD).

When the phase difference between the two inputs of real phase-frequency detector is close to 2π, the rising edge of the leading phase can fall into the reset region. During reset mode, the PFD cannot detect the leading signal, so it treats the following lagged signal as the leading one and generates reversed phase information. This is called a blind zone which is related to the reset path time of PFD. In other words, reset path delay results in a feature common to real PFDs,as shown in Fig. 5a. This figure shows that the linear behaviour of PFD is limited by reset path time and the linear range is less than 4π. These lead to a less accurate phase difference calculation. This non-accurate phase comparison happens when the phase differences of PFD inputs are more than $2\pi - \Delta$ in which Δ is defined as follows [9]:

$$\Delta = 2\pi \cdot \left[t_{\mathrm{reset}} / T_{\mathrm{CLK,Ref}} \right] \tag{2}$$

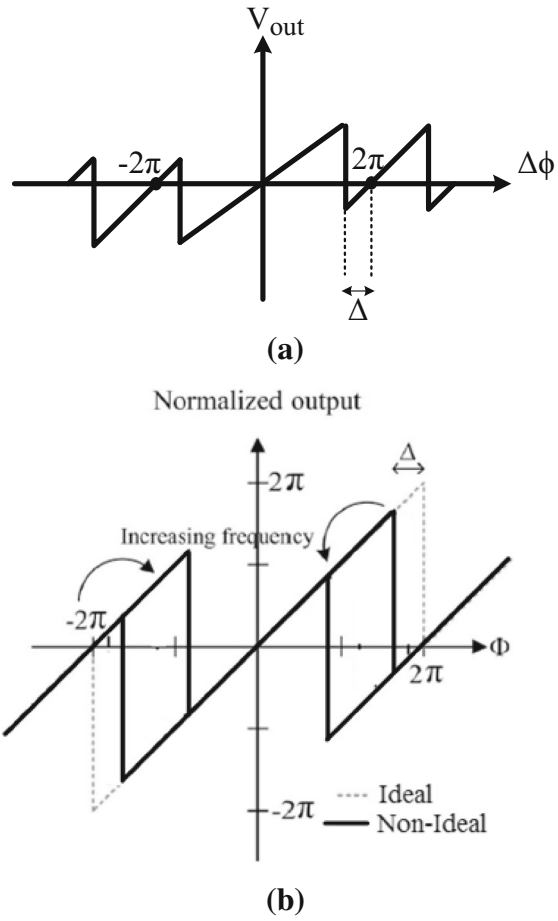


Fig. 5 **a** Non-ideal PFD characteristic, **b** typical characteristic of PFD for different frequencies [3]

In (2), t_{reset} is the reset path delay of PFD. This equation shows that non-accurate phase comparison range of PFD is related to reset path delay time and period of reference clock. Hence, lowering the reset path delay time results in a more accurate PFD which is the aim of this paper. It is worth mentioning that the ratio of $t_{\text{reset}}/T_{\text{CLK,Ref}}$ is bigger in higher frequencies since t_{reset} is almost constant and $T_{\text{CLK,Ref}}$ is lower. In other words, according to (2), for a higher frequency to have fair phase comparison ($2\pi - \Delta$ should more close to 2π), Δ should be small enough since in a higher frequency $T_{\text{CLK,Ref}}$ is small and small values for t_{reset} are needed.

During a reset process, a PFD cannot detect the leading signal, so it treats the following lagged signal as the leading one and generates reversed phase information. In addition, Fig. 5b shows the characteristic of a real PFD for different frequencies. This figure shows that at higher frequencies a blind zone and also reset path time lead to bigger Δ and more non-accurate phase comparison. According to the explanations mentioned above, this paper aims at minimizing the reset path delay time which can lead to better performance of the proposed PFD.

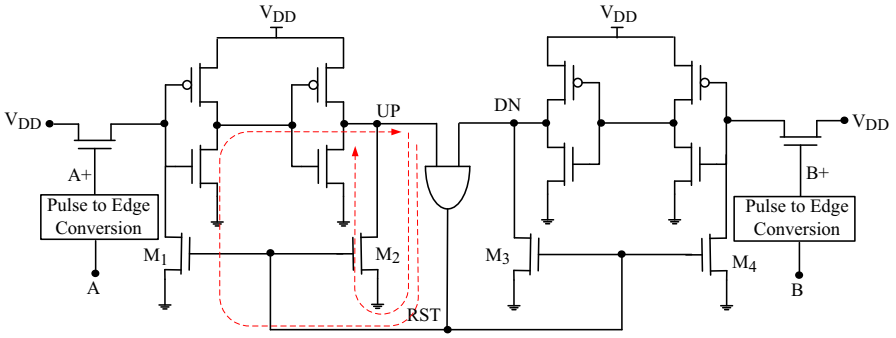


Fig. 6 Proposed phase detector

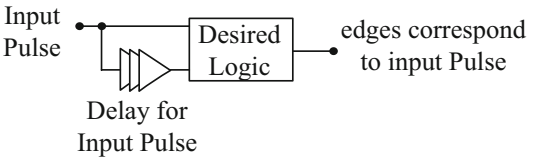


Fig. 7 Converting pulse to corresponding edges

3 Proposed Phase Detector Architecture

The proposed architecture for phase detector, shown in Fig. 6, has 14 MOS transistors (10 nMOS transistors and 4 pMOS transistor). Furthermore, one AND gate is used to reset the UP and DN signals when both of them are logical ONE. If the AND gate is designed in CMOS logic, the base of the proposed architecture needs 20 transistors (13 nMOS and 7 pMOS). In this paper, to have lower chip area, the AND gate is designed in pass transistor logic. Therefore, the proposed structure needs 16 transistors including 12 nMOS and 4 pMOS (transistors which are needed to convert pulse to edge are not considered in Fig. 6).

The manner of operation of the proposed circuit is similar to conventional PFDs. It is worth mentioning that A and B signals (the signals whose phase differences should be calculated) should be converted to A+ and B+ signals—pulses with limited width—to have good operation for proposed phase detector. In other words, the narrower A+ and B+ result in better performance for the proposed architecture. Actually, this circuit performs sampling in small width of A+ and B+. Since the paths of transmission from A+ and B+ to UP and DN are short (these paths contain two inverters and one nMOS transistor), the width of A+ and B+ can be very small (even smaller than 80 ps). The circuit which should have ability to convert pulses to edges is very simple. For example, with selecting appropriate values for delays, the topology of Fig. 7 can be used to produce enough sharp pulses from pulses with different duty cycles. It should be noted that to have positive-edge phase comparison in the proposed PFD, edges of A+ and B+ should be in line with the positive edges of A and B. If negative edge comparison is needed, edges of A+ and B+ should be in line with the negative edges of A and B.

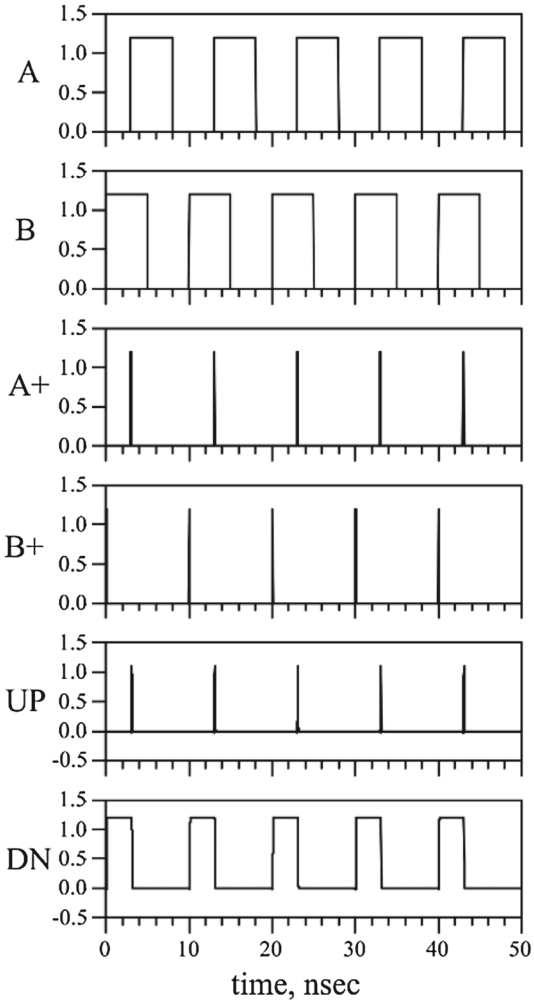


Fig. 8 Waveforms of proposed phase detector when A is lagged form B

The advantages of the proposed circuit can be enumerated as follows. First, this circuit has ability to decrease the reset path delay. As can be seen in Fig. 6, when both UP and DN are logical ONE for a short duration of time, UP and DN will go to logical ZERO from two distinct paths by two red dash line which are shown in Fig. 7. Since M_2 and M_3 are chosen stronger than other transistors, usually DN and UP signals will be logical ZERO by these transistors. In exceptional cases, when logical ONE is remained in the input of the first inverter, the reset path is activated by M_1 and M_4. Therefore, in general, a reset path will just contain a two-input AND gate and one nMOS transistor in a good design. It should be mentioned that even if the circuit works in the worst case of phase detection (resetting the circuit by M_1 and M_4), the proposed circuit still has small reset path delay. In this case, the reset path contains two minimum dimension inverters, one AND gate and a pMOS transistor. It

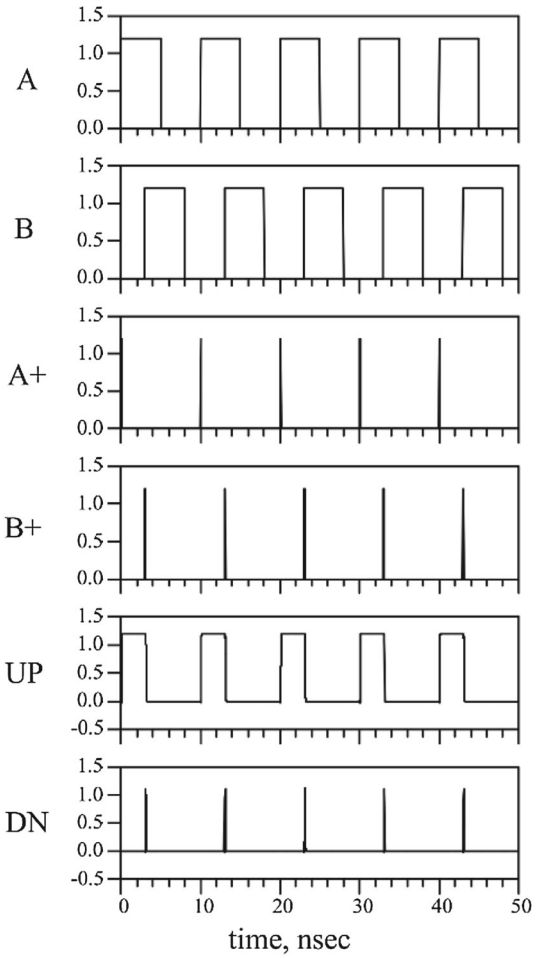


Fig. 9 Waveforms of proposed phase detector when B is lagged form A

should be noted that probability of this case is very small if the circuit is reasonably designed. Therefore, the reset path delay of the proposed circuit is much smaller than conventional PFDs even in the worst case. As will be shown in simulation section, the proposed architecture path has the ability to detect the phase differences about 80 ps by decreasing reset.

Another important advantage of this circuit is related to its low power consumption. Since the circuit is designed with TSMC 0.13 μm, CMOS technology by supply voltage of 1.2 V and a few transistors are used, the power consumption will be much smaller than similar works. In addition, design considerations for low-power circuit such as decreasing the value of capacitors to have lower dynamic power consumption are applied for this circuit.

Another advantage of this circuit is related to the number of transistors which are used for the phase detector. As mentioned before, the circuit uses fewer transistors in

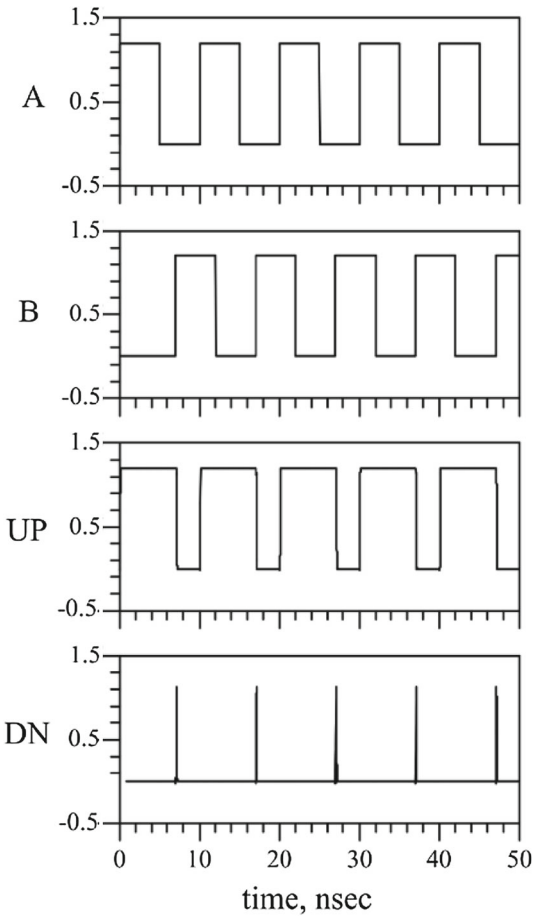


Fig. 10 Waveforms of proposed phase detector when B is lagged form A with more than T/2

comparison with conventional PFDs and other similar works [1]. This results in lower chip area in the proposed phase detector.

The other advantage of the proposed circuit is that there is no force for this architecture to have 50% duty cycle for A and B signals because the pulse to edge converter circuit can convert pulses with different duty cycles to pulses with small enough width. The other merit of the proposed circuit, small glitch time, will be introduced in simulation and results section.

4 Simulations and Results

The proposed phase detector is designed and simulated with TSMC 0.13 μm CMOS technology. Fig. 8 shows the related waveforms of the proposed architecture at 100 MHz when A lags 3 ns from B. As shown in this figure, the phase detector detects phase differences correctly in the positive edges of A and B.

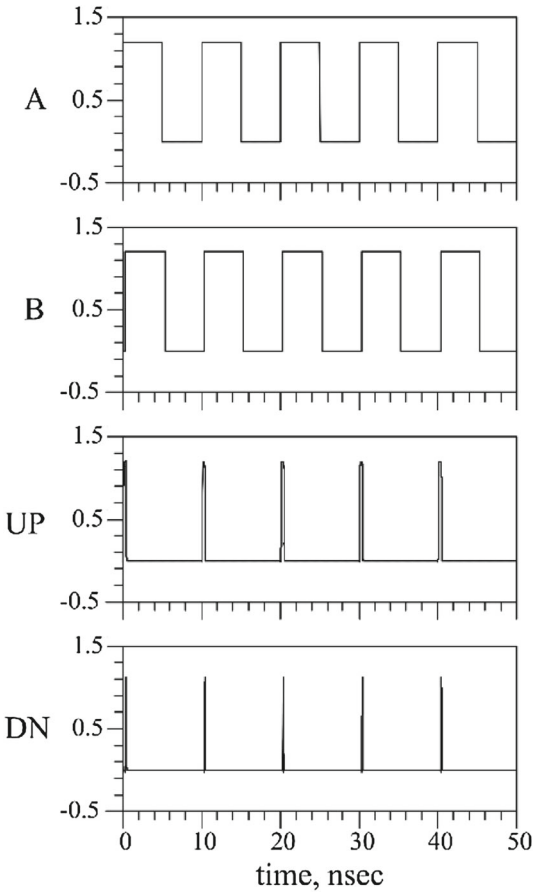


Fig. 11 Waveforms of proposed phase detector when A and B has phase differences about 300 ps

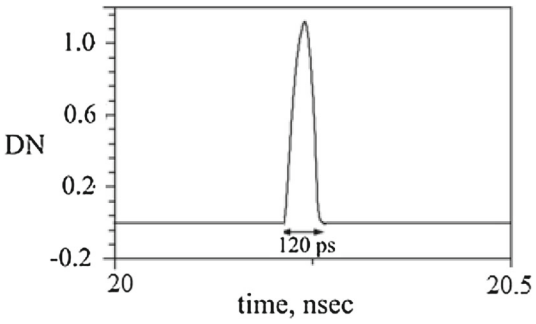


Fig. 12 Blind zone in the proposed phase detector

Fig. 9 shows the related waveforms of the proposed architecture at 100 MHz when B lags from A. As shown in this figure, the phase detector detects phase differences correctly in the positive edges of A and B. In this case, UP has pulse waveforms related to phase difference of A and B. DN signal falls rapidly from one to zero in the positive edges of B.

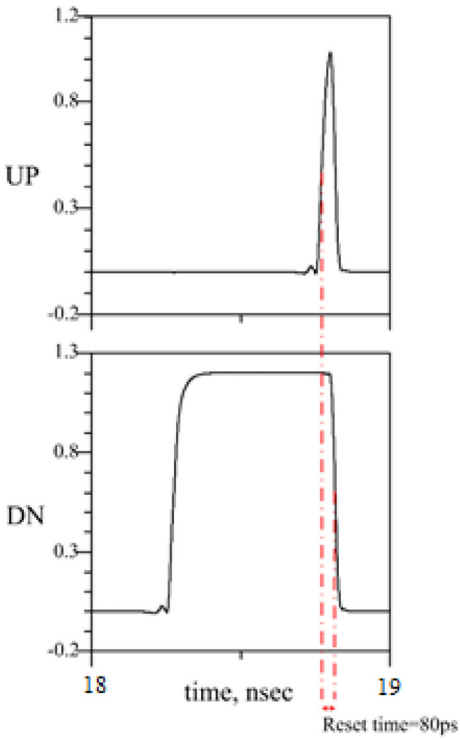


Fig. 13 Reset path time of proposed phase detector

The ability of phase detection for the proposed architecture can be defined by Equation [9].

According to (2):

$$-2\pi + 2\pi\frac{t_{\text{reset}}}{T_{\text{REF}}} < \text{PDR} < 2\pi - 2\pi\frac{t_{\text{reset}}}{T_{\text{REF}}} \tag{3}$$

where T_{REF} is the period of the reference signal, t_{reset} is the reset path delay and PDR is the phase detection range of PFD. Hence, for lower frequencies (when t_{reset} is much smaller than T_{REF}), the proposed phase detector has phase detection range which is very close to 4π since it has a very small reset path delay. For higher frequencies, (1) shows the phase detection range of proposed architecture which can be better in comparison with other similar works since it has lower reset path time. To prove this ability, the waveforms are shown when B lag from A for more than T/2 where T is the period of A and B. These waveforms are shown in Fig. 10. This figure shows that correct performance of the phase detector has the ability to detect large range of phase differences. It can be simply seen that when A lags from B for more than T/2, DN signal has pulses and UP signal falls rapidly from ONE to ZERO in positive edges of B.

To prove the ability of the circuit for detecting small phase offsets between A and B, simulation is done for 300 ps phase differences of A and B. The related waveforms

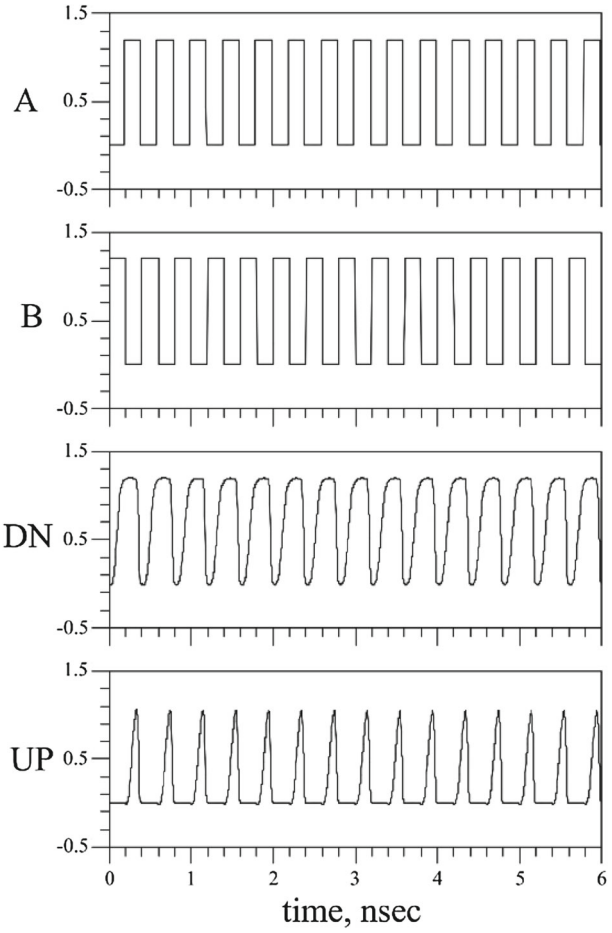


Fig. 14 Waveforms of proposed phase detector at 2.5 GHz

are shown in Fig. 11. These waveforms prove not only the proposed phase detector's ability to detect small phase offset but also its small reset path delay and high-speed operation. It should be mentioned that this circuit can also detect the phase differences as small as 80 ps.

As mentioned before, a blind zone is one of the most important parameters in designing phase detectors. To obtain this parameter, the width of DN signal when just UP signal should have a pulse is calculated. As shown in Fig. 12, the proposed circuit has a blind zone of about 120 ps.

To calculate the reset path time of the propose phase detector, the time at which both UP and DN signals are logical ONE should be calculated. Fig. 13 shows that the reset path time for the proposed circuit is about 80 ps. Is worth mentioning that it is assumed that when the signal is more than 50% of its value, logical ONE occurs and when the signal is less than 50% of its value, logical ZERO is happened. The

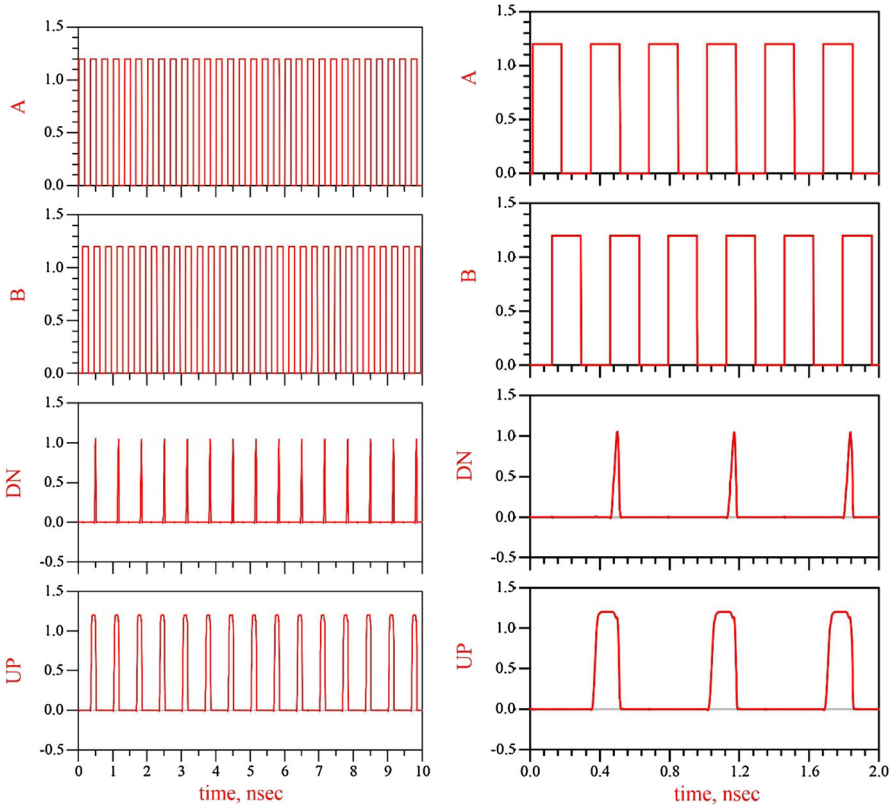


Fig. 15 Waveforms of proposed phase detector at 3 GHz

small value of reset path time can show the higher speed of the proposed architecture, and its ability in detecting small phase difference in comparison with similar works [8,12].

Simulations show that the proposed architecture has the ability to detect phase differences in high frequencies around 3 GHz. The waveforms for detecting phase differences at 2.5 GHz are shown in Fig. 14. In addition, waveforms for detecting phase differences at 3 GHz are shown in Fig. 15. Moreover, a simulation is done to show the ability of the proposed architecture to detect phase differences about 80 ps. The results are shown in Fig. 16 which proves that the proposed PFD can detect phase differences near 80 ps.

A comparison between the proposed circuit and similar works is listed in Table 1. This table shows that the proposed phase detector has a smaller reset path and blind zone, lower power consumption and higher frequency operation in comparison with the previous phase detectors. In addition, simulation over PVT is demonstrated in Table 2. This table shows that the proposed PFD has a good performance in corners.

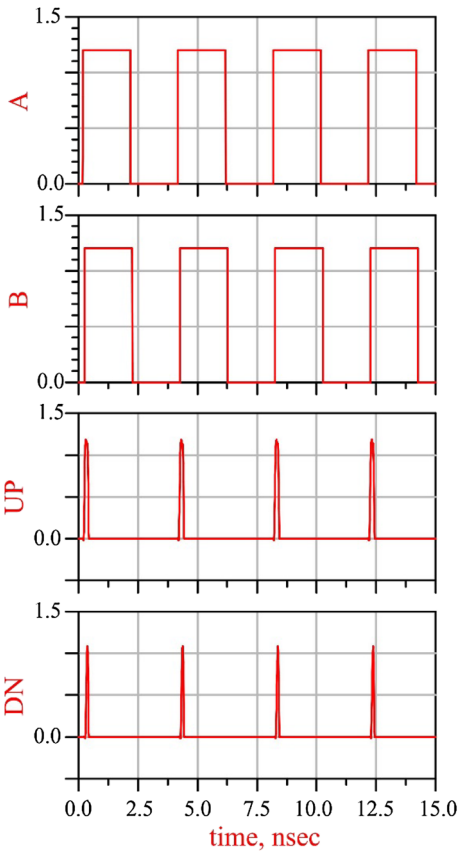


Fig. 16 Ability of proposed PFD to detect 80 ps phase difference

Table 1 Comparison with related works

Parameters	[8]	[12]	[3]	[11]	Conventional	This work[a]
Technology (nm)	800	180	130	90	130	130
Power supply (V)	5	1.8	1.2	1.2	1.2	1.2
Reset pulse time (ps)	162	165	156	NA	230	80
Blind zone time (ps)	221	156	61	0.75	280	120
Maximum operating frequency (GHz)	2.17	2.5	2.94	2.5	1.1	3
Ideal capture range	4π	4π	4π	4π	4π	4π
Power consumption @128MHz (μW)	325	296	496	NA	780	134

[a] Simulation

Table 2 Simulation results in important corners

Parameters	TT Corner @27 °C	FF Corner@−40 °C	SS Corner @80 °C
Reset pulse time (ps)	80	73	98
Blind zone time (ps)	120	110	143
Maximum operating frequency (GHz)	3	3.11	2.79
Power consumption @128MHz (μW)	134	121	165

5 Conclusions

A new phase detector is proposed in this paper. This phase detector has shown smaller reset path delay and blind zone in comparison with pervious phase detectors. In addition, the proposed circuit has lower power consumption and smaller chip area because of using fewer transistors. It can operate at high frequencies about 3 GHz. Hence, it can be used in high-speed DLLs and PLLs. The proposed phase detector is designed in TSMC 0.13μm CMOS technology.

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