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Memristor-Based Low-Power High-Speed Nonvolatile Hybrid Memory Array Design

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Abstract In this paper, a memristor–transistor hybrid architecture-based nonvolatile memory array design approach has been proposed. Here, a single memory cell consists of a memristor and one transmission gate, whereas a conventional SRAM cell consists of six transistors. This proposed design has the advantage of being nonvolatile, having high switching speed and low power requirement. The proposed cell shows better performance in comparison with other published memristor–transistor hybrid memory cell.

Keywords Memristor · Transmission gate · Nonvolatile · High speed · Low power

1 Introduction

As the demand for faster and denser memory devices grows up, memristor offers a promising alternative to conventional memory devices. Memristors are nano-devices that can store information for a comparatively long retention time, switch in nanoseconds, are super dense, and power efficient. This makes memristors poten-

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tial replacements for DRAM, SRAM, flash, and disk. Memristors have the power and speed of the DRAM cell and the potential lifetime of a hard disk. It not only can be treated as a universal nonvolatile memory, but also can perform in logical operations [10,14], programmable analog circuits [13,18] and in modeling and emulation of natural phenomena [5,12].

Initially theorized by Chua [3], the first physical realization of memristor was published in 2008 [20]. Since then, memristor crossbar arrays have been proposed [9] as the potential building block of an ultra-high density memory system. But while considering this kind of structure, the designers are mainly concerned with the sneak paths where the effective resistance of the array is lowered due to many alternated current paths and hence power consumption is high. Also reading errors are much likely to occur in this structure. Although passive crossbar structures with reading techniques alleviating the sneak path phenomenon to a very high extent have been reported [28], it involves very complex and time-consuming reading approach. "Self-gated" memristors with an inherent selector are also reported in the literature [1], but fabrication process of such self- gated memristor is complex and can alter the natural I–V response of the memristor in ON state. A potential solution of this problem is modified hybrid crossbar structure with access transistor gating. Although this will lower the density of the memristor memory system, it will greatly reduce read error problem and lessen power consumption as much control is put on the path of current flows. In the effort of making an efficient memristor–transistor hybrid memory cell, various models have been proposed [6,15,16]. However, designing such a hybrid cell with higher switching speed and lower energy requirement remains a challenge and is the key motivation of this research.

In this work, a memristor–transistor hybrid memory cell is proposed to reduce switching time and energy requirements. The performance of the cell is compared with other published works in terms of switching energy and speed and shows an overall better performance. With the inclusion of the cell into the memory array, a simple and fast data reading mechanism from the array has also been proposed. Simulation of a 64×64 memory array comprising of the proposed cell has been performed to validate the performance of the cell in a large memory array.

The following section describes the key factors playing crucial roles in designing such hybrid cell and the motivations behind the proposed cell design. Then, Sect. 3 puts a highlight on behavior and characteristic of the memristor used in the proposed cell, while in Sect. 4 the structure and working mechanism of the cell is described. Section 5 shows a simple demonstration of a memory array and presents simulation results. Section 6 puts a thorough comparison of the proposed cell against other published cells, and Sect. 7 concludes the whole work.

2 Design Considerations

In designing memristor–transistor hybrid memory cell two major components can be considered: (1) the memristor in which the data are stored and (2) the control circuit which connects the memristors with outside data lines. The control circuits provide well-designed timing signal to connect the memristor with data lines, control the

connection duration, and also ensure bidirectional current flow through the device to exploit its unique property of changing memristance with direction of current flow.

Among the hybrid cell structures, 1T1M (one transistor one memristor) [15] is the smallest memory cell with only two components in its design. However, it requires bidirectional input voltage with significant voltage drop. The 2A1M (two ambipolar transistors one memristor) [6] and 3T2M (three transistors two memristors) [16] cells use unidirectional input voltage with reference voltage at opposite end (inverted input voltage in 2A1M and VDD/4 in 3T2M). In the case of 2A1M, the inclusion of pass transistors and ambipolar transistors on each end causes significant voltage drop and larger area consumption. While, with VDD/4 as the reference voltage 3T1M model has less potential difference across memristor. However, reading mechanism is included in this cell itself with another memristor which is not always a very good idea because of the possibility of corrupting memristance while reading. Also larger area and significant voltage drop across pass transistor will lessen its appeal in cell design approach. Beating them all, 2TG1M (two transmission gates one memristor) [4] could be a smart modeling. To reduce voltage drop, it uses two transmission gates in a cell rather than pass transistors. However, its reading mechanism is not a very straight-forward one. Before read operation data lines are to be charged to VDD, also extra circuitry is required to convert the cell into READ mode. This will not only increase the operation time but also circuit complexity. Use of two transmission gates will result in larger area and cell capacitance hence additional power consumption.

So we suggest that apart from the characteristics of memristors, the circuital features that can be major attributes of a smartly designed hybrid cell are—(1)unidirectional input voltage, (2) less voltage drop across memristor to data line connecting component (preference of transmission gate over pass transistor), (3) small cell dimension, hence, not overloading the data lines with large amount of capacitance and (4) a relatively simple and fast operating circuital arrangement to convert the array from WRITE mode to READ mode. In this design approach, an attempt has been made to include these features.

3 Memristor: A Memory Element

In the physical model representation of memristor [2], it has been shown that the device can be characterized by an equivalent time dependent resistor. The resistance value at a particular time is linearly proportional to the quantity of charge that has been passed through it. Memristance switching mechanisms in many transition metal oxide-based memristors [7,17,21,23] have been widely studied, and it has been proposed that the drift/diffusion of oxygen vacancies [25] (or anions) driven by an electric field and/or thermochemical reduction/oxidation [26] plays a key role. The memristor is turned ON (resistance decreased) by channeling current through the memristor that displaces oxygen vacancies (major charge carrier) drifting them into bulk layer line-up to create a conducting channel. This conducting channel has resistivity that is lower than the bulk layer which will convert the high resistance bulk into low resistance. On the other hand, the memristor is turned OFF (resistance increased) by flowing current in the opposite direction. The movement of oxygen vacancies in the opposite

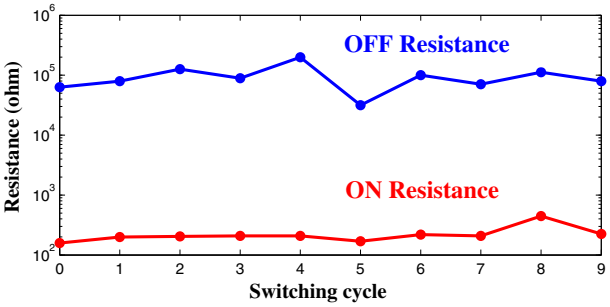

Fig. 1 Electrical performance of tantalum oxide-based memristors under <2 V pulses. Figure shows the reproducible resistance values for the first ten ON and OFF pulses with switching speed under 2 ns. ON and OFF resistance are almost 100 Ω and 100 KΩ, respectively, [11]

direction causes disruption in the conduction channel converting the bulk layer into a high-resistance substance again. Thus memristance can be switched between high and low values by using alternate current direction, hence alternate voltage direction. Significant progress has been achieved in tantalum oxide-based memristors device performance. Demonstration showed over 10^{10} open-loop switching cycles [24] in tantalum oxide-based devices, with the device remaining switchable after 15 billion cycles without any feedback or power-limiting circuits [24,27]. Also using a tantalum oxide system, this record was surpassed within a year to 10^{12} by Lee et al. [8]. In addition, switching in both directions in less than 2 ns has been demonstrated using a relatively low voltage (<2 V) [11], and the results are shown in Fig. 1.

In this work, while simulating the memristive behavior the model proposed by Yakopcic et al. [22] has been used. Instead of using a limited number of physically realizable parameter, it uses a parametric modeling approach for better fitting with memristor data. Also it incorporates a threshold voltage below which the memristor will behave like an ordinary resistor. In our work, the memristor model parameters have been adjusted to match the simulated electrical performance of the memristor with that of the previously published tantalum oxide-based memristor which has just been discussed above in this section [11]. Simulation result is shown in Fig. 2. Here a voltage pulse is applied across the memristor and its resistance alters from a low value to high value. The second pulse is applied (below the threshold level) just to measure the state resistance of the memristor which gives a high resistance value. With third pulse with reverse polarity the memristance decreases from a high value to low value. The fourth pulse below the threshold level is applied to measure the low state resistance value of the memristor.

4 Proposed 1TG1M Memory Cell

4.1 Cell Design

In the mathematical parametric modeling of memristor there is a threshold voltage below which the memristor will behave like an ordinary resistor [22]. This is required

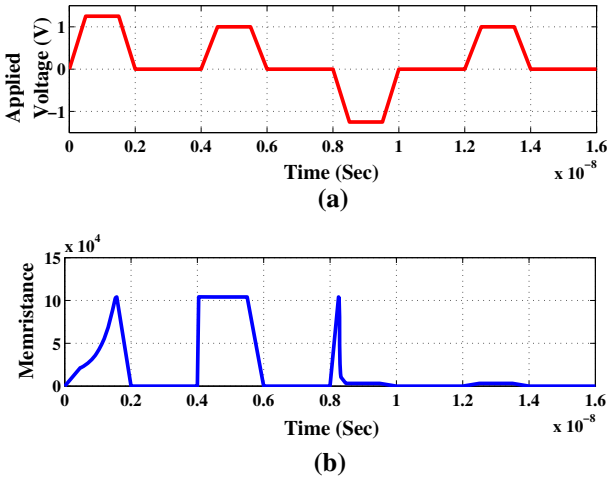

Fig. 2 Simulation result of a single memristor. **a** Applied voltage across the memristor, **b** corresponding measured memristance of the device. ON and OFF resistance is measured to be almost 3 KΩ and 100 KΩ, respectively

to provide a better fit to the characterization data and several of these devices show different threshold values. The memristor used in this work has a threshold voltage of 1.1 V [22], hence we need to apply a voltage greater than this to exploit the memristive behavior and the polarity of the applied voltage across memristor needs to be altered between logic 1 and 0 writing. Keeping these constraints into consideration we have designed the data voltage level for logic 1 and 0 as 2.4 and 0 V respectively, while the core cell is operated at a supply voltage VDD of 1.2 V. This voltage (VDD) will not only provide a reference voltage in WRITE mode causing bidirectional current flow through memristor but also provide reference voltage in READ mode without any circuital complexity involved.

The whole arrangement is shown in Fig. 3. There is a CMOS pass gate connected additionally with the basic cell. It is shown later in the memory array design that this pass gate is used to transfer the data value from bus line to desired column line and is not a part of the basic cell. The additional arrangement for reading data is also shown in the figure which consists of a resistance of 5 KΩ value in series with a NMOS transistor. Like the column connecting transistors, they are also not a part of the basic cell. Depending on the previously written data value, the memristance will be either high or low and that difference will be identified when this memristance is connected in series with a resistance and KVL is applied along that branch. In this design, memristance was high (around 100 KΩ) in writing logical 1 and low (around 3.4 KΩ) in writing logical 0. Vref was set to 2.4 V. The whole reading operation was done with a 1-ns pulse and during that period voltage across memristor device was kept below the threshold level. This threshold value comes as a sheer approximation in the modeling just to match the characterization data, and there is always a finite probability to alter the memristance during read operation. So it is preferred to keep that read pulse width as narrow as possible. A refreshing pulse can be added to prevent the data corruption.

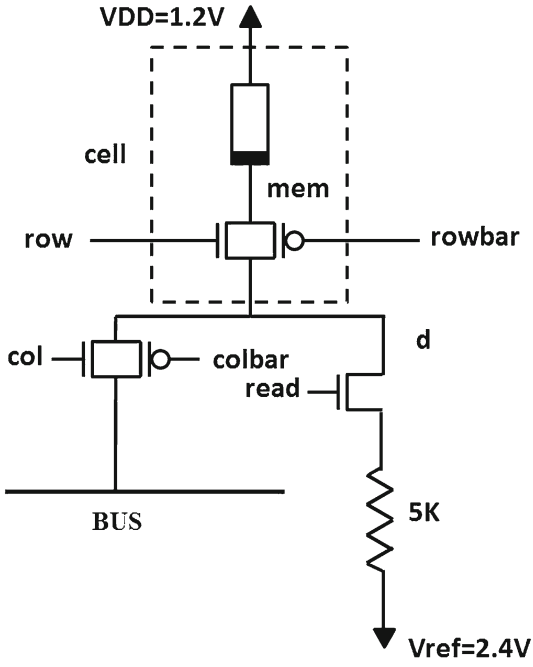

Fig. 3 Proposed memory cell consisting of memristor and MOS devices

4.2 Write and Read Operation

The writing and reading mechanism in the proposed cell is discussed below. However, this is an illustration of reading and writing into a single cell contained within an array structure.

Writing '1': As mentioned earlier, Vref is set to 2.4 V. In writing process, the node 'col' is pulled to high and node 'colbar' to low. This will transfer data (logical 1 as 2.4 V) from BUS line to desired column. At the same time, node 'row' at high (node 'rowbar' at low) causes current flow from that column into the VDD node through the desired cell with indicated memristive polarity. This will pull its memristance to high value.

Writing '0': Same operation is carried over as that was for writing 1 except the direction of current flow through the cell is reversed in this case. The node 'col' is pulled to high and node 'colbar' to low. This will transfer data (logical 0 as 0V) from BUS line to desired column. At the same time, node 'row' at high (node 'rowbar' at low) causes current flow from the VDD node to the desired column (opposite to the case of writing 1) through the desired cell pushing its memristance to low value.

Read Operation: During read operation node 'row' at high, node 'rowbar' at low, and node 'read' at high connect the desired cell with the reading resistor. The read value at node 'd' is then brought back to the BUS line through specific column gate.

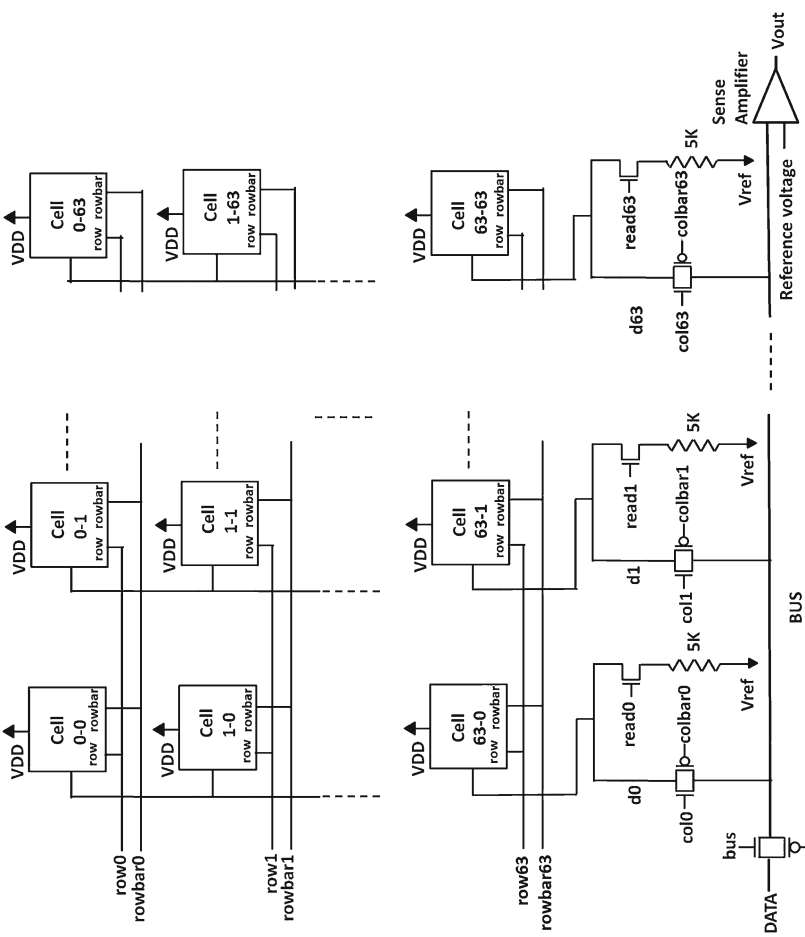

Fig. 4 Proposed memory array structure consisting of memristors, MOS devices, read resistance, and sense amplifier

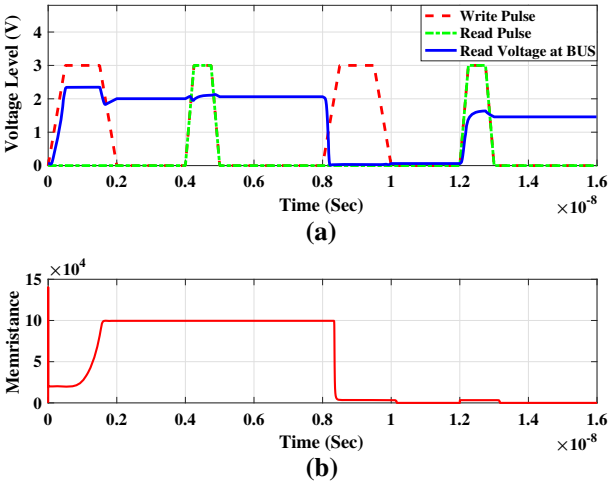

Fig. 5 Writing and reading operations in a single cell of the proposed memory array. **a** Voltage levels of the write pulse (*in red line*), read pulse (*in green line*) and read voltage level at BUS line (*in blue line*). First '1' is written in the cell and read back. In the next pulses, '0' is written in the cell and read back. **b** Memristance in the cell with the mentioned operations (Color figure online)

5 Array Structure with the Proposed Cell

In Fig. 4, a 64 × 64 memory array is illustrated using the proposed cell. The detail working mechanism (both read and write) for the cells in this memory array system has already been discussed in Sect. 4. The proposed system is mainly a one-bit bus system. With the conjugation of proper column and row signaling served by encoder, particular bit can be written into a desired cell.

5.1 Simulation Result

The whole simulation work was carried out using LTspice software. TSMC 180 nm process was used.The NMOS and PMOS transistors in the CMOS pass gate of the cells have width of 2 and 4 μm, respectively, whereas those in the Column Select CMOS pass gates have width of 8 and 16 μm. The size feature of the transistor plays important role in the behavior of the cell. However, focusing on designing an efficient memory cell optimum feature size of the transistors has been chosen. The PMOS width is kept twice of NMOS to ensure equal rise and fall time. Parasitic connecting wire resistances have also been taken into account in the simulation.

In Fig. 5, simulation result for writing and reading into a single cell in the array structure has been shown. Memristance and output voltage at BUS line (before sense amplification) from that particular cell is shown in the figure. First a single cell (cell at first row at first column) in the array structure has been picked up for test operation. '1' is written into the cell (with pulse at 0 ns). Value is read afterward (pulse at 4 ns). The whole operation is repeated for '0' (writing with pulse at 8 ns

Table 1 Characteristic value of the proposed cell in the array

Write pulse	2 ns
Read pulse	1 ns
Memristor resistance after writing '1'	100 KΩ
Memristor resistance after writing '0'	3.4 KΩ
Voltage level while reading '1' (before sense amplification)	2.11 V
Voltage level while reading '0' (before sense amplification)	1.61 V
Noise margin	0.5 V
Energy while writing '1'	1.16801 pJ
Energy while writing '0'	1.3060823 pJ
Energy while reading '1'	0.7020868 pJ
Energy while reading '0'	5.782348 pJ

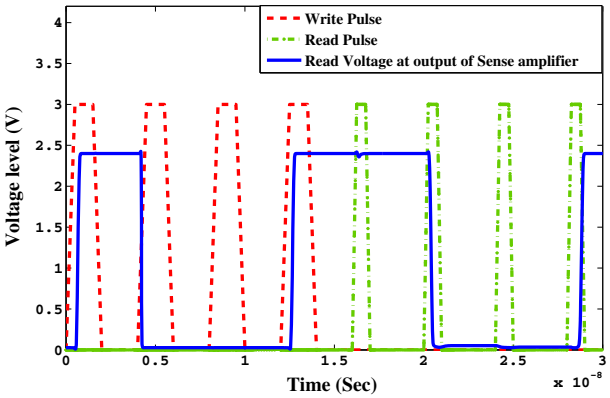

Fig. 6 Writing and reading in multiple cells of the proposed memory array. Voltage levels of write pulse (*in red line*), read pulse (*in green line*) and voltage at the output of the sense amplifier (*in blue line*) are shown. Here, consecutively '1,' '0,' '0,' and '1' are written in four different cells of the memory array and then read back. Additional delay introduced due to sense amplifier operation. Timing operations are listed in Table 2 (Color figure online)

and reading at 12 ns). Characteristic values of the cell in the array are shown in Table 1.

However, in this design case the read voltage for logical 1 and 0 roams around approximately 2.11 and 1.61 V respectively, (mentioned in Table 1). So, a sense amplifier as a peripheral circuit has been connected to the BUS line. This will trigger these read voltage values to the data voltage level with some additional delay introduced. Write and read operations were performed over several cells on the array system. In this case, randomly four different cells were selected and tested for writing and reading operations. '1' or '0' was written in the selected cells and read back. Read voltages are taken at sense amplifier output. Simulation results are shown in Fig. 6, and timing operations are listed in Table 2.

Table 2 Timing and operations performed in the array system

Timing (ns)	Operation
0–2	Writing '1' into cell at 1st column 1st row
4–6	Writing '0' into cell at 2nd column 1st row
8–10	Writing '0' into cell at 1st column 2nd row
12–14	Writing '1' into cell at 2nd column 2nd row
16–17	Reading from cell at 1st column 1st row
20–21	Reading from cell at 2nd column 1st row
24–25	Reading from cell at 1st column 2nd row
28–29	Reading from cell at 2nd column 2nd row

6 Switching Speed and Energy Requirements

For required energy in such a hybrid cell, two factors will play crucial roles. The first one is the characteristic of the memristor (the ON and OFF memristance and switching interval between these two states). Another factor is the circuital arrangement within the cell. However, the first factor will vary with material composition, processing and fabrication technology. So we will conduct our comparison with other models just on the basis of circuital arrangement. In doing so, it can be shown that this proposed model requires less energy than 1T1M [15], 2A1M [6] and 3T2M [16] model. In the proposed model, transmission gate allows a complete pull-up or pull-down of input voltage where there is a significant voltage drop across pass transistors in other models mentioned above. And, because of inclusion of one transmission gate instead of two, this cell consumes less energy than 2TG1M [4] too. Another important comparison factor is switching time (time for a memristor to completely switch logic state). Switching time also contributes to the energy consumption factor as small switching time means less energy is being consumed and the switching speed is proportional to the effective magnitude of potential difference across memristor. As the proposed model allows almost a complete pull-up or pull-down of input voltage, it shows relatively fast switching speed and less energy requirement. Here, power consumption is monitored from the moment a particular cell is selected for writing until the memristor completely switches its state. While writing 1 or 0 into the proposed cell, power consumption by the cell components along with leakage currents through other cells and column select gates' power consumption are taken into account. A comparison of our proposed cell with other published cells and SRAM in terms of energy and switching time is shown in Table 3.

Here, it can be emphasized again on the fact that energy consumption is largely dependent on the characteristics of the memristor itself. In the proposed design, the ON, OFF memristance and switching speed of the used memristive device are 3.4, 100 KΩ, and 2 ns respectively. With larger OFF resistance and smaller switching time, our proposed cell (and other models too) will require lesser energy requirement than shown. So the comparison table may not tell us the whole story. But in terms of energy requirement and switching speed the proposed model will show superior performance

Table 3 A comparison between the proposed cell and other published cells and SRAM

Memory cell	Energy in writing '1'	Energy in writing '0'	Switching time for '1'	Switching time for '0'
1TG1M (proposed here)	1.16801 PJ	1.3060823 PJ	2.00 ns	2.00 ns
1T1M [15]	1.67 PJ	350.6 PJ	27.22 ns	18.86 ns
2A1M [6]	2.83 PJ	1.23 PJ	56.00 ns	47.13 ns
3T2M [16]	1.82 PJ	0.67 PJ	102.12 ns	44.17 ns
2TG1M [4]	1.66 PJ	1.66 PJ	12.14 ns	14.67 ns
6T SRAM (180 nm Tech)[19]	24.625 PJ	24.625 PJ	0.85 ns	0.85 ns

over other models. Here one end of memristor is kept at fixed potential and voltage drop occurs only across the transmission gate.

7 Conclusion

In this work, an efficient memristor–transistor hybrid memory cell design has been proposed which requires one memristor and one transmission gate. A recently demonstrated tantalum oxide-based memristor [11] has been incorporated in the design in simulating which a parametric-based simulation model [22] has been used. The performance of the memory cell has been verified by putting it into a 64×64 memory array. The proposed cell not only shows better performance than other similar published cells [4,6,15,16] in terms of energy requirement and switching speed but also offers a relatively simple and fast operating WRITE mode to READ mode conversion technique in the array system. As a general case, memristor with higher OFF resistance and smaller switching period will push this writing delay and power consumption further lower. This design may not be generalized for every type of memristor to show such high performance but with memristor having high OFF resistance, high threshold voltage capability, fast switching time and with the proposed cell design approach, the memory cell can show superior performance. However, as mentioned earlier, in such hybrid cell the size of transistor becomes crucial in the end. This is compensated by the lower power consumption and less read error probability than the 'only memristor' comprising crossbar. High supply voltage (2.4 V) and three level of supply voltage (0, 1.2, and 2.4 V) also can be considered as some negative attributes of the proposed design. However, in the arena of memristor–transistor hybrid memory cell design technique this proposed cell can offer a better performance.

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