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Alternative Realizations of CMOS Current Feedback Amplifiers for Low Voltage Applications

BRENT J. MAUNDY,[1]* IVARS G. FINVERS[1] AND PETER ARONHIME[2]

[1] *Department of Electrical and Computer Engineering, University of Calgary, 2500 University Drive NW, Calgary, Alberta, Canada T2N 1N4*
[2] *Electrical Engineering Department, University of Louisville, Louisville, KY 40292, USA*
E-mail: maundy@enel.ucalgary.ca

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Abstract. Two variants of a new current feedback amplifier (CFA) are presented in this paper. These CFAs are realized in CMOS technology and both are capable of working at low voltages. It is shown that one circuit performs better than the other by virtue of an increased impedance at its Z terminal achieved through the use of additional transistors. Analysis of both variants of the current conveyor and buffer that form the current feedback amplifier gives an insight into the location of primary poles and zeros of the CFAs. Simulation results indicate an overall gain bandwidth product in excess of 59 MHz and 102 MHz for each circuit at a gain of -10 and with a 3.3 V supply. Experimental results from a chip fabricated in a 0.35 μm CMOS technology agree closely with the simulation results.

Key Words: Current feedback amplifiers, Low-voltage CMOS

1. Introduction

Current feedback amplifiers (CFA) are noted for their potential for high bandwidth, high slew rate, and a closed-loop bandwidth which is almost independent of the closed loop gain [1,2]. Bipolar implementations are popular due to their high speed and the ease with which the low impedance current sensing node can be implemented [3,4]. The lower transconductance of MOS transistors typically makes CMOS current feedback amplifiers inferior to bipolar implementations. A CMOS CFA is, however, desirable for mixed-signal IC applications. In such applications, the choice of IC technology is dictated not by the needs of the analog signal processing circuitry but by that of the digital circuitry. Also because CMOS CFAs are typically composed of a CMOS current conveyor [5,6] followed by a buffer stage, a low-voltage CMOS current conveyor would enable CFA based circuits to be implemented in submicron CMOS IC technologies with reduced supply voltages. Examples of low voltage CMOS current conveyors that could be used to build low voltage CFAs are given in [7–10], where novel low voltage techniques are employed. A high drive CFA was reported by [11]. But with several devices stacked between its rails, operation at low voltages may become an issue.

In this paper we report on two CMOS implementations that are suitable for low supply voltage applications. The basic topology is built around a modification of the work in [9] which in turn was inspired by the work of [10]. In the first of these two implementations, referred to as circuit 1 in this paper, only two devices are stacked between the supply rails. Its design is therefore greatly simplified, and its only drawback is its low output impedance at the Z node which will affect its performance at high gains. In a second implementation, referred to as circuit 2, low voltage high-swing current mirrors are employed in a unique configuration. The high swing, low voltage current mirror offers the advantage of improved Z terminal impedance while allowing low supply operation. In both circuits, the Z terminal circuit is formed by copying the output of the amplifier used to form the buffer. Like a conventional CFA, the current feedback occurs externally through a feedback

*Address correspondence to: Dr. Brent J. Maundy, P. Eng., The University of Calgary, Department of Electrical & Computer Engineering, 2500 University Drive N.W., Calgary, Alberta, Canada T2N 1N4. Tel.: (403) 220-6177, Fax: (403) 282-6855. http://www.enel.ucalgary.ca/People/Maundy/Maundy.html

resistor. The CFA property of constant-bandwidth relatively independent of closed loop gain is maintained in both these designs.

2. Circuit Description

A. *Circuit 1*

Consider the CFA circuit shown in Fig. 1 that consists of a novel second generation current conveyor (CCII+) followed by a unity gain buffer. The current conveyor portion of the CFA differs from the design suggested in [9] by not relying on a bias current and contains only one compensation capacitor. The lack of a bias current allows the input to swing to the threshold voltages of the input transistors since $V_{ds,\min}$ of the bias current were absent. Its only drawback is that its CMRR is lower than if the bias current is present. The CCII+ is identical to the unity gain buffer stage with the exception of the extra pair of transistors M7 and M8. Transistors M1 through M4 form the differential input stage of the amplifier. The node labeled a acts a high impedance node whose gain $g_1 r_{o1}$ depends on the product of the transconductance of M1/M3 and the output impedance seen at node a. Here g_1 represents the transconductance of M1 and M3 and r_{o1} is the reciprocal of the total conductance seen at node a. Henceforth the output resistance of a gain stage is represented by the r_o terms. Transistors M5 and M6 provide additional gain by acting as an inverting amplifier whose gain A_v is $-g_2 r_{o2}$ where $g_2 = g_{m5} + g_{m6}$. The inverting amplifier high frequency performance characteristics are well known, but capacitor C_{c1} (and C_{c2}) are still required for high frequency compensation as shown in [12]. To understand the voltage following action of this circuit, assume that the voltage at the Y node rises and no current is injected into the X node, i.e., $i_x = 0$. At node a the voltage falls immediately on account of the high gain and inversion between nodes Y and a. At node X the voltage rises due to the inversion with node a. This serves to push more current into node a negating the gain action caused by transistor M3. Consequently, V_x follows V_y faithfully. It can be easily shown that the DC gain of this circuit is given by

$$\frac{V_X}{V_Y} = \frac{g_1 g_2 r_{o1} r_{o2}}{1 + g_1 g_2 r_{o1} r_{o2}} \cong 1 \tag{1}$$

if $g_1 g_2 r_{o1} r_{o2} \gg 1$. Copying the currents in transistors M5 and M6 using identical transistors M7 and M8 generates the current i_z in the presence of an input current i_x with $i_z \cong i_x$ if $g_3 = g_2$. The current following action of the current conveyor formed in this manner has been well documented and explained in [2] and [12]. Note that i_z is not an exact copy of i_x because some current is lost to the buffer's output impedance. It is therefore important that r_{o2} be as large as possible. One means of accomplishing this goal is to use large length transistors at the expense of a reduction of the amplifier's bandwidth. A small signal model of the current conveyor portion of Fig. 1 reproduced from [12] for convenience is shown in Fig. 3. To employ this model, which serves for both circuits 1 and 2, the plus (+) sign must be used with the dependent current sources to represent circuit 1. To model circuit 2 the minus (−) sign is used as explained later on. The small signal model of the buffer is not shown because it is identical to the buffer section of the CCII. Additionally, C_{1-3} represent the total parasitic capacitances at the high impedance nodes. Note the negative feedback action forces the input resistance at the X node to be as small as possible, and the poles of the X terminal impedance are the same as those of the buffer formed from the amplifier.

B. *Circuit 2*

Not mentioned in the previous section is the fact that by using large transistor lengths the maximum open loop gain of the amplifiers formed by transistors M1–M6 and M9–M12 is limited to about 70 dB. This is primarily due to the output impedances r_{o1} and r_{o2} which will typically be less than 100 KΩ. One way of improving the open loop gain of the amplifier and increasing the output impedance at the Z terminal is to use improved current mirrors that provide high impedance nodes. Such a circuit is shown in Fig. 2(a). Here the input stages M1–M4 and M9–M11 remain the same as in Fig. 1, but the gain forming second stage is built around a non-inverting amplifier that uses the wide-swing cascode mirror. A simplified version of the operational amplifier that is used to implement Fig. 2(a) is shown in Fig. 2(b) for comparison purposes. The operation of the wide-swing cascode mirror is well documented and is increasingly becoming popular in many analog low voltage designs [13]. To ensure maximum input dynamic range, complementary transistors M5a–M6b and M13a–M14b are used at the input of the second stage gain in Fig. 2(a). The remaining transistors M5c–M7b, M6c–M8b, M13c–M13f, and M14c–M14f form

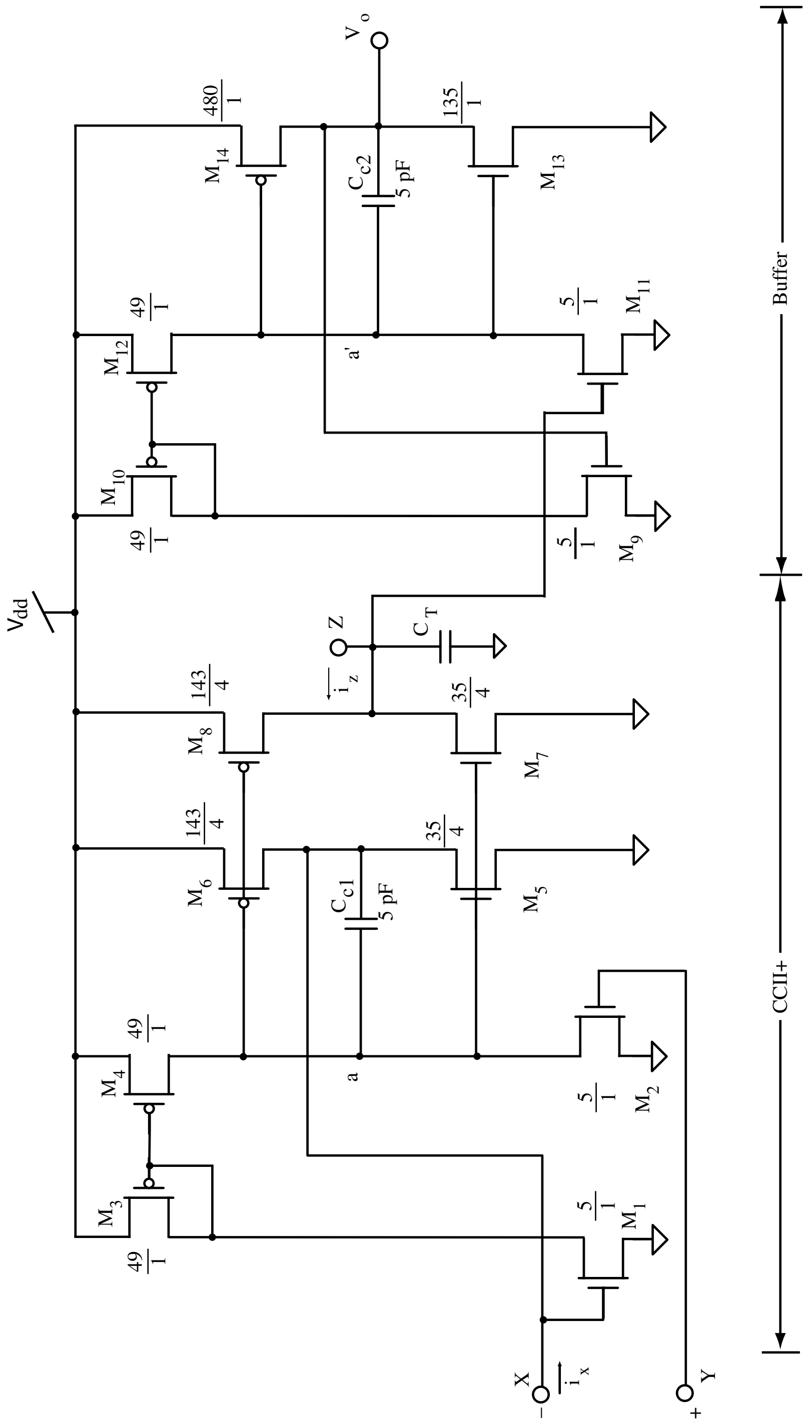


Fig. 1. Circuit diagram (Circuit 1) of the proposed CMOS CFA.

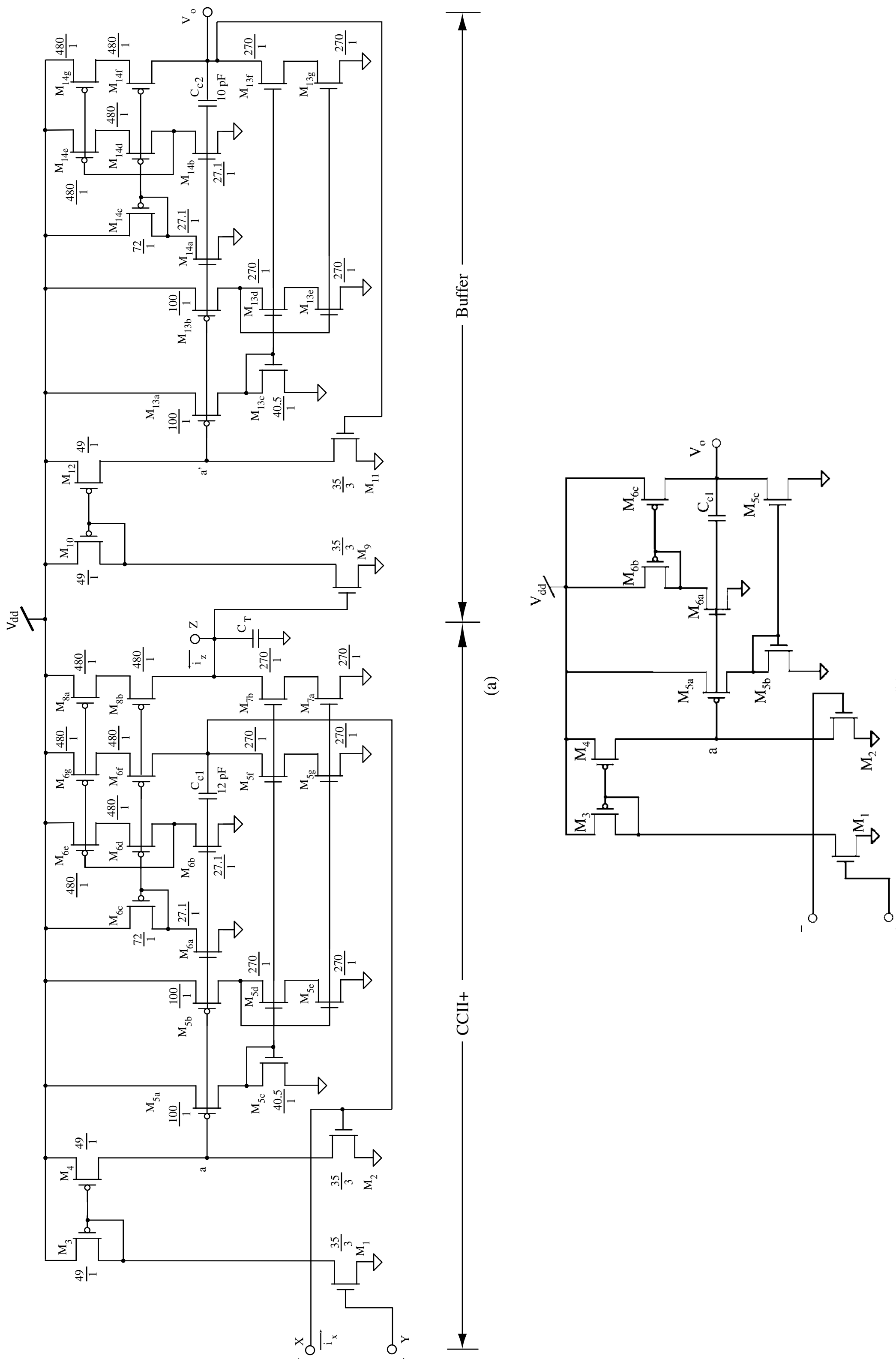


Fig. 2. (a) Circuit 2, an improved implementation of circuit 1. (b) A simplified version of the operational amplifier used in circuit 2.

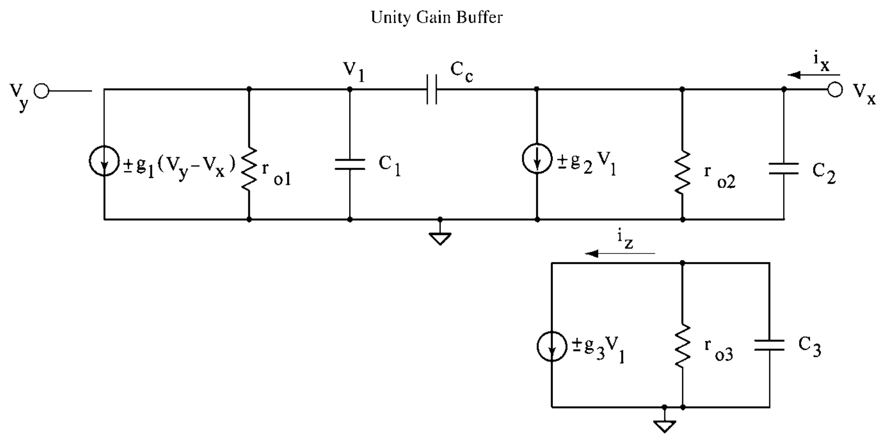


Fig. 3. AC model used for circuits 1 and 2. The (+) sign applies when considering circuit 1 and the (−) sign when considering circuit 2.

the high-swing cascode mirrors. Note, that in circuit 2 the gates of transistors M2 and M11 form the voltage following nodes as opposed to transistors M1 and M9 of circuit 1. This is due solely to the fact that the second stage gain is non-inverting in circuit 2 while it is inverting in circuit 1. This is reflected also in the small signal model shown in Fig. 3 by using the minus sign (−) on the dependent current sources. Otherwise the ac models are identical in form. Like the first circuit, Figs. 2(a) and 2(b) require compensation capacitors. However, because the output impedance of the circuit of Fig. 2(a) is greater than that of Fig. 1, its gain and high frequency performance can be expected to be improved over circuit 1 with proper compensation.

3. Circuit Observations

Table 1 summarizes the important parameters for both circuits such as pole/zero frequencies and input

Table 1. A summary of the important parameters of the CFA.

Characterisitic	Governing Equation		CFA Component
Dominant poles	$s_{p_1}^{V_x/V_y} = s_{p_1}^{r_{in,x}} \cong -\frac{g_1}{C_c\left(1-\frac{g_1}{g_2}\right)}$	Buffer parameters	CCII parameters
	$s_{p_2}^{V_x/V_y} = s_{p_2}^{r_{in,x}} \cong -\frac{(g_2-g_1)}{C_1\left(1+\frac{C_2}{C_1}+\frac{C_2}{C_c}\right)}$		
Input resistance (Low frequencies)	$r_{in,x} \cong \frac{1}{g_2}\frac{1}{g_1 r_{o1}}$		
Dominant zeros	$s_z^{r_{in,x}} \cong -\frac{1}{(C_1+C_2)\,r_{o1}}$		
	$s_{z_1}^{i_z/i_x} \cong -\frac{g_1}{C_c}$		
	$s_{z_2}^{i_z/v_y} \cong -\frac{1}{r_{o2}C_c}$		
Output current (Low frequencies)	$i_z = \frac{g_3}{g_2}\left(i_x - \frac{v_y}{r_{o2}}\right)$		

resistance. Other high frequency poles exist in the circuits particularly in circuit 2, but these will not discussed here. Table 1 also shows that for unity gain stability $g_2 > g_1$ and $C_{c1,2} > C_{1,2}$. Also from Table 1, it follows for both amplifiers that if the second stage tranconductance is high and the first stage gain is high, $r_{in,x}$ will be low. A further comparison between circuits 1 and 2 yields the observation that the down side of circuit 1 is the fact that g_2 and r_{o2} and hence the bandwidth are dependent on the power supply voltage. A stable power supply would therefore be a necessity to ensure that r_{in} and hence the bandwidth of circuit 1 does not vary with supply voltage. In fact it can be easily shown that g_2 is proportional to V_{dd} and the quiescent current that flows through M5–M6, M7–M8, M11–M12, and M13–M14 is proportional to V_{dd}^2. This in turn makes the power dissipation in these transistors proportional to V_{dd}^3 which can be undesirable especially for battery-powered operation. Using larger devices at the expense of a reduction in bandwidth can reduce the power dissipation. Circuit 2 is less prone to supply variations in g_2 because of the decoupling between the g_m generating transistors and the output stage via the wide-swing cascode mirrors.

On the subject of power supply regulation and biasing several options exist to improve the power supply rejection [14]. One option proposed is to use a regulated follower amplifier that supplies the inverter chains with power. However, the amplifier must be supplied with a higher voltage than V_{dd} which can present a problem. Another option is to use AC coupling in the inverters through high valued resistances and capacitances, but the improvement is only marginal compared to no bias control. The last option borrowed from AC coupling, is to use the auto-zeroing property of dynamic bias to replace the RC coupling [15]. While offering the best solution the high frequency clock noise will be present in the output and can be minimized, but never completely eliminated.

Finally, it is instructive to get a feel for the useful power supply range of circuits 1 and 2. Using circuit 1 because of its simplicity and examining the inverters formed from M5–M6, M7–M8, M11–M12, and M13–M14 the equivalent input voltage V_{eq} that maximizes g_2 and hence the gain of the inverters is given by

$$V_{eq} = \frac{V_{dd} - |V_{Tp}| + V_{Tn}\sqrt{\frac{\beta_n}{\beta_p}}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} \tag{2}$$

where the symbols V_{Tn} and V_{Tp} have their usual meaning and β is the MOS transistor gain that is dependent on process parameters and the device geometry. Thus as V_{dd} is reduced the input voltage required for maximum gain at node a is reduced for fixed aspect ratios according to (2). To ensure that M2 (or M11) remains in saturation requires that $V_Y - V_{Tn} \leq V_{eq}$. Since V_Y is typically set at 50% of the supply voltage then it follows that V_{dd} should be less than two times the sum of V_{eq} and a threshold voltage to avoid the edge of the triode region for M2 (or M11). This is easily accomplished by choosing the inverter aspect ratios such that V_{eq} is equal to $V_{dd}/2$ and hence $V_{X,Z} = V_{eq}$. Note intuitively at the same time V_{eq} (and V_X) cannot be less than one V_{Tn} for obvious reasons. Hence it follows that V_{dd} should be greater than $2V_{Tn} + |V_{Tp}|$ because the p-transistor in the inverter chain should be considered. In a typical CMOS process such as the one this circuit was implemented in with $V_{Tn} = 0.57$ V and $|V_{Tp}| = 0.7$ V this implies $V_{dd,\min} \cong 1.8$ V. For maximum input dynamic range around $V_{dd}/2$ however, this lower limit changes to $3V_{Tn} + |V_{Tp}|$ because the transistors in the inverter remain in saturation when $V_{eq} - V_{Tn} < V_{X,Z} < V_{eq} + |V_{Tp}|$. For circuit 2 the minimum supply voltage is dictated by $V_{ds,\min}$ required to maintain the output transistors in saturation.

4. Simulation and Experimental Results

To utilize the circuits of Figs. 1 or 2 as an inverting voltage amplifier they must be used in the configuration shown in Fig. 4. Here we assume that the internal node Z has a capacitor C_T connected to it. Its

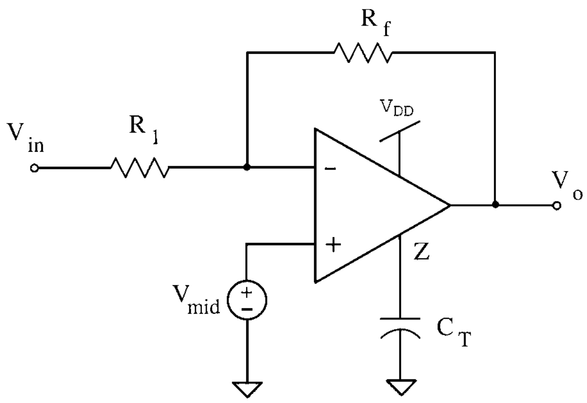
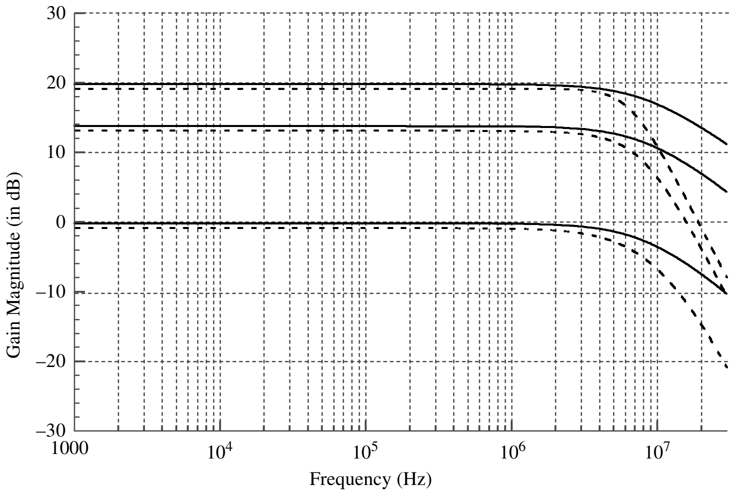


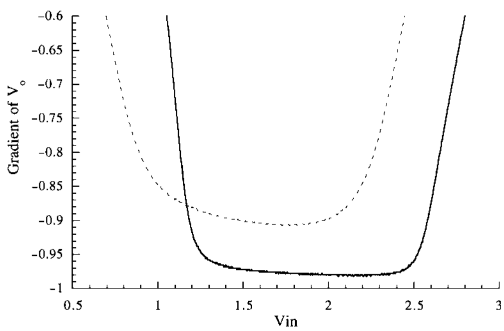
Fig. 4. Circuit diagram of the proposed CMOS current feedback amplifier.

function is to set the open loop transresistance pole frequency $\omega_p \cong 1/r_{o2}C_T$ and hence the bandwidth of the amplifier. Note that the bandwidth of the buffers employed in the amplifier must be greater than ω_p. This is easily achievable by adjusting C_T and $C_{c1,2}$ appropriately. The input signal V_{in} is applied through resistor R_1, and a feedback resistor R_f is connected between the output and the inverting terminal in classic fashion. The non-inverting terminal of the op-amp is assumed to be held at midsupply V_{mid}.

To confirm circuit operation, HSPICE simulations were performed on the circuits of Figs. 1 and 2 using 0.35 μm CMOS Level-28 model parameters. The supply voltage was set at 3.3 V. The aspect ratios used in circuits 1 and 2 are shown in Figs. 1 and 2(a), respectively. The output stage of each circuit was designed to drive a load of 5 pF. The feedback resistor R_f was set at 5 kΩ and the input resistor R_1 varied with values of 0.5 kΩ, 1 kΩ, and 5 kΩ. Capacitance C_T was set at 5 pF and 2.1 pF for circuits 1 and 2, respectively to satisfy bandwidths of 6.5 MHz and 10.5 MHz, respectively at a gain of -10. Figure 5 shows that the closed loop bandwidth remains approximately constant as the gain is varied from -1 to -10. The unity gain bandwidth of the buffer in circuit 1 was 16 MHz whereas it was 24 MHz for circuit 2. Also the open loop gain of the buffer in circuit 1 was 70 dB whereas it was 90 dB for circuit 2. Note that circuits 1 and 2 provide an overall gain bandwidth product in excess of 59 and 102 MHz, respectively at a desired gain of 10. Circuit 2 achieves a higher gain-bandwidth product due to the increased output impedance. The distinction between

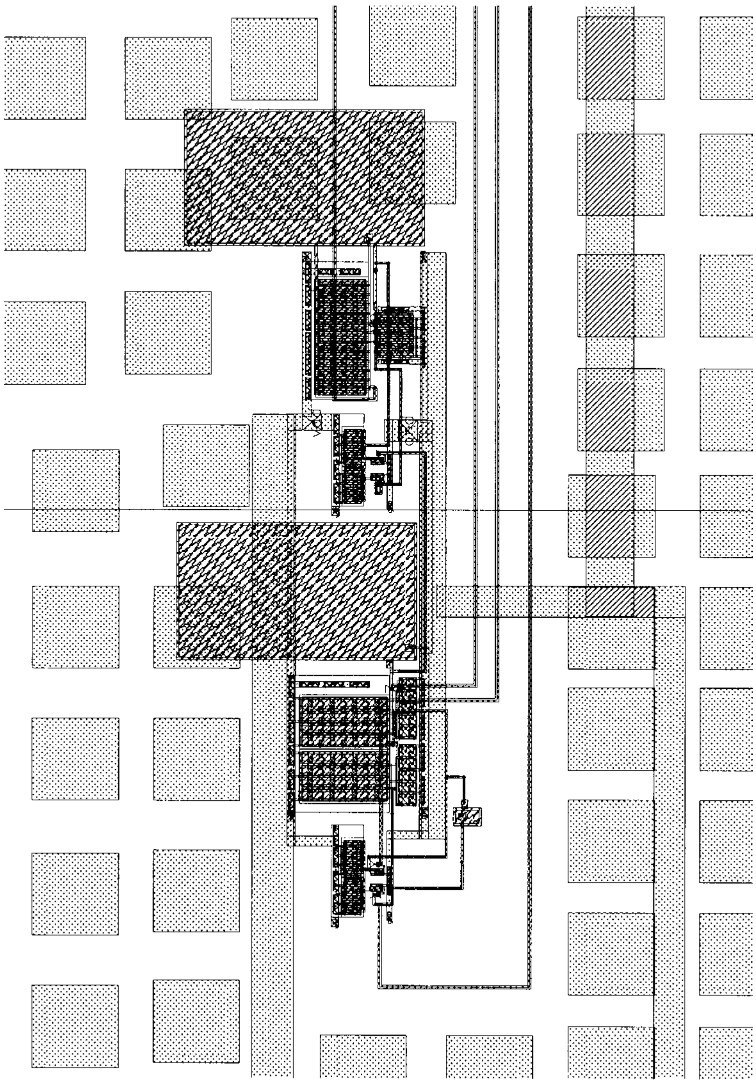


(a)

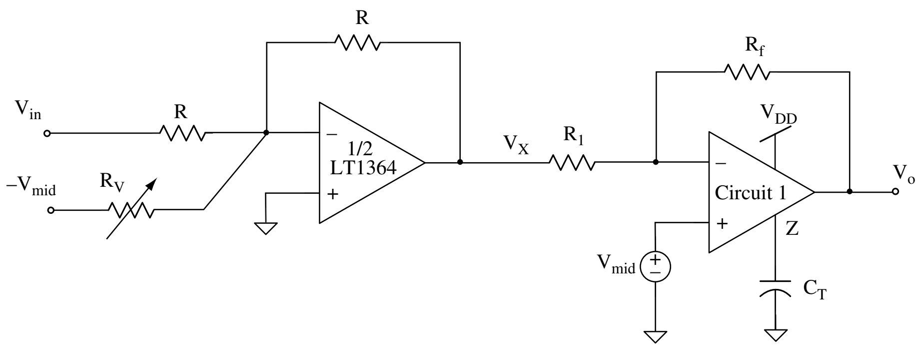


(b)

Fig. 5. (a) HSPICE simulation results for the frequency response of circuits 1 and 2 with $R_f = 5$ kΩ and R_1 varying from 0.5 kΩ to 5 kΩ. The solid line represents circuit 2 while the dashed line represents circuit 1. (b) DC simulation of the gradient of the output with a gain of -1 to illustrate the input voltage range.



(a)



(b)

Fig. 6. (a) IC layout (350 μm × 118 μm) of circuit 1. (b) Test setup for circuit 1.

Table 2. Selected extracted parameters for circuits 1 and 2.

Parameter	Circuit 1	Circuit 2
$r_{in,x}$ (Low frequencies)	15.11 Ω	4.87 Ω
r_z	47.9 kΩ	126.4 kΩ
Output resistance of the CFA R_o	<0.2 Ω	<0.2 Ω
Power consumption	2.2 mW@1.8 V 45 mW@3.3 V	4.7 mW@1.8 V 93 mW@3.3 V
$C_X = C_2$ (Parasistic capacitance)	0.24 pF	1.40 pF
$C_Z = C_3$ (Parasitic capacitance)	0.24 pF	1.42 pF

the two circuits can clearly be seen as the desired gain increases and the error increases. If C_T is decreased any further for circuit 1, it exhibits peaking at high frequencies as pointed out in [3]. But not shown in Fig. 5(a). A dc sweep of the input was also examined for both circuits at a gain of -1, and the gradient of the output is shown in Fig. 5(b). The input voltage range is clearly visible for both circuits. In transient simulations at a frequency of 1 MHz, the output offset voltages were recorded at 45 mV and 5.6 mV for circuits 1 and 2, respectively. Additionally, Table 2 shows the results for the input resistance and parasitic capacitances at the X and Z nodes of the CFA. The difference between circuits 1 and 2 particularly for $r_{in,x}$ and r_Z can clearly be seen here. Also comparing circuit 1 with Fig. 1(b) of [9] the values of $r_{in,x}$ and r_Z compare favorably when the bias current of Fig. 1(b) is in excess of 80 μA. The power consumption of each circuit was also extracted from the simulations and is shown in Table 2 for two supply ranges 3.3 V and 1.8 V. Note that at a 1.8 V supply, the bandwidth of each circuit was reduced approximately by half as to be expected and the power consumption reduced to 2.2 mW and 4.7 mW for circuits 1 and 2, respectively.

Finally, due to available space only of the two circuits was fabricated, that is circuit 1 in TSMCs 0.35 μm process. A photograph of the chip layout is shown in Fig. 6(a). The input conditions used for testing were the same as those of the simulation results except that the test chip containing circuit 1 was driven from a LT1364 seventy megahertz Dual opamp to generate the required input AC and DC levels. The test setup arrangement is shown in Fig. 6(b). The LT1364 is a bipolar CFA that was used in the unity gain configuration with a bandwidth of 70 MHz. An error in laying out C_{c1} for circuit 1 resulted in a value far less than the 5 pF required. This meant that the first op-amp in circuit 1 could not be compensated properly resulting in a non-dominant pole response. However, in a closed loop configuration the op-amp still proved to be stable in simulations despite the error in C_{c1}. The measured results shown alongside the simulation results for comparison purposes in Fig. 7 confirm this was the case.

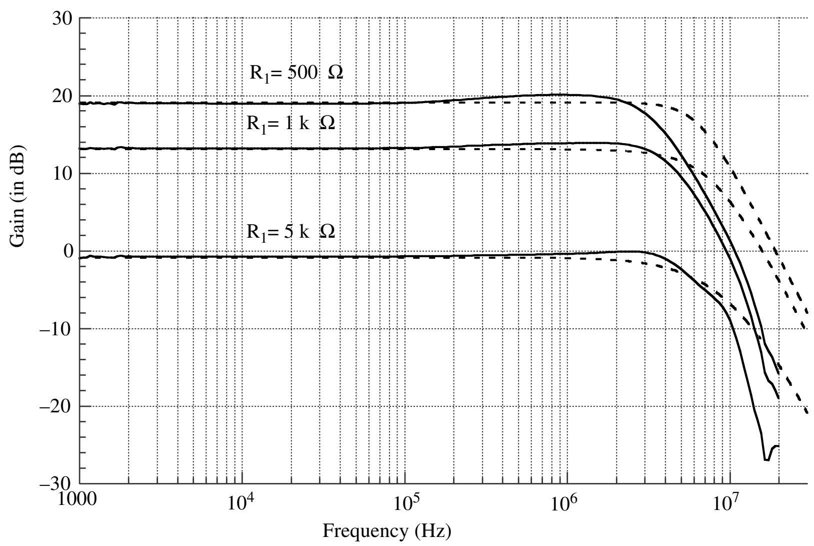


Fig. 7. Measured frequency response results for circuit 1 with gains of -1, -5, and -10 are shown with solid lines. The dashed lines represent the simulation results duplicated from Fig. 5(a).

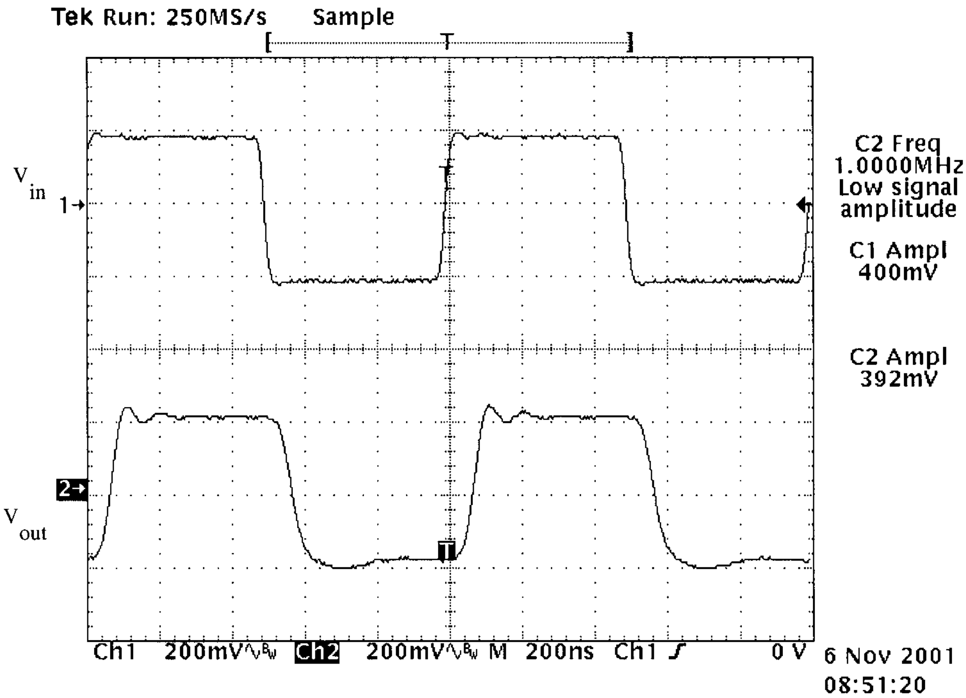


Fig. 8. Transient response of circuit 1 at a gain of −1 to a 1 MHz square wave input. Top trace is V_{in} to the LT1364 op-amp. Bottom trace is V_{out} of circuit 1.

Note that the measured bandwidth of the closed loop amplifier in circuit 1 was 6.4 MHz which is in good agreement with the results from simulation. The DC gains of the amplifier for input resistor R_1 of values 0.5 kΩ, 1 kΩ, and 5 kΩ were 8.9, 4.6, and 0.91, respectively which was also in close agreement with the simulation results. At high frequencies unforeseen parasitic board capacitances affected the performance of the circuit and could not be eliminated without altering the board design. Note it was not possible to measure the power dissipation associated with circuit 1 because its supply line was integrated with other circuitry on the test chip. Finally, Fig. 8 shows the small signal response of circuit 1 for a gain of −1 to a peak to peak input signal of 400 mV. The output can be seen to be faithfully following the input given the inversion due to both the LT1364 and circuit 1.

5. Conclusion

Two simple low-voltage current feedback amplifiers have been presented. As expected for CFAs, they maintain a nearly constant closed loop bandwidth as the closed loop gain is varied. The bandwidth of the CFA depends on the feedback resistor R_f and the compensation capacitor. Circuit 2 performs better than circuit 1 by virtue of its higher output impedance at the Z terminal, but uses nearly three times the transistor count of circuit 1. Even though circuit 2 was not manufactured it is expected that its performance would be comparable with the obtained simulations results as was the case for circuit 1. Finally, both circuits are suitable for a range of applications such as high frequency filters.

Acknowledgments

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Dr. Brent J. Maundy received his B.Sc. and M.Sc. degree from the University of the West Indies, Trinidad in 1983 and 1986, respectively. In 1992 he received his Ph.D. from Dalhousie University (formerly TUNS) while working in the area of analog neural networks. In 1983–1984 he worked as an electrical engineer in TSTT. During the periods 1986–1988 and 1993–1994 he taught at the University of the West Indies as a lecturer in the areas of electronics and communications. He was a visiting assistant professor at the University of Louisville in 1995. Later on that year he joined Litton Systems Canada as a system engineer where he worked on firmware products for the defense industry. He subsequently joined the Department of Electrical Engineering at the University of Calgary as an assistant professor in 1997, teaching graduate and undergraduate courses in filter design, and circuit analysis. His main research interests are in low voltage analog IC design, filter design and analog signal processing applications.

Dr. Ivars G. Finvers received his B.Sc. and M.Sc. degrees in electrical engineering from the University of Alberta in 1985 and 1988, respectively. In 1994 he received a Ph.D. degree from the University of Calgary for his work on precision CMOS amplifiers for high temperature instrumentation applications. From 1985 to 1986 he was a Member of Scientific Staff at Bell Northern Research engaged in the development of test equipment for fiber optic system installation and monitoring. The period between his M.Sc. and Ph.D. degrees was spent at NovAtel Communications Ltd. as an IC design/test engineer responsible for the design, simulation, testing, and support of custom integrated circuits for cellular telephony applications. He was with Mitel Semiconductor from 1995–1997, where he was involved in all aspects of the design, testing, and production of standard product telecommunication ICs. In 1997 he joined the University of Calgary as assistant professor and focused his research on high performance analog CMOS circuits for telecommunications applications. At the beginning of 2000, he took a leave of absence from the University of Calgary to become Director of Analog ASIC Development at SiWorks Inc.

Dr. Peter Aronhime is professor of electrical and computer engineering at the University of Louisville. He received the BEE from the University of Louisville and the MSEE and Ph.D. from Colorado State University, Ft. Collins, CO. He has held engineering positions at Bell Telephone Laboratories, Winston-Salem, NC, and at Hughes Aircraft, Fullerton, CA where he designed linear- and switch-mode regulated power supplies. Before returning to Louisville in 1976, he was a faculty member in the Electrical Engineering Departments of Tri-State University, Angola, IN, and the Illinois Institute of Technology, Chicago. His research interests include: network theory, design of analog signal processing systems, instrumentation, and computer-aided testing of analog circuits and devices.

Dr. Aronhime was an NSF Science Faculty Fellow and has received the IEEE Louisville Section Outstanding Electrical Engineer Award (1981) and the Outstanding Engineering Educator Award (1990 and 1994). He received the University of Louisville's Distinguished Teaching Professor Award (1986), the Alumni Scholar for Teaching Award (1995), and the Thomas M. Murray, Jr. Outstanding Teaching Award (1995–1996). In 1998, he was a co-recipient of the Myril B. Reed Best Paper Award. He received the IEEE Third Millenium Medal awarded by the Louisville Section. Dr. Aronhime is a senior member of the IEEE, a member of the Steering Committee of the MWSCAS, and a member of the IEEE CAS Analog Signal Processing Technical Committee. He is a member of Eta Kappa Nu, Sigma Xi, Phi Kappa Phi, and Omicron Delta Kappa.