PV Balancer
--Concept, Architectures and Realization

by

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Abstract

This thesis presents a new concept of module-integrated converters called PV balancers for photovoltaic applications. The proposed concept enables independent maximum power point tracking (MPPT) for each panel, and dramatically decreases the requirements for power converters. The power rating of a PV balancer is less than 10% of its counterparts, and the manufacturing cost is thus significantly reduced.

In this work, two architectures of PV balancers are proposed, analyzed, realized, and verified through simulation and experimental results. In addition, future work which will focus on enlarging PV balancer's merits and solving its shortcomings is mentioned as well. It is anticipated that the proposed approach will be a low-cost solution for future photovoltaic power systems.

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Chapter 1 Introduction

Background

Photo-Voltaic History

After Becquerel first observed an important method to converter solar radiation into electricity by photovoltaic effect [10], Photovoltaic (PV) power supplied to the grid is gaining more and more visibility, and PV market saw a burgeoning growth. This is driven by the factor of increasing power demand and worldwide concerns about the global warming with finite non-renewable energy. Digitimes Research estimates that total global new PV system installations reached 25,000 GWp in 2012, representing 13.8% growth on the 2011 figure [11].

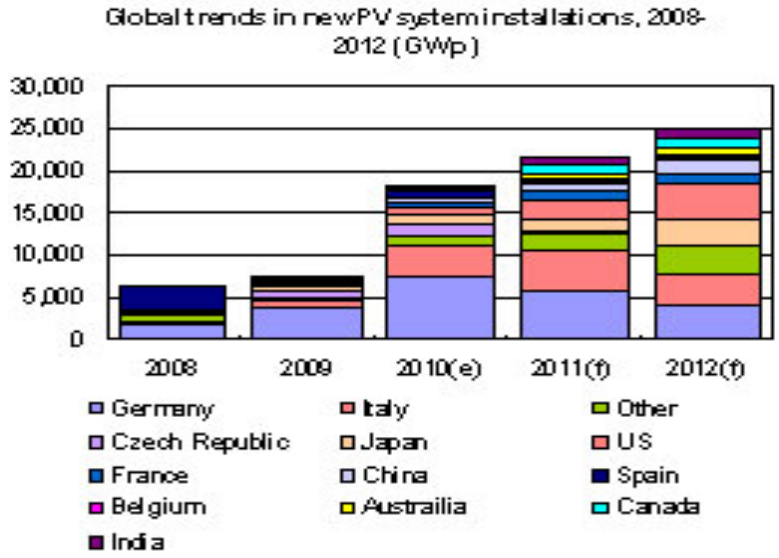


Figure 1 Global trends in new PV system installations, 2008-2012 (GWp) [11]

Photovoltaic Module Modeling and Electrical Characteristics

Practically all photovoltaic devices incorporate a pn-junction in a semiconductor across which the photovoltaic is developed. These devices are also known as solar cells [10]. A solar cell can be simply modeled as a current source (I_L), which is directly

proportional to the light falling (G) on the cell, in parallel with a diode. Additional shunt resistor R_{SH} and series resistor R_S could be concluded when power loss is considered under a real operation. Figure 2 [8] depicts an equivalent circuit model for the PV cell. PV panel is then accomplished by series connecting PV cells for a higher output voltage or by parallel connecting PV cells for a higher output current.

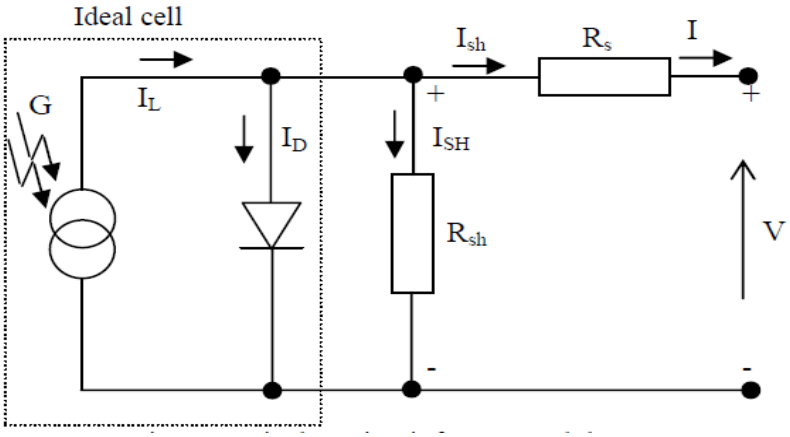


Figure 2 Equivalent Circuit Model for a PV Cell

Math equations for a PV panel based on the PV cell equivalent circuit model are explicated below [8] [9].

$$I = I_L - I_0\left(e^{\frac{V+I\,R_S}{n\,V_t}} - 1\right) - \frac{V+I\,R_S}{R_{sh}} \quad (1)$$

Where, Vt is the junction thermal voltage

$$\mathrm{V_t} = \frac{\mathrm{AkT}}{\mathrm{q}} \quad (2)$$

The diode saturation current I_0 and I_L are temperature dependent.

$$\mathrm{I_L} = \mathrm{I_L(T_1)} + \mathrm{K_0(T - T_1)} \quad (3)$$

$$\mathrm{K_0} = \frac{\mathrm{I_{SC}(T_2) - I_{SC}(T_1)}}{\mathrm{T_2 - T_1}} \quad (4)$$

$$\mathrm{I_0} = \mathrm{I_0(T_1)} \times \left(\frac{\mathrm{T}}{\mathrm{T_1}}\right)^{\frac{3}{\mathrm{A}}} \mathrm{e}^{\frac{\mathrm{qV_q(T_1)}}{\mathrm{nk}\left(\frac{1}{\mathrm{T}} - \frac{1}{\mathrm{T_1}}\right)}} \quad (5)$$

There are several parameters appeared in the math model above, while k is Bolzmann's constant, q is the charge of the electron, n is the number of cells in the panel connected in serious, A is the diode quality (ideality) factor, V_q is the band gap energy of the semiconductor, T is the real temperature and T_1, T_2 are the given reference temperatures. Other electrical terms are I_{SC}, short circuit current, which produced by the short circuit condition V=0: $I_{SC}=I_L$; V_{OC}, open circuit current, which is produced by the open circuit condition $I_{sc}=0$; Since this work only focuses on solving power output of each PV panel under different illustration, the temperature factor is neglected for brevity in the following part of this thesis.

For any given set of operational conditions, modules usually have a single operating point where the values of the output current (I) and output voltage (V) of a module result in a maximum power output, which is known as the maximum power point (MPP). While the MPP shifts under different solar irradiances, the module output current varies greatly yet the output voltage varies slightly. This is partly because a solar cell is a p-n junction and its V-I characteristics are similar to that of a diode.

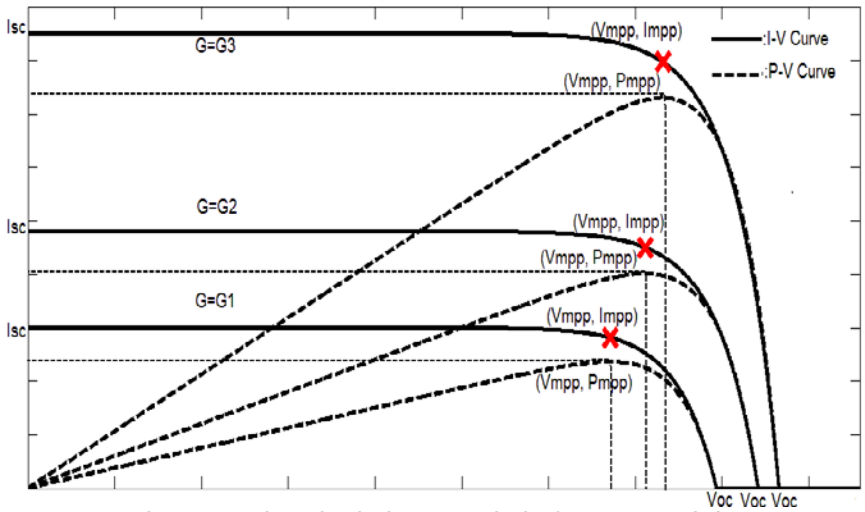


Figure 3 Electrical characteristic for PV module

MPP, Maximum Power Point: $P=P_{MPP}$, $V=V_{MPP}$, $I=I_{MPP}$

Single Phase Grid Connected Converters for PV application

Solid-state converters have been defined as the enabling technology for combining PhotoVoltaic into the utility [1]. Numerals of approaches for grid connected PV installation have been proposed and thus commercially implemented in the past decays, such as centralized, string, multi-string, and Module-integrated converters (MICs), etc. The following part is concentrated on a broad overview of these different topologies.

A. Centralized Inverter

Centralized inverter as illustrated in figure 4 is the first generation for PV application; the PV modules are divided into several strings, each string generates sufficient high voltage, eliminating further voltage boost. These strings are then paralleled connected through a string diode to get sufficient current/power [1]. The nominal power of this topology can be up to several megawatts [14].

Although this topology is robust, high efficient and cheap, the major shortcomings for centralized inverters are: the required DC wiring increases cost and extra protection consideration; Maximum Power Point Tracking (MPPT) is not accessible for each panel, mismatch among panels caused by partial shading may thus dramatically decrease the total output; A flexible system is difficult to achieve because of the high power range and series connection of the modules [12].

B. String Inverter

As an enhanced version of centralized inverter, string inverter topology series connects PV modules in a single string to reach as high as several hundred Volts and several kilowatts power. There is little loss for the string diodes and independent MPPT can be maintained at the string's level, reasonable cost and high efficiency due to mass

production can also be drawn by this method. Figure 5 depicts a typical string inverter topology [1].

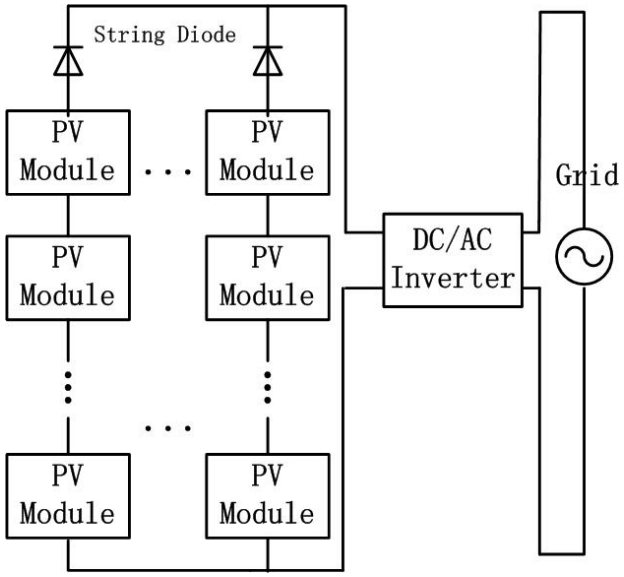


Figure 4 Centralized Inverters Configuration

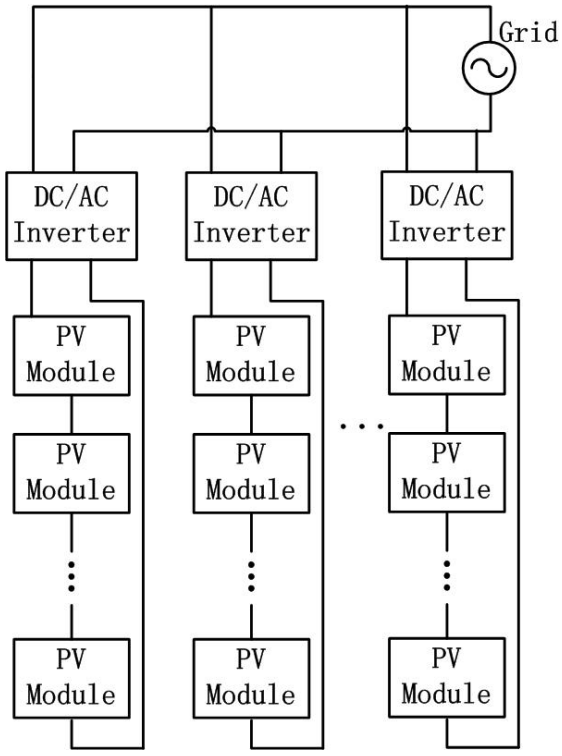


Figure 5 String Inverters Configuration

C. Multi-string Inverter

Multi-string inverter, as shown in Figure 6, inherits the merits of low costs of centralized inverters and higher efficiency of string inverters. Lower power DC/DC converters are stacked to a single string in order to keep MPPT at the string level; several strings are parallel connected to a DC bus by their individual DC/DC converter for a higher power output. The DC bus then feeds power to the grid through a DC/AC converter.

Nevertheless, neither string inverter nor multi-string inverter has performed MPPT at the PV module level. A single PV panel output is still subjected to the performance of its neighbors. The total tolerance of the PV system against the solar irradiants mismatch had not yet been mitigated. Researchers and industries are still seeking for alternatives for a higher power output capturing.

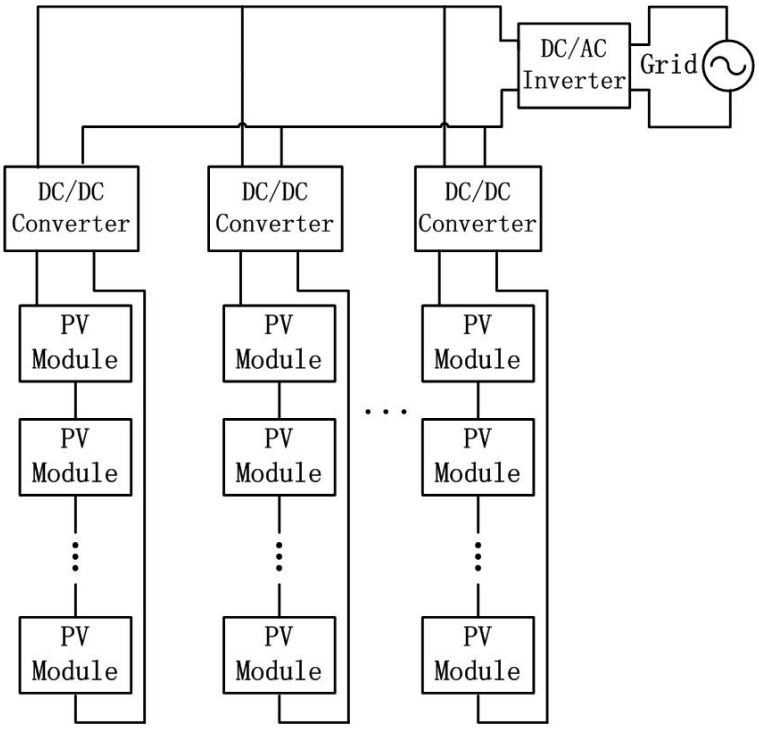
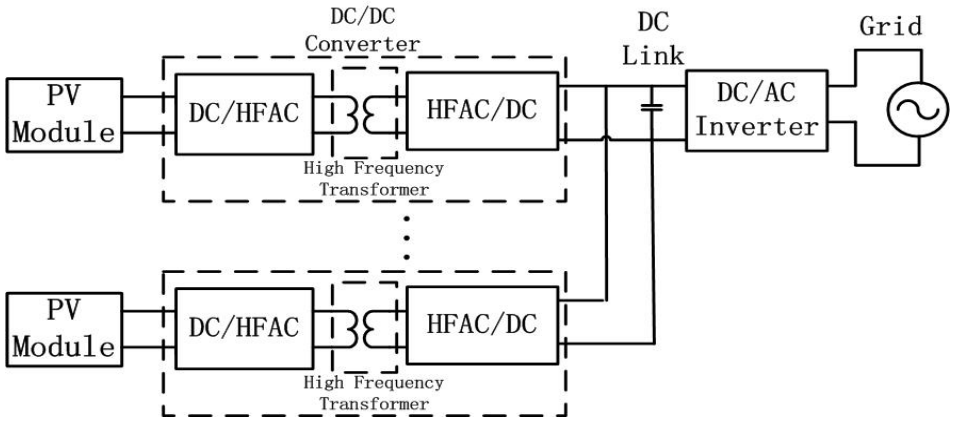


Figure 6 Multi-String Inverters Configuration

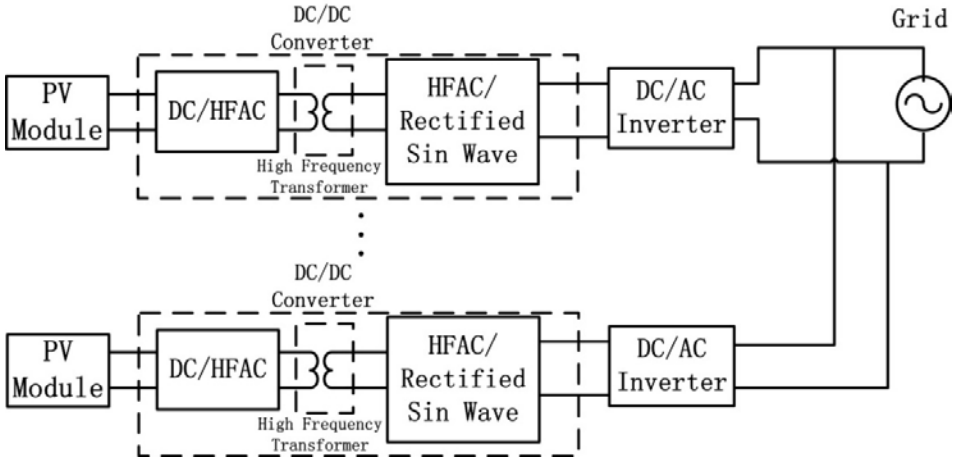
D. AC Modules / PV Module Integrated Converters (MICs)

The AC module or PV module integrated converter (MIC) is the integration of the DC/DC or DC/AC converter and a PV module into one electrical appliance. This novel technology has been rapidly developed in recent years for more than a few qualities: individual MPPT for each PV panel has removed mismatch among different panels so that maximum power output has been captured even if some panels are under partially shaded; parallel connection of these AC modules to the grid has made “plug in and play” device become possible; although further voltage amplification has lower the total efficiency and power density, mass production has dramatically decreased the manufactory and installation cost [1].

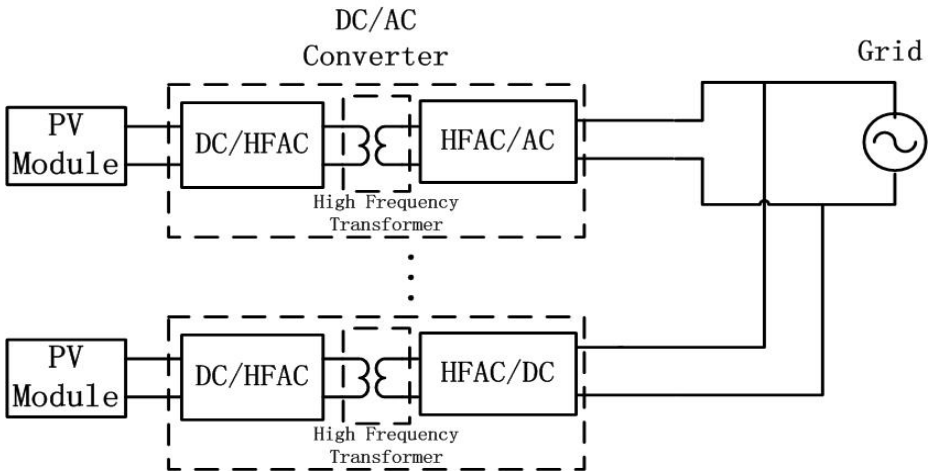
In general, either a line frequency or a high frequency transformer can be implemented as the voltage amplifier from the low voltage of the PV module output to higher voltage of the grid [13]. Soft switching technology such as Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS) allows resonate converter / high frequency transformer to be incorporated with incomparable higher efficiency and less power loss [4]; therefore, line frequency transformer will not be an optimum application here. Figure 7 depicts three typical MIC scenarios---MIC with a DC link, MIC with a pseudo DC link and MIC without a DC link--- in terms of the DC link configuration [13].



a. MIC with DC Link



b. MIC with Pseudo DC Link



c. MIC without DC Link

Figure 7 Three typical MIC scenarios

In order to achieve transformer-less approach and mitigate mismatch in the string topology, G.R.Walker and J.C.Pierce first proposed another power capatured-effective alternative, which is referred to as Cascaded DC/DC MICs [3] [15].

A cascaded DC/DC MICs prototype as shown in figure 8, the MPPT module-oriented DC/DC converters are series connected in a string and feeding power to the grid via a DC/AC inverter. Such PV power plants have nominal power ratings of are up to several megawatts [14], and increase energy capture by more than 30% if there is temporary shade or a permanent defect on a panel [2].

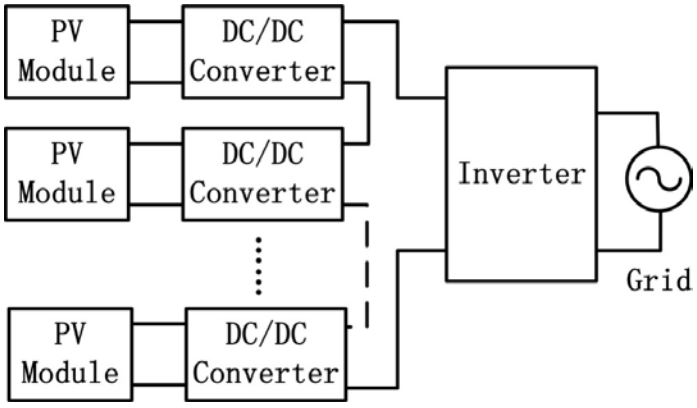


Figure 8 Cascaded MICs Configuration

However, all the MICs discussed above have one critical challenge: the module-oriented converter process full power generated by its integrated PV panel, so the converter must have an accordingly power rate, thus, MICs technologies nowadays have suffered the key disadvantage of higher equipment initial cost. And also, the solar power system is very sensitive to the efficiency of power converter; bad performance of the converter can erode the total solar productivity [15].

Bypass DC/DC MIC [15] or Generation Control Circuit (GCC), which is originally invented by Toshihisa Shimizu [6] [7], and further developed by G.R.Walker and J.C.Pierce [15] [16] is expected to compensate different current among these PV

Modules stacked in a series string. The module- converters utilized in this very unique scenario only process partial power generated by the PV modules, and under nominal condition, no power goes through these by-pass converters [15]. Figure 8 illustrate one typical GCC configuration. Other characteristics such as MPP is maintained for each PV module including shaded modules, no future voltage boost is required, and the decrease in the total generation power is minimized are just the same as the cascaded DC/DC MICs.

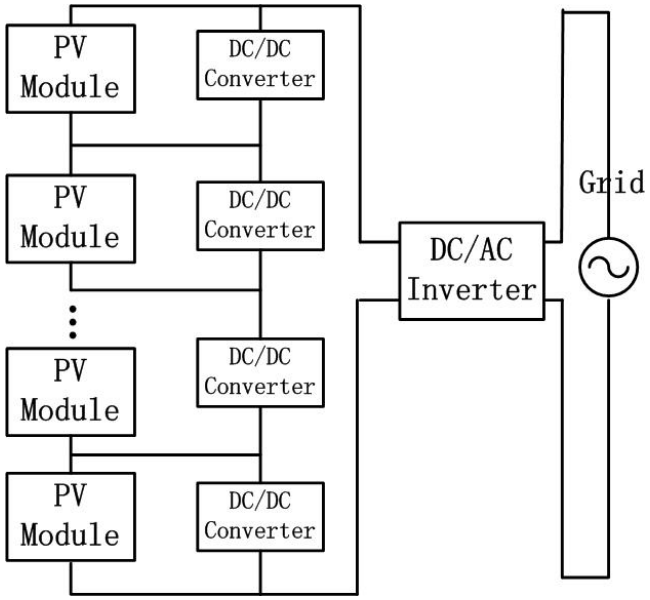


Figure 9 Scenario of Generation Control Circuit

It is necessary to note that, for above two prototypes---cascade DC/DC MIC and GCC---under the greatest mismatched conditions, e.g. when one module in the string is generating its maximum power and other modules are completed shaded and generate little power, the module-integrated converters may be unable to maintain the minimum inverter input voltage and the total efficiency penalty will be increase. Moreover, although the GCC converters are claimed to process partial power of their connected panel, they are required to provide full power if the connected panels are completed

shaded or failed. The converters, thus, must have current, voltage and power ratings equivalent to the panels they support [16].

E. PV Cells

For the AC Cells, where one large PV cell is directly connected to the grid through a dc-ac inverter, the use of an entire module-size thin film layer results in a simpler manufacturing process and lower the cost, but the main challenging for this design is high voltage boost from 0.5-1V to about 110V grid level, thus, converts call for a new concept and special design [1].

Organization of the thesis

compared to GCC technology, PV Balancer, compensates differential voltage, eliminates deep buck mode [16] for a module-integrated converter under a series mismatch condition, and power rating for this kind of MIC is ‘really’ partial of the output of the PV panel. Chapter 2 below will devote to illustrate a thorough knowledge of this new MIC including motivations, two architectures based on this proposal, analysis of advantages and disadvantages, in additional, a similar concept referred as SCBU will be analyzed and compared with PV balancer; Chapter 3 and 4 will present software and experimental verification respectively; Chapter 5 will address the benefits and main challenges for this new approach and proposals for the future work.

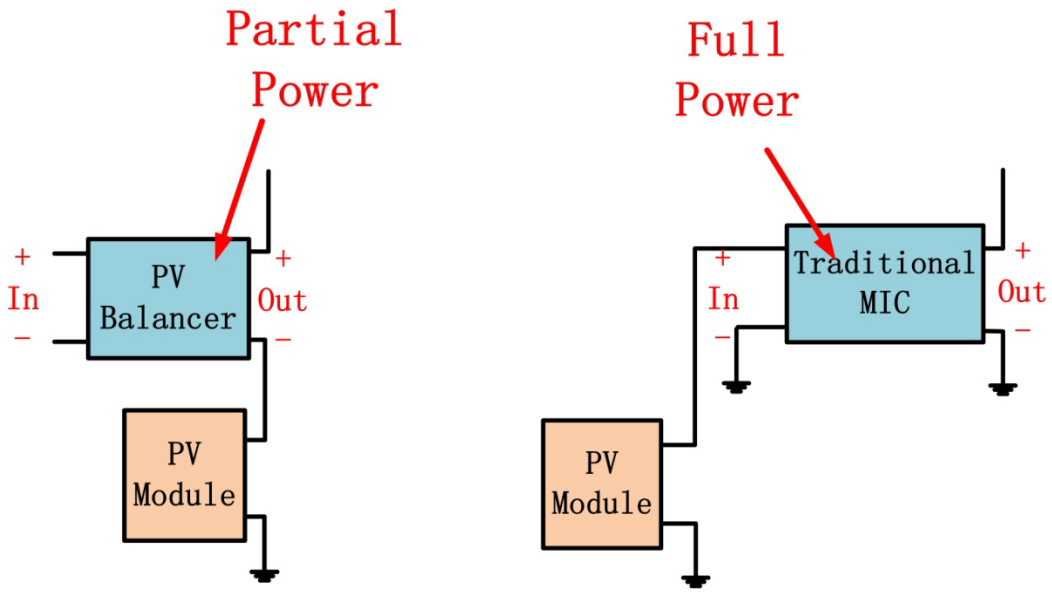
Chapter 2 PV Balancer

Motivation and Concept of PV Balancer

While the purpose of GCC in PV application is compensating differential currents among series PV modules in a string, the PV Balancer is compensating differential voltages among paralleled PV modules. Figure 10 sketches a basic circuit model for one single PV Balancer and it is compared to a traditional MIC.

The driven force of this new idea can be observed from VI Characteristics shown in figure 2. The module output current varies significantly while the output voltage varies slightly when the MPP shifts under different solar irradiances. For instance, in figure 2, the current varies from 1.83A to 0.35A from curve G3 to curve G1, and that the voltage only varies from 20.97V to 24.24V.

Even though, comparing to traditional MICs, both converters in GCC and PV balancer prototypes are dedicated to processing partial power instead of whole power generated by the PV panels, the power rating of the module-integrated converters in the PV balancer are significantly minimized. The reason is very simple: because power = voltage × current and the differential voltage is about 10 times smaller than a single module output voltage, PV balancer only procedures less than 20% of the total power; however, in GCC, because the module current varies greatly, this approach cannot reduce the power rating of the module-integrated converters significantly. In fact, for design purpose, the converters in GCC should be capable of the same current, voltage and power ratings as the panels they support [16].



(a) PV balancer (b) Traditional MIC

Figure 10 Comparison of the proposal concept and a traditional MIC

As a brief summary, the proposed PV balancer enables independent MPPT for each panel, reduces mismatches between different modules, and maximizes the total energy extraction. Compared to the conventional topology, the new concept enables 80% reduction of the power rating and power loss of a module-integrated converter, thus decreasing the manufacturing cost and increasing total efficiency significantly. Even in harsh mismatch conditions, the PV balancer is able to reach the required efficiency and maintain the inverter input voltage. It is anticipated this approach will reduce the PV converter cost and help reach the eventual goal of $1 per watt and 1W per cm^3 power density for PV systems.

Architectures for PV Balancer

Two possible architectures of PV Balancers are shown in figure 11 and 12. These balancers are not limited by their circuit topologies; actually, they are essentially dc-dc converters integrated into each panel and combined at a common DC bus. The DC bus

feeds the power to the utility at the inverter stage. The DC bus voltage is a little higher than the maximum output voltage of PV modules. PV balancers autonomously regulate their output voltage and compensate for the differential voltages between the DC bus and each module. Since the output voltage and output current of each panel can be set independently, PV modules operate at their own maximum power points, maximizing the energy harvested. Detailed analysis of these two architectures is presented in the next session.

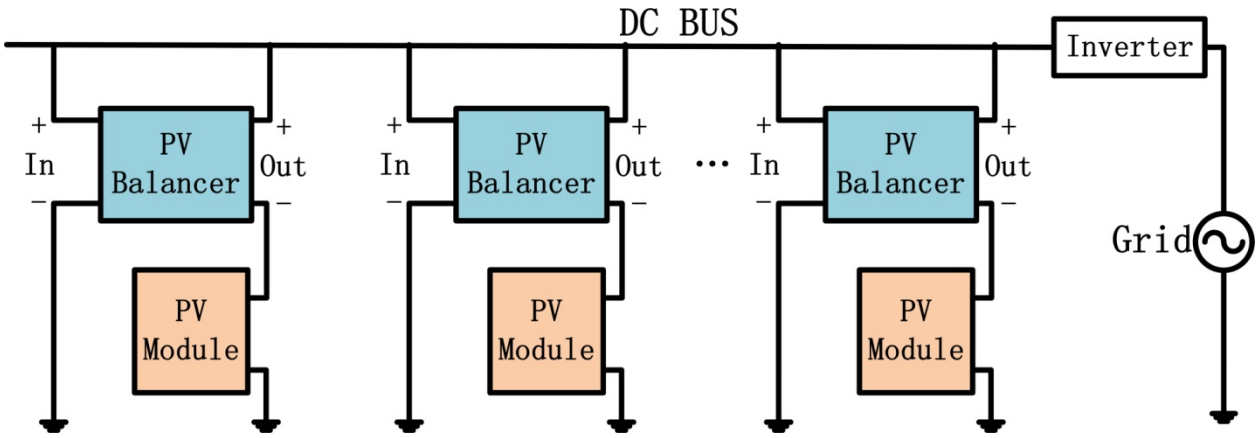


Figure 11 Architecture I of PV balancers

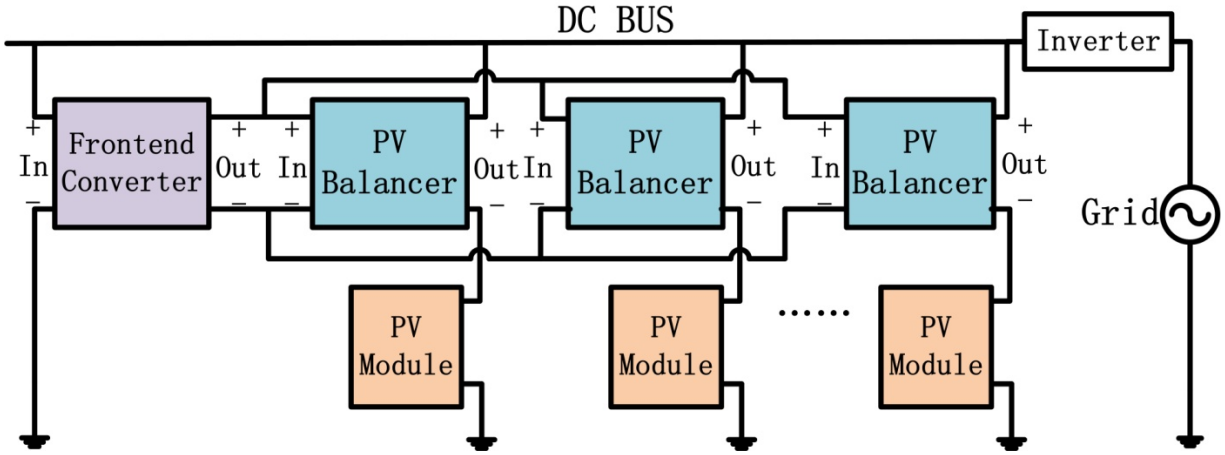


Figure 12 Architecture II of PV balancers

Architecture I

Figure 11 above depicts the first design architecture for the PV balancer. The input is from the common DC bus, and the output is the compensation voltage between the DC bus and PV module. This architecture is simple and modularized, but the PV balancers have a high voltage transformation ratio that may incur an extra cost and lower efficiency.

Architecture II

As an improved version for the architecture I, the second type of PV balancer shares a front-end converter as the input. The front-end converter steps down the DC bus voltage and feeds relatively low voltage to the PV balancers in each module. This architecture is more economical and efficient.

For instance, suppose that the DC bus here is set to be 28 Volts and the compensating differential voltage is only about 3 Volts; In Architecture I, the voltage ratio is nearly 9:1 for each balancer. But, for the alternative approach, a considerable voltage drop, such as 28: 10, can be accomplished by the front-end converter, thus, voltage transfer ratio is only around 3:1 for each balancer and a simple transformer-less DC/DC converter can be utilized. However, the wiring, design and control are also more complicated in architecture II. Frontend output voltage control which will be investigated in detail in the next part is one of these challenges.

To study the PV balancers qualitively, we define the V_{MPP} and I_{MPP} as the output voltage and the output current of a module operating at its maximum power output P_M. From above definitions, we have

$$P_{MPP} = V_{MPP} I_{MPP} \quad (6)$$

We define VDC as the value of the DC bus voltage, V_{OUT} as the PV balancer output voltage, I_{OUT} as the PV balancer output current, and P_{OUT} as the PV balancer output power. We get

$$V_{OUT} = V_{DC} - V_{MPP} \quad (7)$$

Because the PV balancer is in series with the PV module at the output, we have

$$I_{OUT} = I_{MPP} \quad (8)$$

$$P_{OUT} = V_{OUT} I_{OUT} = (V_{DC} - V_{MPP}) I_{MPP} \quad (9)$$

The ratio between the PV balancer output power and the module output power is

$$R_{PwR} = {}^{P_{OUT}}/_{P_{MPP}} = {}^{V_{OUT}}/_{V_{MPP}} = {}^{V_{DC}}/_{V_{MPP}} - 1 \quad (10)$$

As V_{DC} is only a few volts higher than V_M, R_{PWR} is usually less than 20%.

We define P_{LOSS} as the power loss of the balancer, P_{IN} as the input power of the balancer and η as the effiency of the PV blancer. We get

$$\eta = \frac{P_{OUT}}{P_{IN}} = 1 - \frac{P_{LOSS}}{P_{OUT}+P_{LOSS}} \approx 1 - \frac{P_{LOSS}}{P_{OUT}} \quad (11)$$

To compare the efficiency of the PV blancer to a traditional MIC, the power loss of the PV balancer need to be normalized by the module output power P_{MPP}(which is equal to the input power of the traditional MIC) and the equivalent efficiency of the PV balancer is:

$$\eta_E = 1 - \frac{P_{LOSS}}{P_{MPP}} = 1 - R_{PWR}\frac{P_{LOSS}}{P_{OUT}} \quad (12)$$

As R_{PWR} is usually less than 20%, the equivalent efficiency η_E is significantly higher than the PV balancer efficiency η.

Realization for Architecture I and II

Since the PV balancer is designed to boost the PV panel output voltage to reach the DC bus value, many types of non-inverting power converters, such as Flyback, SEPIC, Buck and Forward, etc, are suitable for developing this new concept converter. For the purposes of demonstration, flyback converters are employed as PV balancers in Architecture I. In Architecture II, buck converters are employed as PV balancers for each panel and a flyback converter is employed as the frontend.

Realization for Architecture I

Any given DC/DC converter with a transformer inside can be utilized as the PV balancer, such as Flyback or Forward converter. Just for demonstration, a Flyback converter with positive input and output voltages has been implemented here, depicted in figure 13. The input of the Flyback is from the common DC bus and converter's output is series attached to the PV panel to boost the voltage.

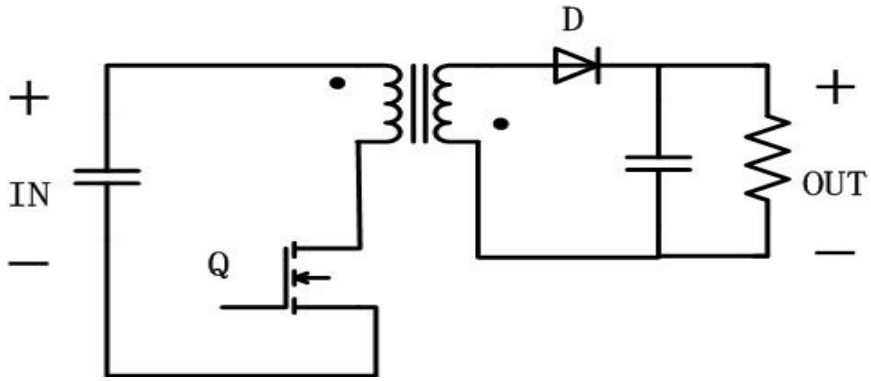


Figure 13 Non-inverting Flyback Converter

Realization for Architecture II

In this dual level topology, the front end converter use the same Flyback (or Forward etc.) depicted above. In addition, since the frontend Flyback steps down the voltage for

the balancers, these DC/DC converters could have smaller voltage ratio so a simple buck converter can meet the voltage ratio requirement. However, a special design for the buck converter should be considered for the floating output limitation mentioned above: observed from figure 12, the buck converter should have positive grounding instead of negative grounding. Therefore, in figure 14, a unique scenario for the Buck converter is proposed and implemented here.

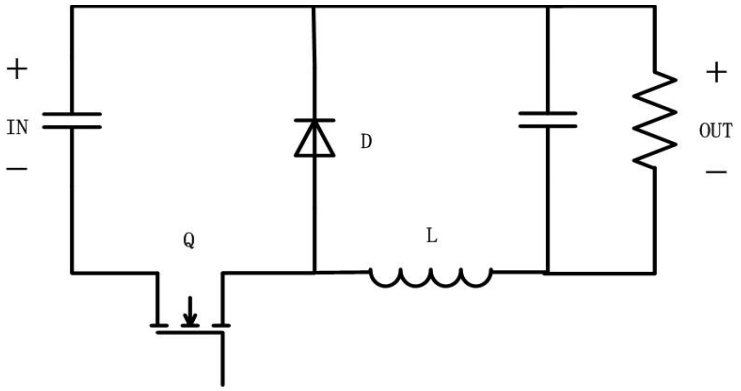


Figure 14 Proposed Prototype of Buck Converter

DC Bus Voltage and Frontend Output Voltage Control

Unlike conventional design, the outputs of PV balances should be positive grounding and be grounded with the DC bus, thus DC bus voltage needs to be controlled extremely carefully. If the dc bus voltage is too close to the panel voltage, the voltage transformation ratio of a PV balancer will be too high, although the power rating of PV balancers would be lower. If the DC bus voltage is too high, the voltage transformation ratio may be lower but the power rating of PV balancers would be increased.

Besides, in architecture II, the frontend output voltage also requires caution since voltage transfer ratio for the buck converter has a practical boundary, generally, greater than 20%. Thus, a practical problem comes out: if the voltage is set to be other than an optimum value, some PV balancer will have voltage transfer ratio larger than 100% or

smaller than 20%, so the PV balancer needs to be replaced by a non-inverting buck-boost converter for a large output voltage range, this yields an extra cost and lower efficiency.

Numerical studies based on the above analysis can be derived from equation (13) to (16).

$$V_{BR} = V_{DC} - V_{PV} \quad (13)$$

$$D_{BR} = \frac{V_{BR}}{V_{FD}} \quad (14)$$

$$(R_{BR})_{min} \geq 20\% \ , \quad (15)$$

$$(R_{BR})_{max} \leq 100\%, \quad (16)$$

Where, V_{BR} is the output voltage of the PV balancer; V_{DC} is the voltage of the DC bus; V_{PV} is the solar panel output voltage under its MPP condition; R_{BR} is the voltage transfer ratio of the balancer buck converter.

$(R_{BR})_{min}$ occurs at the condition V_{PV} is at its maximum value, i.e. the panel are under full illumination, less voltage boost is required from the balancer; $(R_{BR})_{max}$ occurs at the condition V_{PV} is at its minimum value, greater voltage compensation is required from the balancer, i.e. the panel are under most severe illumination.

Comparison of the PV balancer and the idea of SBCU

Concept of SBCU [21]

The Series Connected Boost Unit, SCBU for short converter, is derived from the idea of biasing an isolated voltage source on another source. It adds an isolated DC-DC converter to a PV panel to reach a unique series connection, and transmits power to the load. The DC/DC converter utilized here also only takes partial power generated by the panel, so this SCBU can be considered as high efficiency, high power density, high

reliability and low cost technique for the future PV application. Figure 15 helps better illustrate the SCBU topology.

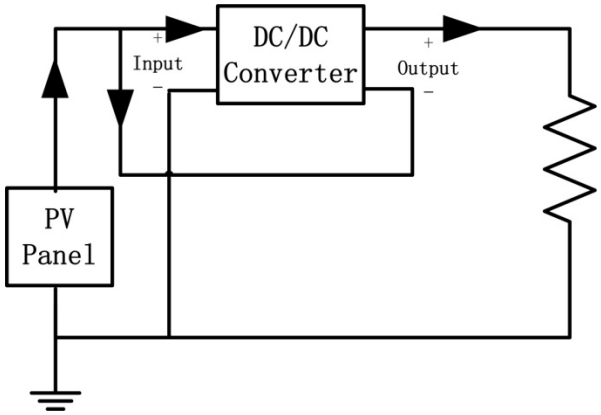


Figure 15 Topology of SCBU

Identify PV balancer and SCBU

Although SCBU also allows the DC/DC converter to handle partial power generated by the module, and realizes a low-cost high-efficiency solution for photovoltaic applications. SCBU can be also used in PV balancer architectures. There are some major differences to identify the idea proposed in this paper from SCBU.

First, the application objectives are not same. The SCBU is focused on any single PV input feeding a single load while the PV balancers are trying to eliminate the mismatch among multiple PVs connected to the utility grid and improve the performance at the system level.

Second, the circuit connections are not the same. The input of a SCBU is from the PV module so it requires galvanic isolation within the DC/DC converter, however, the input of a PV balancer is from the DC bus, the input and output of PV balancers can be grunded at the common dc bus without isolation.

Third, the voltage transformation ratios and the power flow are different. The SCBU may have a smaller voltage transformation ratio because the output voltage of PV module is a little lower than the DC bus voltage. But the input power of SCBU must receive from the PV module connected to it while the input power of a PV balancer is from the common dc bus, which is not limited to the PV module connect to it.

Chapter 3 Software (Matlab/Simulink) Simulation Results

Just like any engineering project, it is indispensable to simulate the new concept in the PV application before hardware or experimental verification is undertaken. This chapter will present a detailed systematic simulation in Matlab/Simulink, including three PV modules modeling, each of which is rated around 40W under full irradiation and around 7W under 1/5 full irradiation, three Flyback converters modeling, referred as PV balancers in the first architecture, one Flyback converter and three special buck converter modeling, referred as the frontend and three PV balancers in the second architecture respectively.

PV Module Modeling

Though for design purpose, all the PV balancer and PV panels should be identical in terms of the specification of their voltages, currents and power ratings, since the irradiations for each panel are different, their working conditions (different illuminations) as listed in table 1 are not the same. Table 1 also includes open circuit voltages; short-circuit currents; output voltages, currents and power ratings under MPP conditions.

PV No.	V_{OC} (V)	I_{SC} (A)	V_{MPP} (V)	I_{MPP} (A)	P_{MPP} (W)	Illumination (W/m^2)	Temp (K)
1	24.80	0.375	20.97	0.35	7.38	200 (About 1/5 full illumination)	300
2	26.47	0.75	22.38	0.70	15.75	400 (About 2/5 full illumination)	300
3	28.67	1.95	24.24	1.83	44.35	1040 (Full illumination)	300

Table 1 Specifications for the three panel simulated in Matlab/Simulink

Electrical characteristics of the three modeling PV panels are plot in figure 16 and 17. The output voltages of the panels vary less compared to the current under different irradiation and working condition.

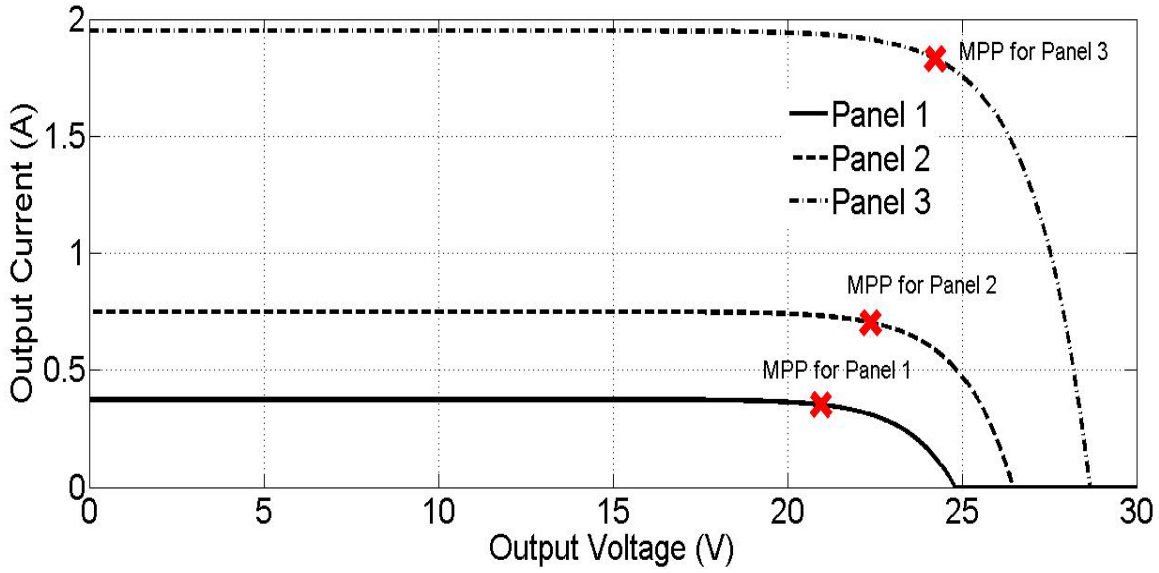


Figure 16 I-V Characteristic for the Three Panels

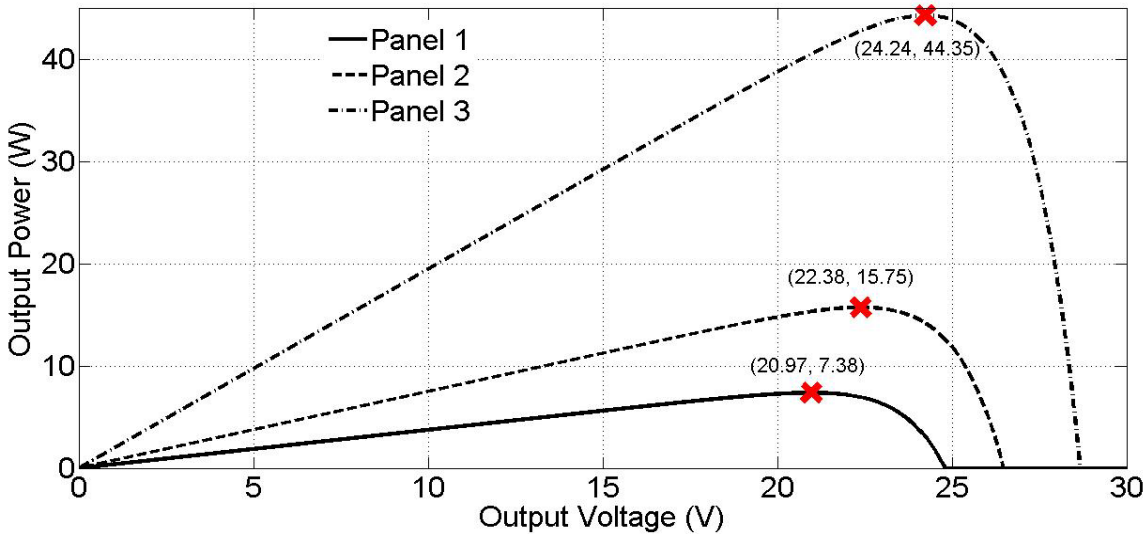


Figure 17 P-V Characteristic for the Three Panels

According to the equations (1) to (5), a controlled current source is modeled as the PV module in Matlab/Simulink, as expounded in Appendix 1.

PV Balancer Modeling

PV Balancer Modeling for Architecture I

For PV Balancer in Architecture I, a flyback converter and a subsystem accordingly are modeled in Matlab/Simulink, as presented in Appendix 2.

Frontend Converter and PV Balancer Modeling for Architecture II

As mentioned in last section, the frontend converter utilized in architecture II is the same as that in architecture I, only the voltage ratio and detailed specifications for each component varies.

For PV balancer in Architecture II, a buck converter and a subsystem built from the converter are modeled in the software, as shown in Appendix 3.

DC Bus Voltage and Frontend Output Voltage for this Simulation

DC bus voltage varies from case to case, how the value being determined should take output voltage range of the panels, practical voltage transfer ratio for a power converter and overall efficiency into account. Following of this section will provide a comprehensive method to find the optimum DC bus voltage and the power rating of PV balancer based on the optimized value and specification listed in table 1 for both architectures.

DC Bus Voltage for Architecture I

Figure 18 sketches what's the max/min power goes through each converter vs. different DC voltage, lower maximum and minimum power is better since the cost and size of power converter is proportional to its power rating. Figure 19 provides the minimum and maximum power ratio (min/max×100%) for a single converter vs. different DC voltages, greater ratio value is better since greater ratio indicates smaller power range for converters, thus, higher use efficiency.

An optimum value can be observed from 26.24V (2 Volts above the maximum voltage of panels' outputs and 6.27 Volts above the minimum voltage of the panels' output) to 28.24V (4 Volts above the maximum voltage of panels' outputs and 8.27 Volts above the minimum voltage of the panels' output) based on the observation of the two figures, any value lower than 26.24 would challenge a real power converter for a small output and input voltage ratio; any value greater than 28.24 would have a greater power rating of the PV balancer and lower use efficiency for a relatively low min/max power ratio.

A DC bus voltage which is equal to 28 Volts can be set in accordance with the summary above.

Therefore, the max voltage transfer ratio is:

$$(R)_{max} = \frac{V_{DC} - (V_{PV})_{min}}{V_{DC}} = \frac{28 - 20.97}{28} = 25.11\% \quad (17)$$

The min voltage transfer ratio is:

$$(R)_{min} = \frac{V_{DC} - (V_{PV})_{max}}{V_{DC}} = \frac{28 - 24.24}{28} = 13.43\% \quad (18)$$

Voltages, currents and power for each PV balancer are listed in table 2 below. Just for comparison, values for conventional MICs are also listed here:

		Input Voltage	Output Voltage	Output Current	Output Power
Flyback Converters in Architecture I	**1**	28V	7.03V	0.35A	2.48W
	2	28V	5.63V	0.70A	3.96W
	3	28V	3.77V	1.83A	6.89W
Conventional MIC	**1**	20.97	N/A	0.35	7.34
	2	22.38	N/A	0.70	15.67
	3	24.24	N/A	1.83	44.36

Table 2 Voltage, current and power for each PV balancer

As a summary for architecture I design, the DC bus is set to be 28 Volts, three Flyback rating at 6.89 Watts are required here as PV balancers, this power rating is only about 15% as that of a conventional MIC. The use efficiency for a single PV balancer is greater than and $\frac{2.48}{6.89} \times 100\% = 36.0\%$.

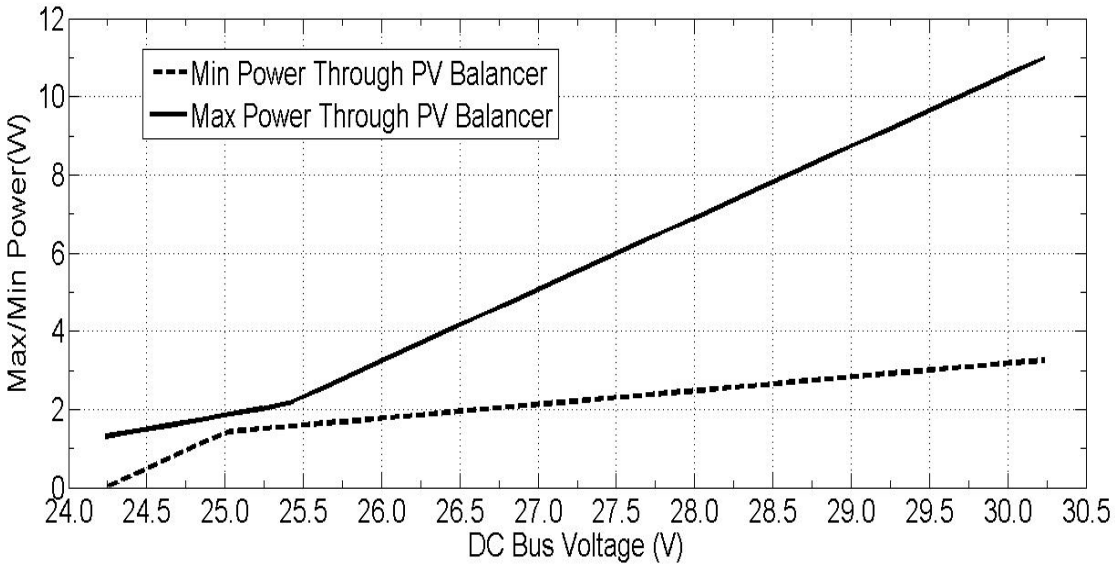


Figure 18 Max/Min Power Through Each PV Balancer vs. DC Voltage Value.

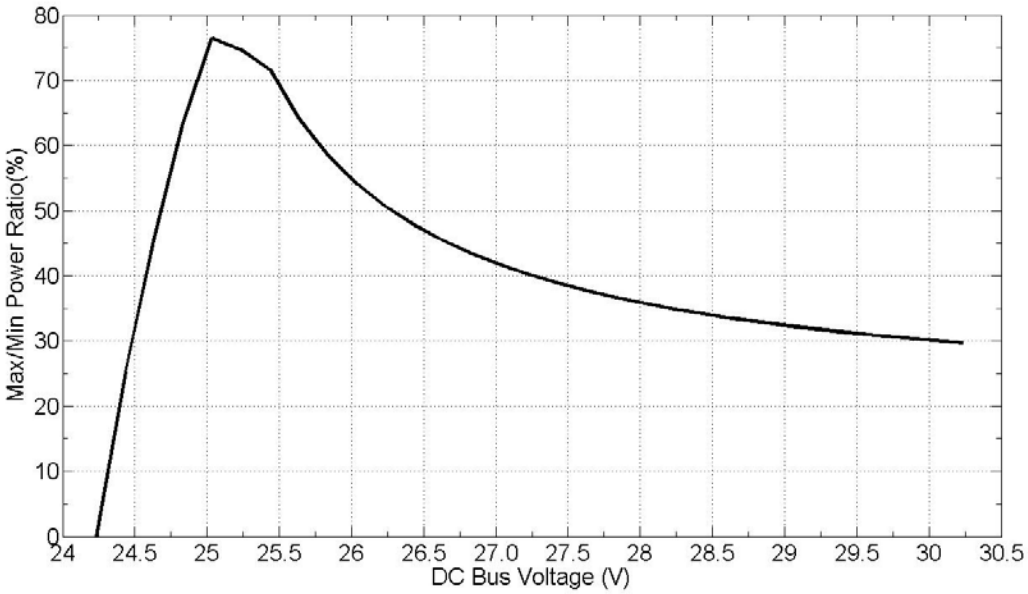


Figure 19 Max/Min Power Ratio Through Each PV Balancer vs. DC Voltage Value

DC Bus Voltage and Frontend Output Voltage Control for Architecture II

The max/min power through each PV balancer vs. DC bus sketched in figure 18 is also applicable for architecture II.

Based on equations (13) to (16), figure 20 depicts the relationship between the DC bus voltage and the maximum voltage transfer ratio of the PV balancer for varied minimum voltage transfer ratio of the PV balancer. Since it's hard to achieve very low output voltage with a high transfer ratio, it is meaningless to discuss DC bus voltage fewer than 26.24 Volts (2 Volts above the maximum voltage of panels' outputs). Thus, the DC bus voltage varies from 26.24 to 30.24 Volts (6 Volts above the maximum voltage of panels' outputs). The red line indicates the maximum voltage transfer ratio is 100%, which is also the maximum ratio for a practical buck converter.

Based on the observation in figure 20, a practical operation area for a DC bus voltage and the min/max voltage transfer ratio should be below the red line. For

instance, if the min voltage transfer ratio is set to be 45%, the DC bus voltage should no less than 26.84 Volts, as illustrated in point A. Therefore, when the DC bus voltage is set to be 28 Volts, almost there is no limitation in terms of max or min voltage transfer ratio.

From equation (15) and (16), certain constrains are also necessary to calculate the frontend voltage, as given by equations (20) and (21).

$$(R_{BR})_{max} = \frac{V_{DC}-(V_{PV})_{min}}{V_{FD}} = \frac{28-20.97}{V_{FD}} \leq 100\% \quad (20)$$

$$(R_{BR})_{max} = \frac{V_{DC}-(V_{PV})_{min}}{V_{FD}} = \frac{28-24.24}{V_{FD}} \geq 20\% \quad (21)$$

Combination of (20) and (21) yields $7.03\text{Volts} \leq \text{V}_{\text{FD}} \leq 18.8\text{V}olts$,

Thus, the frontend voltage is set to be V_{FD} =10 Volts, so the max voltage transfer ratio is:

$$(R_{BR})_{max} = \frac{V_{DC}-(V_{PV})_{min}}{V_{FD}} = \frac{28-20.97}{10} = 70.3\% \quad (22)$$

The min voltage transfer ratio is:

$$(R_{BR})_{min} = \frac{V_{DC}-(V_{PV})_{max}}{V_{FD}} = \frac{28-24.24}{10} = 37.6\% \quad (23)$$

Voltage, current and power for each PV balancer, the frontend converter are listed in table 3 below, values for conventional MICs can be observed from table 2 :

		Input Voltage	Output Voltage	Output Current	Output Power
Buck Converters in Architecture II	**1**	10V	7.03V	0.35A	2.48W
	2	10V	5.63V	0.70A	3.96W
	3	10V	3.77V	1.83A	6.89W
Frontend Flyback in Architecture II		28V	10V	1.33A	13.32W
Conventional MIC	**1**	20.97	N/A	0.35	7.34
	2	22.38	N/A	0.70	15.67
	3	24.24	N/A	1.83	44.36

Table 3 Voltage, current and power for each PV balancer and frontend converter

As a summary for architecture II design, the DC bus and the frontend output voltage are set to be 28 Volts and 10 Volts respectively. One flyback, which is rating $6.89 \times 3 = 19.14$ Watts acts as the frontend converter and three Buck, each of which is rating at 6.89 Watts which are only about 15% as that of a conventional MIC are required here as PV balancers. The use efficiency for a single PV balancer and the frontend converter are greater than $\frac{13.32}{19.14} \times 100\% = 69.6\%$ and $\frac{2.48}{6.89} \times 100\% = 36.0\%$ respectively.

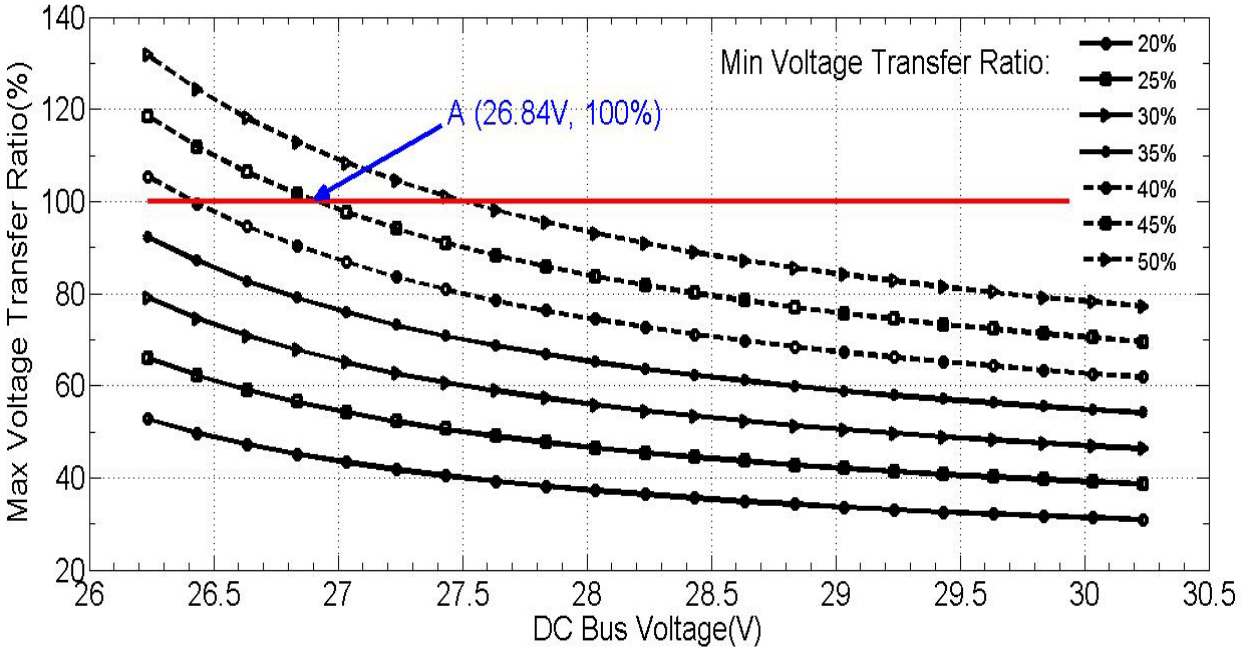


Figure 20 Max Voltage Transfer Ratio for PV Balancer vs. DC Bus Voltage

Codes used for figure 16 to 20 in Matlab can be seen from Appendix 4.

Simulation Results

The DC Bus is modeled as a constant voltage source in Matlab/Simulink, for a real design, this voltage can be derived from the utility grid via an AC/DC transformer.

Architecture I Simulation Result

The systematic diagram in Matlab/Simulink is sketched in Appendix 5.

Figure 21 shows the module output voltages and currents in Architecture I, and Figure 22 shows the PV balancer output voltages (= DC bus voltage minus panel output voltages).

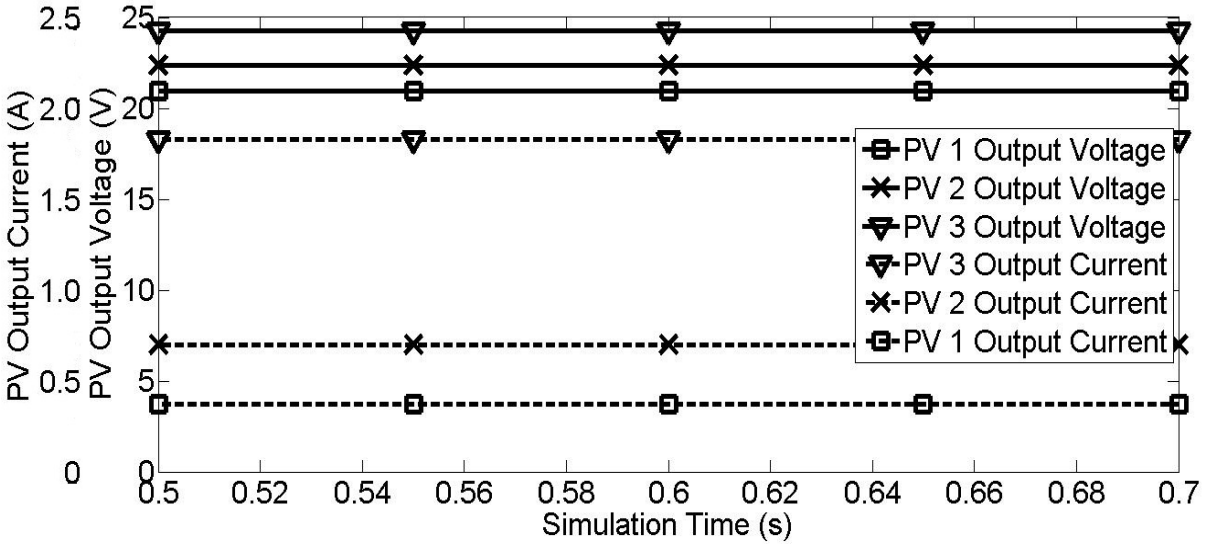


Figure 21 Module Output Voltages and Currents in Architecture I

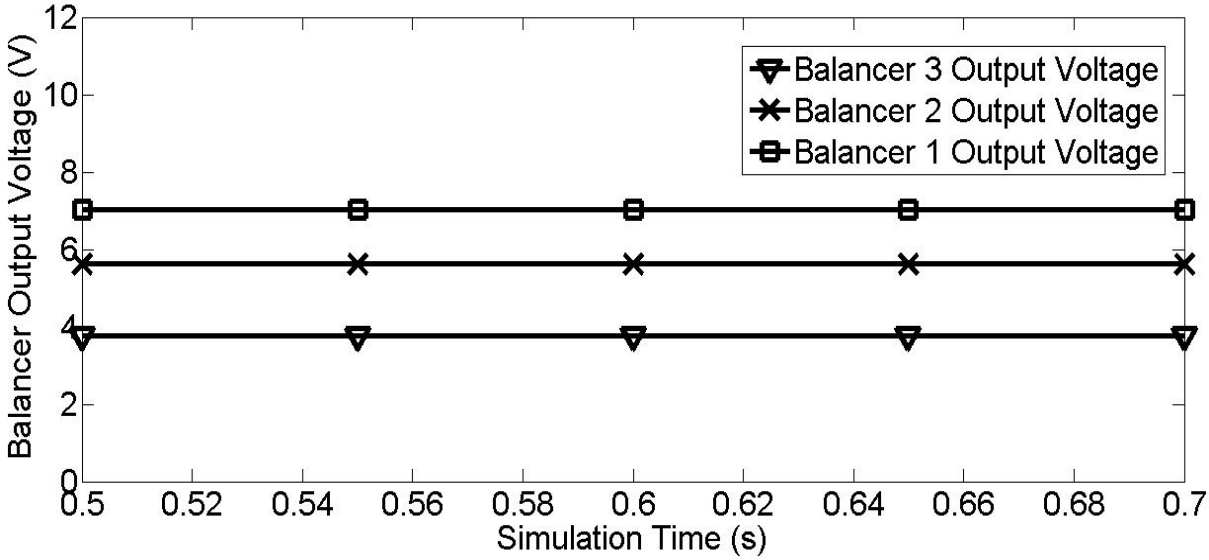


Figure 22 PV balancer Output Voltages in Architecture I

Architecture II Simulation Result

The systematic diagram in Matlab/Simulink is sketched in Appendix 6.

Fig. 22 shows the panel output voltages and currents in Architecture II and Fig. 23 shows the PV balancer and the frontend converter output voltages.

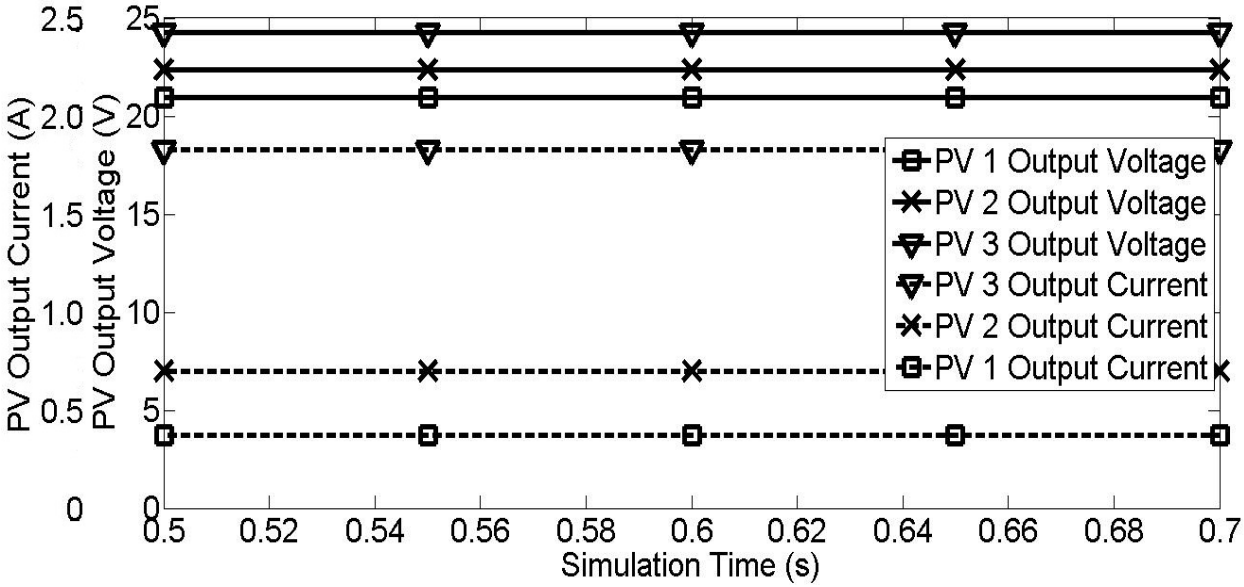


Figure 23 Module Output Voltages and Currents in Architecture II

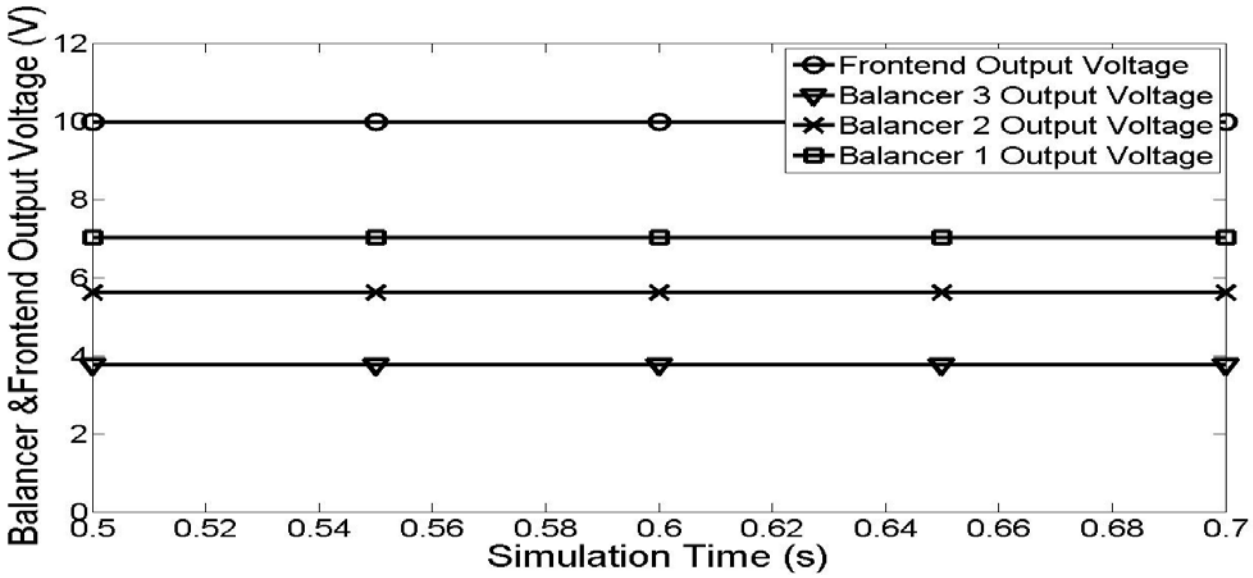
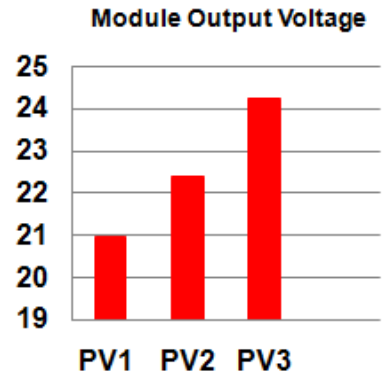


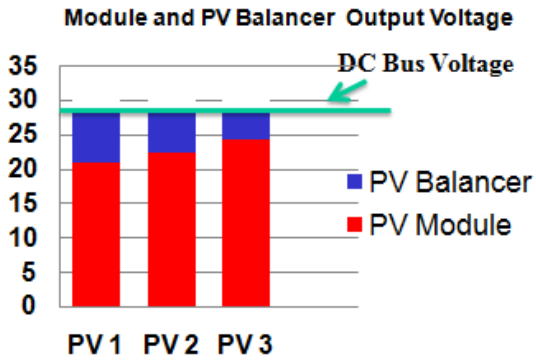
Figure 24 PV balancer Output Voltages in Architecture II

Analysis of Simulation Results

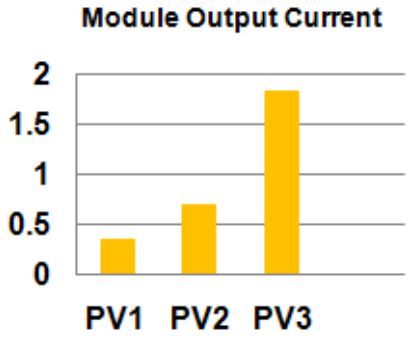
These simulation results are better illustrated in Fig. 25. It shows that the output currents of PV balancers are equal to the output currents of corresponding PV modules and the output voltages of PV balancers compensate the difference between the DC bus voltage and PV module voltages.



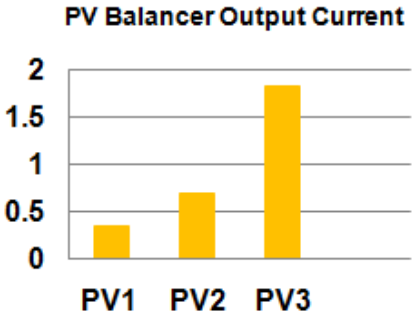
(a) Output voltages of PV modules



(b) Output voltages of PV balancers



(c) Output currents of PV modules



(d) Output currents of PV modules

Figure 25. Simulation results of PV modules and PV balancers

Observed from the simulation results, this new concept has been verified at software level. Compared to conventional PV converter scenario---three 24.24 Volts × 1.83 Amps = 44.36 Watts Converters directly connected with PV modules---the new concept is a lower power rating solution---only plug in three 6.89 Watts Flyback in Architecture I, and one 20.67 Watts Flyback and three 6.89 Watts in Architecture II.

Chapter 4 Hardware Verification

This chapter presents the hardware verification for both architectures proposed in the previous chapter. This includes hardware realization of the PV panels, hardware design for the PV balancers and frontend converter. At the end of this chapter, the control logic and future optimization for the special buck converter will be discussed. Altium Designer has been applied as the Printed Circuit Board (PCB) layout tool for the PV balancers design.

Hardware Realization and Design

Hardware realization for the PV Module

Observed from figure 2 and 3, PV panel performs more like a current source, thus, three current sources (Mastech Linear Power Supply 50V 5A HY5005D-2 Dual Outputs, figure 26) have been chosen acting as the PV Module.

Figure 26 Mastech DC Power Supply HY5005D-2 [20]

Hardware Design for PV Balancer in Architecture I and Frontend Converter in Architecture II

Since PV balancers in architecture I and Frontend Converter in architecture II are essentially Flyback Converters and have already been standard products in manufacturing, comprehensive design procedure will not be listed in this work.

Specifications of these Flyback converters have been enumerated in table 2 and table 3. Figure 27 presents the prototypes of these converters.

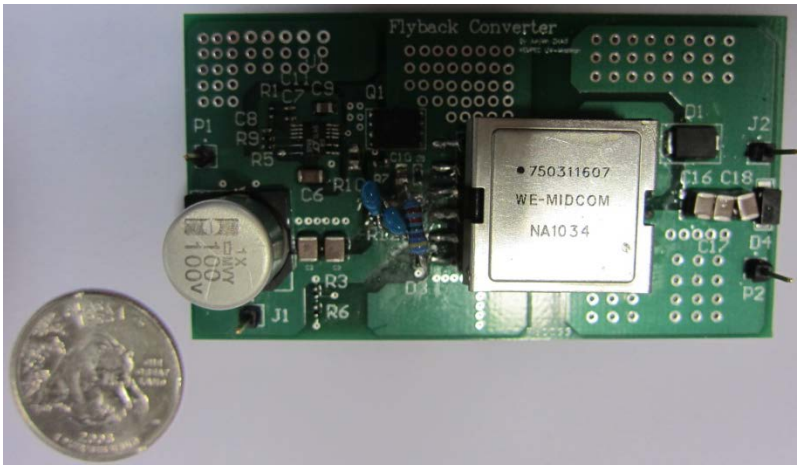


Figure 27 Prototype of PV balancers in Architecture I and Frontend Converter in Architecture II

Hardware Design for the PV Balancer in Architecture II

Based on the analysis of the Buck Converters for architecture II in last chapter, special concerns, such as positive common grounding and control algorithm, have been considered as the key point for this design.

Figure 28 shows the basic block diagram for these buck converters.

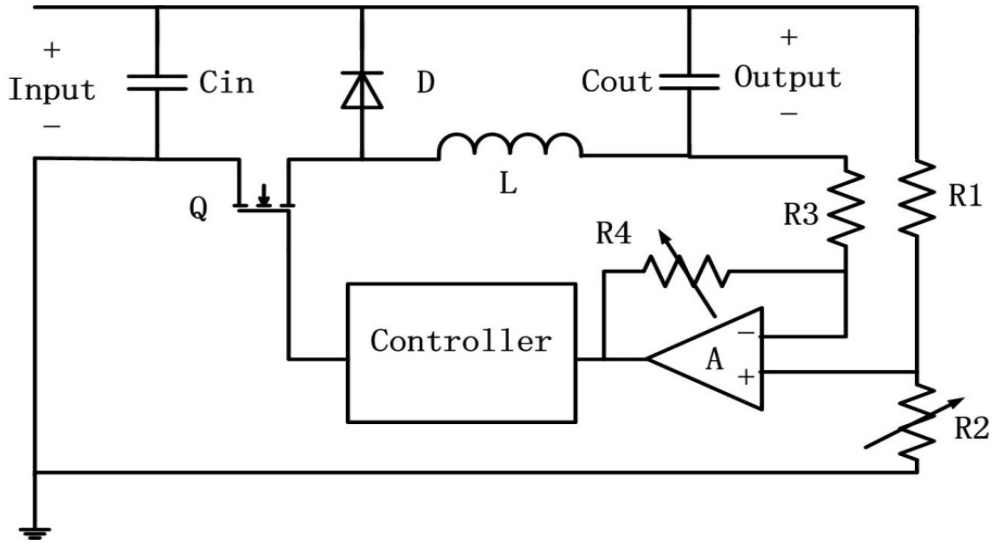


Figure 28 Buck Converter Design in Architecture II

The basic power circuit in figure 28 is the same as that shown in figure 14, however, the control circuit is much different from a traditional buck converter: A subtracter, composed of a comparator and four resistors, has monitored the output voltage of the power converter. Torex Semiconductor XC9101 controller uses the output result from the subtracter as the input signal and feeds the gate signal to the Mosfet. Part of the XC 9101 data sheet has been illustrated in Appendix 7.

The full version of PCB schematic in Altium Designer is then given in Appendix 8.

Figure 29 presents the prototypes of PV balancers in Architecture II.

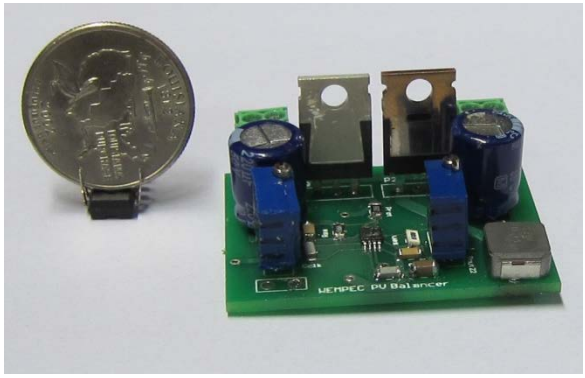


Figure 29 Prototype of PV balancers in Architecture II

Hardware Results

Figure 29 shows the output voltages of PV balancers in Architecture I. Figure 30 shows the output voltages of PV balancers in Architecture II. These experimental results are identical to simulation results.

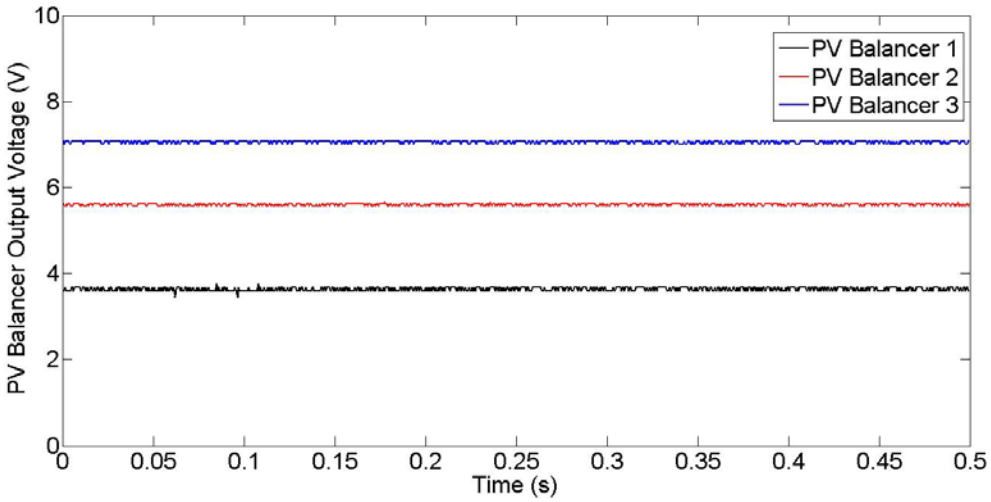


Figure 30. Output voltages of PV balancers in Architecture I

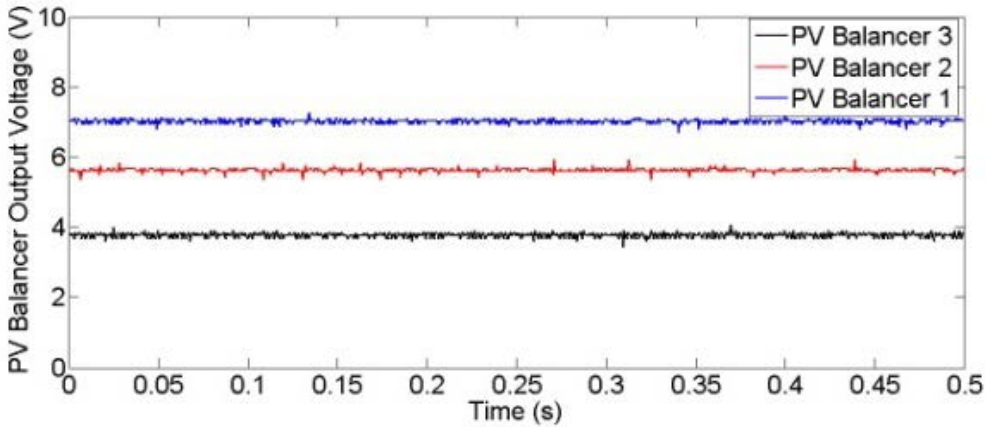


Figure 31. Output voltages of PV balancers in Architecture II

The efficiency of PV balancers are approximately 75%~ 85% depending on the output voltages. The equivalent efficiency of PV balancers η_E is about 96% calculated by (12). The purpose of this paper is to demonstrate the concept of PV balancers and maximizing power density and efficiency was not a focus in our first-pass design. Diode rectifiers and transformers without optimization may jeopardize the efficiency. Nevertheless, the efficiency of this first prototype is low compared to many commercial DC-DC converters with similar specifications and an efficiency of more than 90% (which will achieve an equivalent efficiency of 98%). High efficiency DC-DC converters optimized for the PV balancer concept will be developed in the future.

Chapter 5 Conclusion

Both architectures have been verified applicable at the software and experimental level, this chapter will give a thoroughly investigation of the merits, short comings and a comparison between these two architectures for the PV balancer. Moreover, in order to achieve the final goal as minimizing the total set up and maintenance rate of the PV application as well as a reliable source to the utility grid, a proposal for future work will be followed by the end of the session.

Merits of the PV Balancer

The power rating and power loss of a PV balancer are much smaller than its counterparts, traditional MICs. For instance, if the maximum power that a module can produce is 100W, the DC-DC converters in for the traditional MIC should deliver the same maximum power (=100W). Considering a PV balancer which compensates up to 20% of the module output voltage, the PV balancer thus delivers up to 100W×20%=20W maximum output power, which is only 1/20 the power of its counterparts. Assuming both the PV balancer and the traditional MICs can achieve 90% efficiency, the maximum power loss of the PV balancer is up to 2W, which represents 2% of the maximum output power. In comparison, the maximum power loss of the traditional MIC is up to 10W, which represents 10% of the maximum output power. Table 4 summarizes a comparison of power rating and efficiency of the traditional MIC and the PV balancer. Since the size, cost, loss and other performance aspects of a DC-DC converter is roughly inversely proportional to its power rating, PV balancers will have clear economic advantages over the conventional technology.

	PV Balancer	Traditional MIC
Power Rating	20W	100W
Power Loss	2W	10W
Equivalent Efficiency η_E	98%	90%

Table 4 Comparison of Traditional MIC and PV Blancer

PV balancers also achieve an excellent inherent fault tolerance and high reliability. For instance, if a PV module fails, the PV balancer connected to it will disconnect the PV module from the DC bus as shown in Fig. 7 and there is no adverse influence over other modules. If a PV balancer fails, the output of the PV balancer will be shorted and the PV module connected to it will be reconnected to the DC bus as shown in Figure 32. The PV module can still generate some power though the PV module may not operate at its maximum power point.

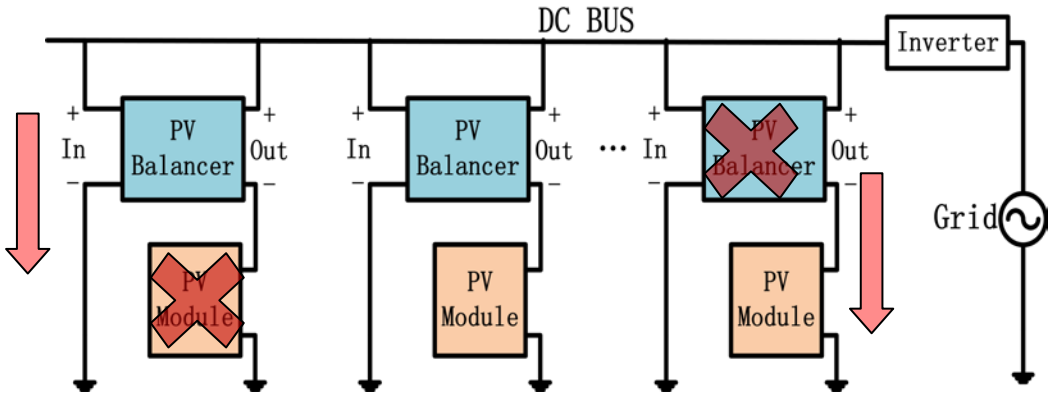


Figure 32 Inherent fault tolerance and high reliability of PV balancers

PV balancers may simplify the requirement of energy buffering of a single-phase inverter. In a single-phase inverter system, there is an instantaneous unbalance between the input dc power and the output ac power [1] [22] [23]. An energy buffer is needed to provide reactive power varying at twice the line frequency. Bulky electrolytic capacitors could be used at the inverter input in parallel with PV modules to provide necessary energy buffering however it will jeopardize the MMPTs of PV modules

because of the ripples on the capacitors. Besides, bulky electrolytic capacitors are not preferred in photovoltaic applications because of their low reliability. “Third-port” topologies, which provide the energy storage buffering within the converter, have been widely investigated [22][23]. High reliability and small size film capacitors are used in these topologies. However, these topologies need extra switching devices and passive components to realize energy buffering and power circuit as well as control become complicated. For PV balancers, however, we could use the input capacitors of the inverter as the energy buffer and let the dc bus voltage containing a ripple at twice the line frequency. As the inverter input is not connected directly to PV modules, there is no coupling between the energy buffer and the MPPTs of PV modules. This approach may simply the design of energy buffering in a single-phase system and may be investigated later in our future work.

Shortcomings of the PV Balancer

Though PV balancer has advantages mentioned above, it is deniable that there are several disadvantages associated risks need to be solved or improved for a bright prospect.

One of disadvantages of PV balancers is that it requires a high voltage transformation ratio at the inverter stage. The new transformation ratio is the same as that of a micro-inverter [4][22][23]. Since micro-inverters have been proved to be highly efficient (>96.5%) and feasible in many studies, this disadvantage is not a fatal flaw of the PV balancer concept.

Moreover, the approach presented in this paper may overcome the primary disadvantages of micro-inverters, e.g., that micro-inverters have a higher equipment

initial cost than a centralized converter, because in this new concept, the number of inverters is reduced and so is ac wiring. Nevertheless, an inverter especially designed for PV balancers will be developed in the future, but that is not within the scope of this paper.

Compared to DC-DC converters in Figure 7, PV balancers may need a larger voltage transformation ratio of the input and the output which may reduce the efficiency of PV balancers and increase their cost and size. Highly efficient DC-DC converters for the purpose of PV balancers need to be further studied.

Compared to micro-inverters in Figure 8, PV balancers may suffer extra power loss due to low-voltage dc bus. We may estimate the loss as the following. Assuming the output power of a PV module is 100W and the output dc current is 5A. If the dc cable is made by the AWG wire size of 5, which has a diameter of 5mm and a dc resistance of 1.0mΩ/m, the power loss on the cable is 0.025W/m, which is about 0.025% efficiency loss. The loss is insignificant when the number of PV modules is small and the DC bus is short but it may be significant when the number of modules is large and the DC bus is long. Micro-inverters in Figure 33 mitigate this problem because the output power of PV modules are combined at the AC line which has a higher voltage and less current than the low-voltage DC bus of PV balancers. The DC bus loss could be reduced with a larger gauge of copper wire, but it will incur extra cost of copper. In high power photovoltaic applications with a large number of PV modules, the PV balancers could be integrated on PV strings instead of on PV modules as shown in Figure 33. This approach will enable an independent MMPT on each string, minimize the dc bus loss and reduce the transformation ratio of the inverter stage.

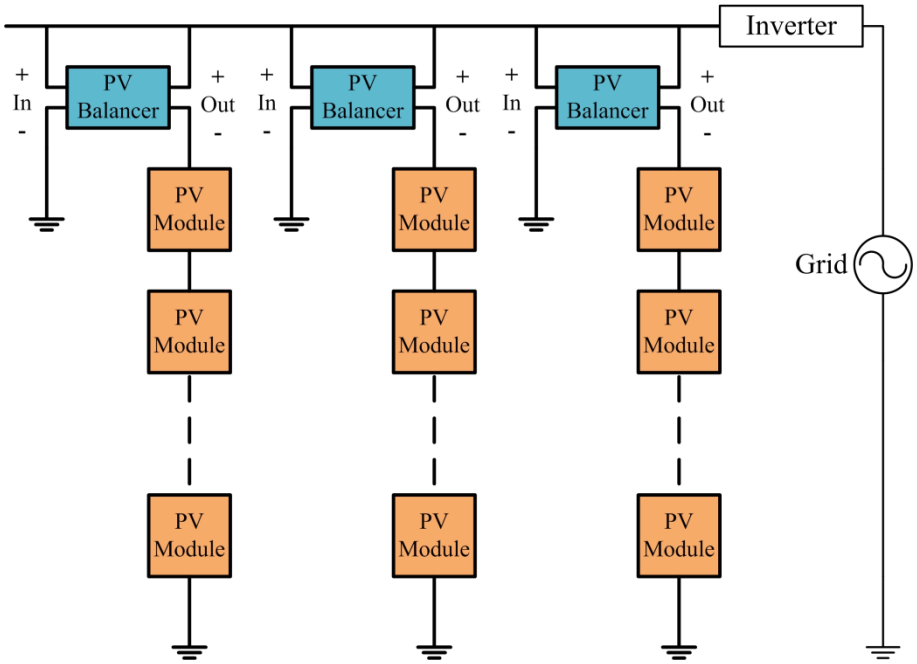


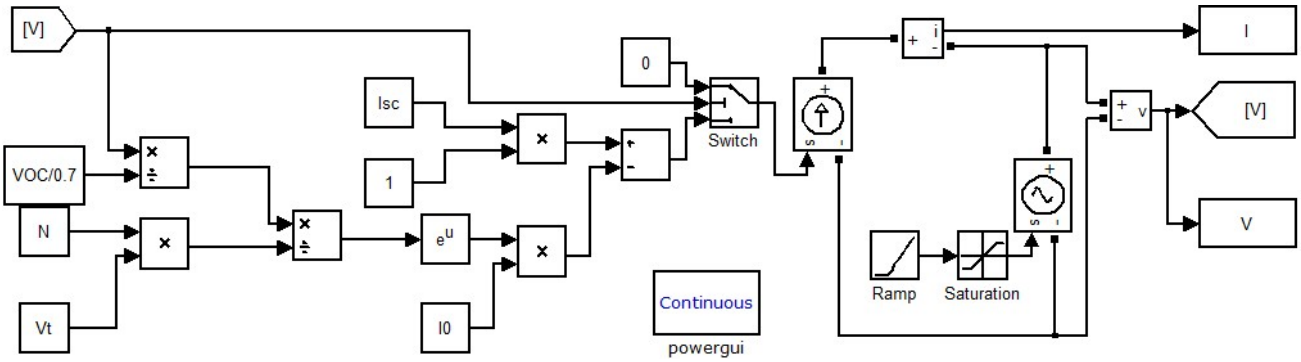
Figure 33 PV balancers applied to series strings of PV modules

Future work for PV Balancer

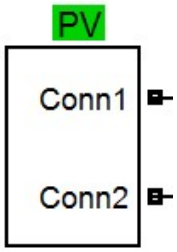
A new concept of module-integrated converters called PV balancers has been proposed and verified in this thesis. The proposed concept enables independent maximum power point tracking (MPPT) for each module, and dramatically decreases the requirements for power converters. PV balancers may have a significant economic value for photovoltaic systems in the future.

Future work will be focused on power converter optimization, dc bus voltage control, and developing a highly efficient inverter for PV balancers.

Appendix 1

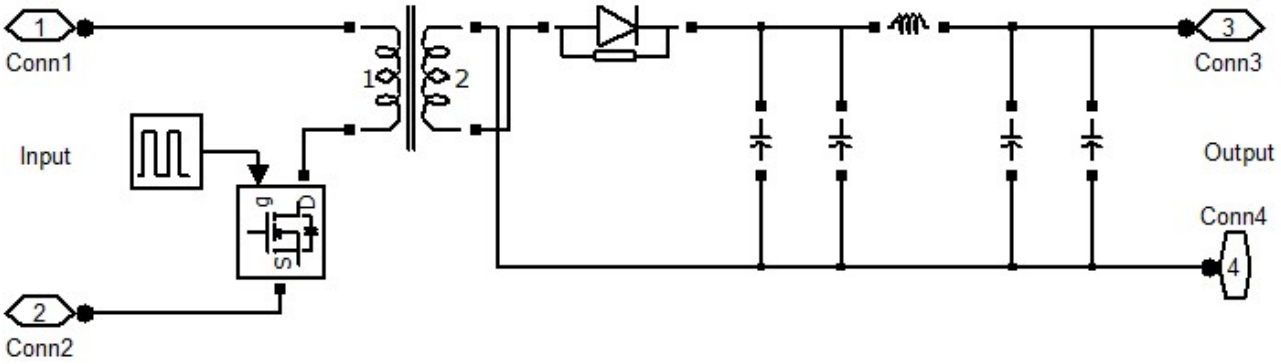


PV Module Modeling in Matlab/Simulink

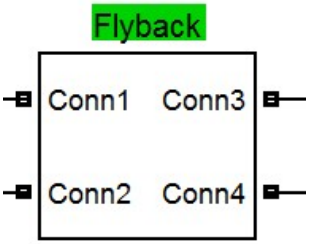


PV Module Subsystem in Matlab/Simulink

Appendix 2

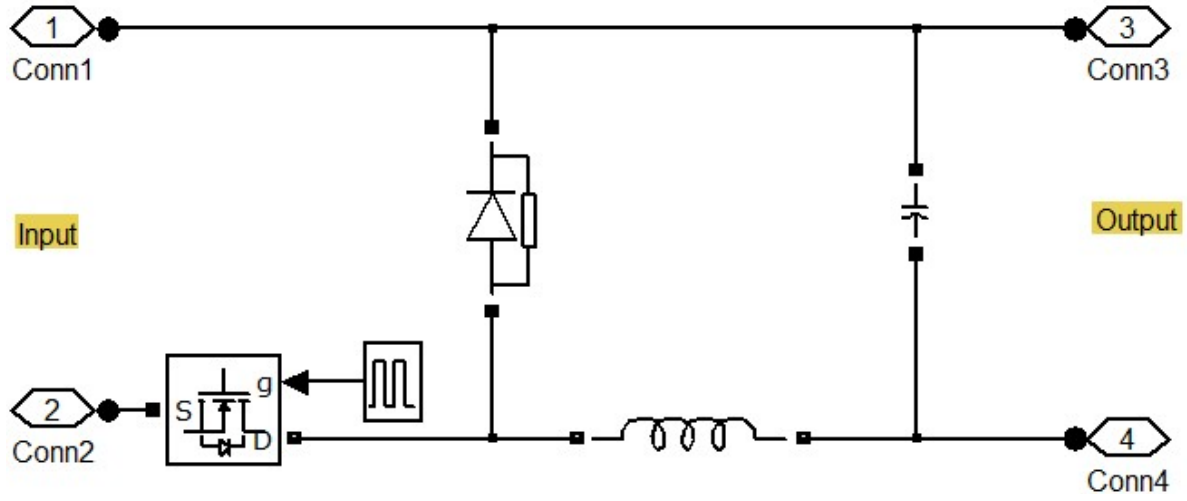


PV balancer (Flyback Converter) Modeling in Matlab/Simulink for Architecture I

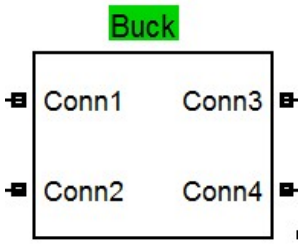


PV balancer (Flyback Converter) Subsystem in Matlab/Simulink for Architecture I

Appendix 3



PV balancer (Buck Converter) Modeling in Matlab/Simulink for Architecture II



PV balancer (Buck Converter) Subsystem in Matlab/Simulink for Architecture II

Appendix 4

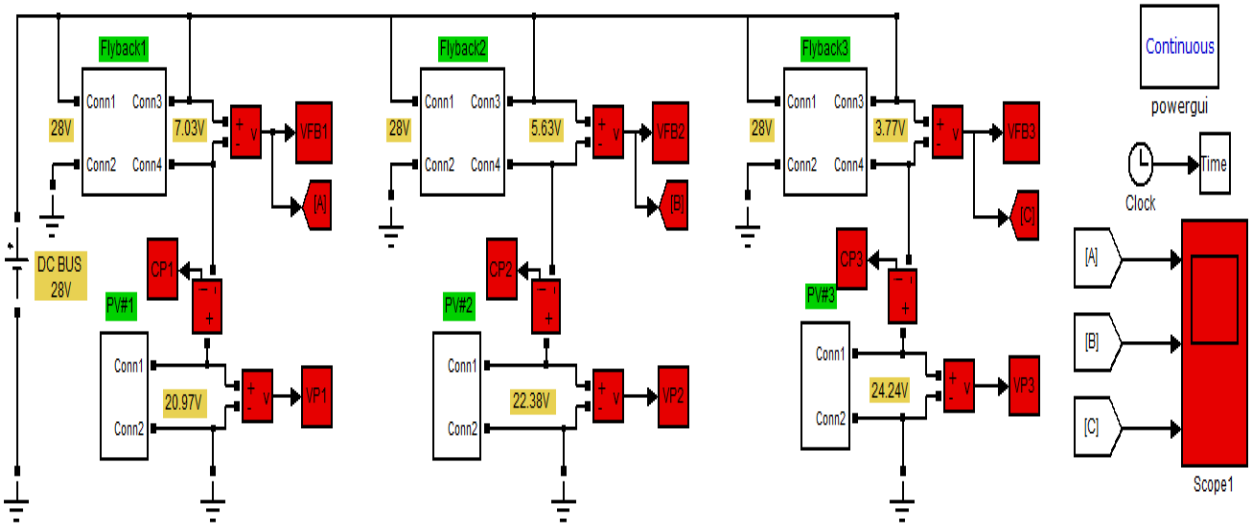
```
%%%%%%%%%%l%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%Three PV Modules Modeling%
Isc=[0.375 0.75 1.95]; %Short-circuit Current
VOC=[24.8 26.47 28.67];%Open-Circuit Voltage
Voc=0.7;
q=1.6e-19;
k=1.38e-23;
T=300;
Vt=k*T/q;
N=1.5;
I0=Isc*exp(-Voc/N/Vt);
for n=1:3;
```

```
    V(n,:)=0:1e-3:30;
    n=n+1;
end;
for n=1:3;
    for m=1:30001;
        if V(n,m)>=VOC(n);
           I(n,m)=0;
        else
           I(n,m)=Isc(n)-exp(V(n,m)/(VOC(n)/Voc)/(N*Vt))*I0(n);
        end;
        m=m+1;
    end;
n=n+1;
end;
for n=1:3;
    P(n,:)=V(n,:).*I(n,:);
    [a b]=max(P(n,:));
    Vmpp(n)=V(n,b);
    Impp(n)=I(n,b);
    n=n+1;
end;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%PV Panel I-V Characteristics%
figure(1);
for n=1:3
    plot(V(n,:),I(n,:),'g');
    hold on;
    plot(Vmpp(n),Impp(n),'rx');
    n=n+1;
end;
xlabel('Output Voltage (V)');
ylabel('Output Current (A)');

%PV Panel P-V Characteristics%
figure(2);
for n=1:3;
    plot(V(n,:),P(n,:));
    hold on;
    n=n+1;
end;
xlabel('Output Voltage (V)');
ylabel('Output Power (W)');

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
Vstep=0:0.2:6;
for n=1:31;
```

```
    Vopt=Vmpp(3)+Vstep(n)-Vmpp;
    Popt(n,:)=Vopt.*Impp;
    %Use Efficiency of the Balancer%
    effi(n)=min(Popt(n,:))/max(Popt(n,:))*100;
    %Architecure II,Min Duty Cycle is Determined by Balancer
with max Vmppt%
   duty_PVbalancer_max(n)=(max(Vmpp)-min(Vmpp)+(n-1)*0.2)/((n-…
    …-…1)*0.2*(1/0.5))*100;
    %(1/0.5) Can Be Changed for Value:
(1/4.5),(1/4),(1/3.5),(1/3),(1/2.5)
    n=n+1;
end;
%DC Bus Voltage%
Vstep=Vstep+Vmpp(3);

%Power for Each Balancer under Different DC Bus Voltage%
figure(3)
for n=1:31;
    plot(Popt(n,:),'g')
    plot(Popt(n,:),'rx');
    hold on;
    n=n+1;
end
xlabel('Num of Converter');
ylabel('Power Go Though Converter (W)');

%Max and Min Power Go Through Each Balancer%
figure(4)
for n=1:31
    Popt_31max(n)=max(Popt(n,:));
    Popt_31min(n)=min(Popt(n,:));
    n=n+1;
end;
plot(Vstep,Popt_31min);
hold on;
plot(Vstep,Popt_31max);
xlabel('DC Bus Voltage');
ylabel('Max/Min Power Go Though Converter (P)');

%Use Efficiency for Balancer for Different DC Bus Voltage%
figure(5)
plot(Vstep,effi);
xlabel('DC Bus Voltage');
ylabel('Use Efficiency (%)')

%Max Voltage Transfer Ratio For Different Balancer%
figure(6);
```

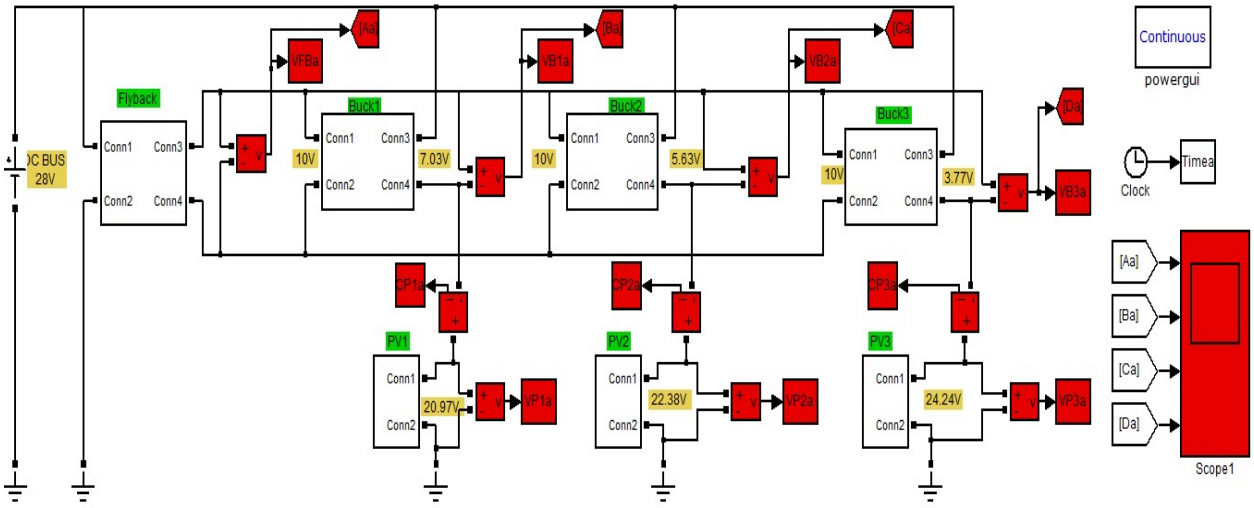
```
plot(Vstep(11:31),duty_PVbalancer_max(11:31));
hold on;
xlabel('DC Bus Voltage(V)');
Ylabel('Max Voltage Transfer Ratio for PV Balancer (%)');
```

Appendix 5



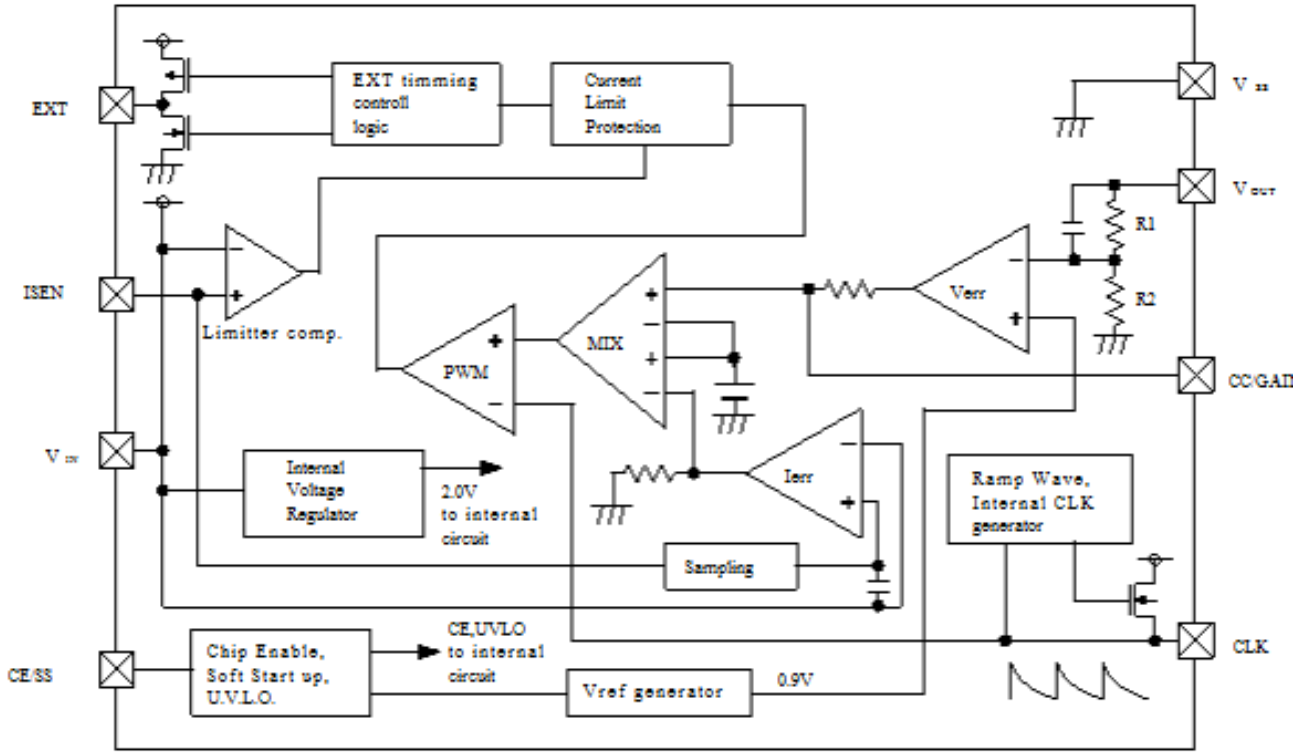
Systematic Diagram for Architecture I in Matlab/Simulink

Appendix 6



Systematic Diagram for Architecture II in Matlab/Simulink

Appendix 7



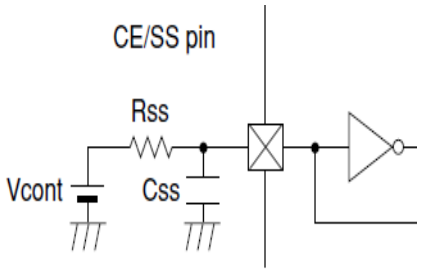
Block Diagram of XC9101 Series

PIN NUMBER	PIN NAME	FUNCTION
1	EXT	Driver
2	Isen	Current Sense
3	VIN	Power Input
4	CE／SS	CE/Soft Start
5	CLK	Clock Input
6	CC／GAIN	Phase Compensation
7	VOUT／FB	Voltage Sense
8	VSS	Ground

Pin Assignment

1. Soft Start:

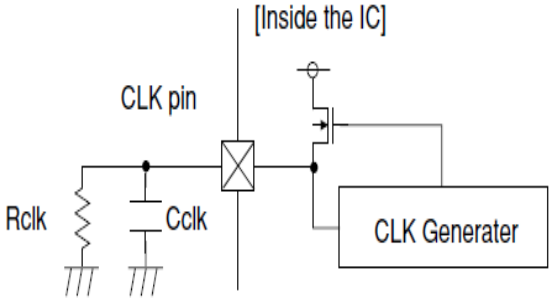
CE and soft start (SS) functions are commonly assigned to the CE/SS pin. Soft start time is approximated by the equation below according to values of Vcont, Rss, and Css.



$$T = -C_{SS} \times R_{SS} \times \ln \frac{V_{cont} - 1.55}{V_{cont}}$$

2. Oscillation Frequency:

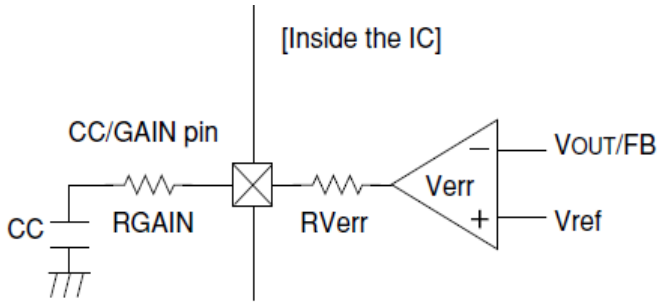
The oscillation frequency of the internal clock generator is approximated by the following equation. To stablize the IC's operation, set the oscillation frequency within a range of 100kHz to 600kHz. Select a value for Cclk within a range of 150pF to 220pF and fix the frequency based on the value for Rclk.



$$T = {}^{1}/_{-C_{clk} \times R_{clk} \times \ln(0.26)}$$

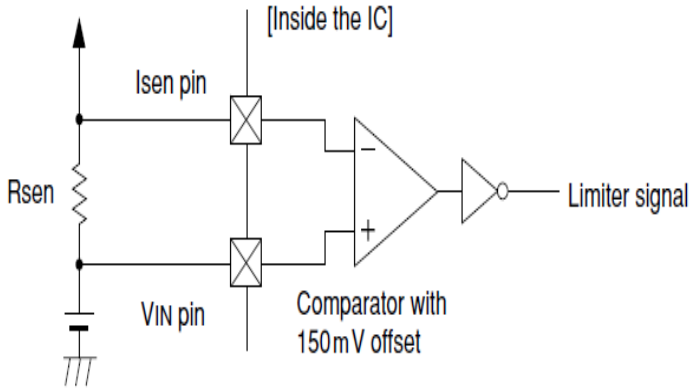
3. Gain and Frequency Characteristics of the Verr Amplifier

The gain at output and frequency characteristics of the Verr amplifier are adjusted by the values of the capacitor and resistor attached to the CC/GAIN pin. It is generally recommended to attach a CC of 220 to 1,000 pF without RGAIN.



4. Current Limit

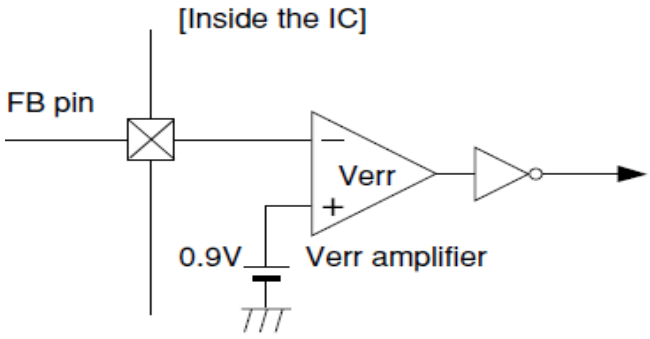
The current limit value is approximated by the following equation according to resistor RSEN inserted between the VIN and Isen pins.



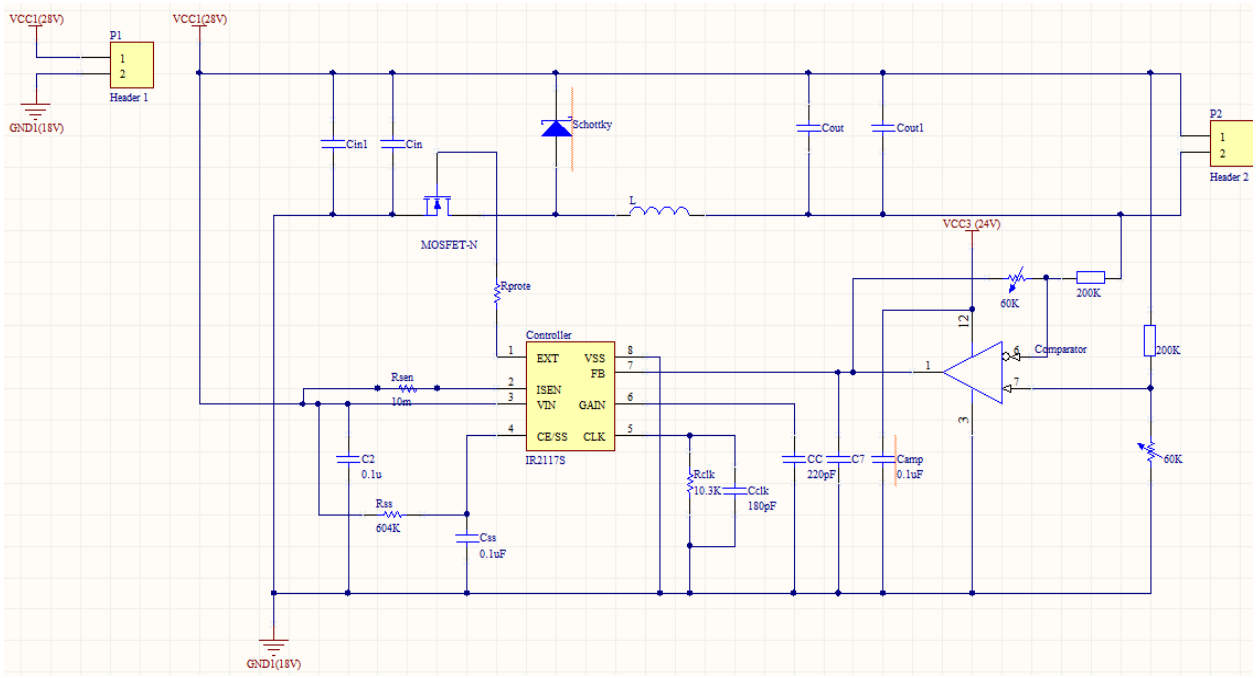
$$I_{peak\_limit} = {}^{0.15}/_{Rsen}$$

5. FB Voltage

The signal value to the feedback pin is desired to be 0.9 Volts based on the internal comparator.



Appendix 8 [17]



PCB Schematics for Buck Converter in Architecture II

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