A 73dB SNDR 20MS/s 1.28mW SAR-TDC Using Hybrid Two-Step Quantization

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Roadmap

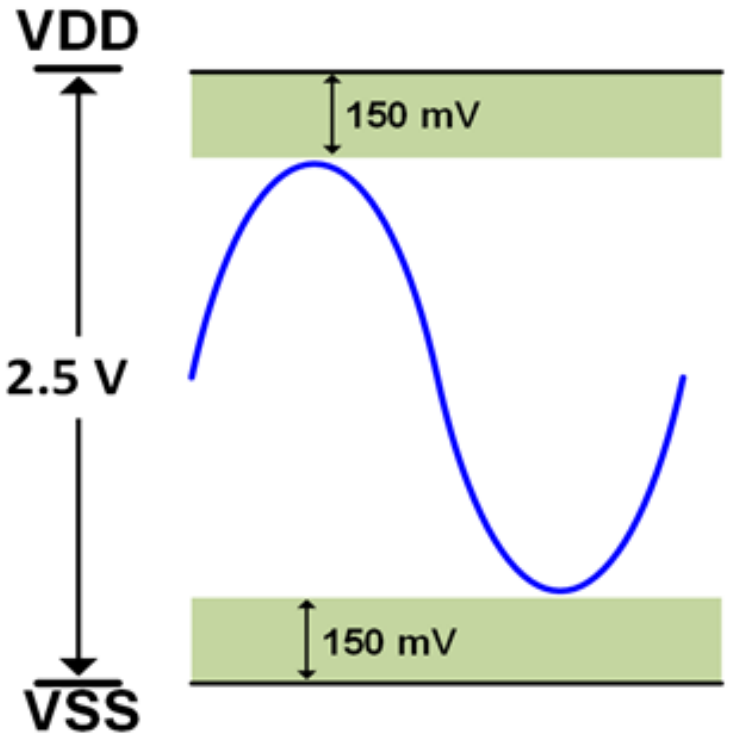
- Research Motivation
- Voltage Domain Solutions
- Proposed Hybrid ADC
- Results and Conclusion

The Internet-of-Things

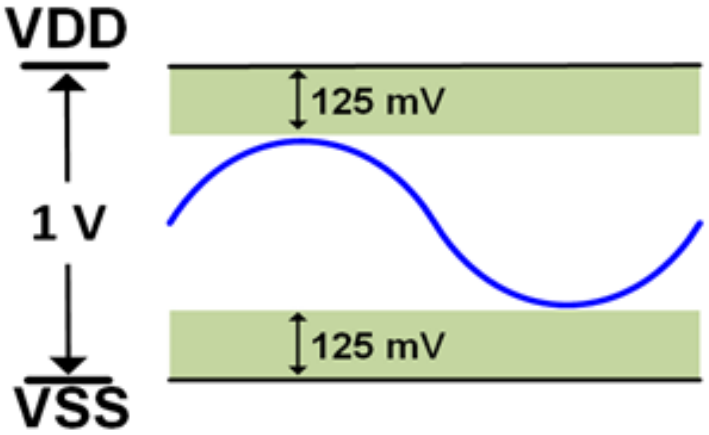



- **Evolution of portable electronics**
  - **WiFi, GPS, Accelerometer, Gyroscope, etc.**
- **Research focus:**
  - **Power efficiency for high resolution**
  - **Develop scaling 'friendly' design techniques**

Supply Voltage Scaling



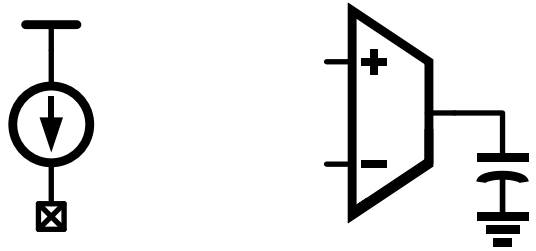
Older Process



Newer Process

- **Scaled CMOS degrades analog efficiency**
  - **V_{DD} ↓ Swing ↓ SNR ↓ C ↑ Power ↑**

CMOS Process Scaling



Digital

- Smaller area
- Faster switching
- Lower Power

Analog

- Noise/Matching limited area
- Intrinsic gain

➢**How can analog design take advantage of digital process scaling?**

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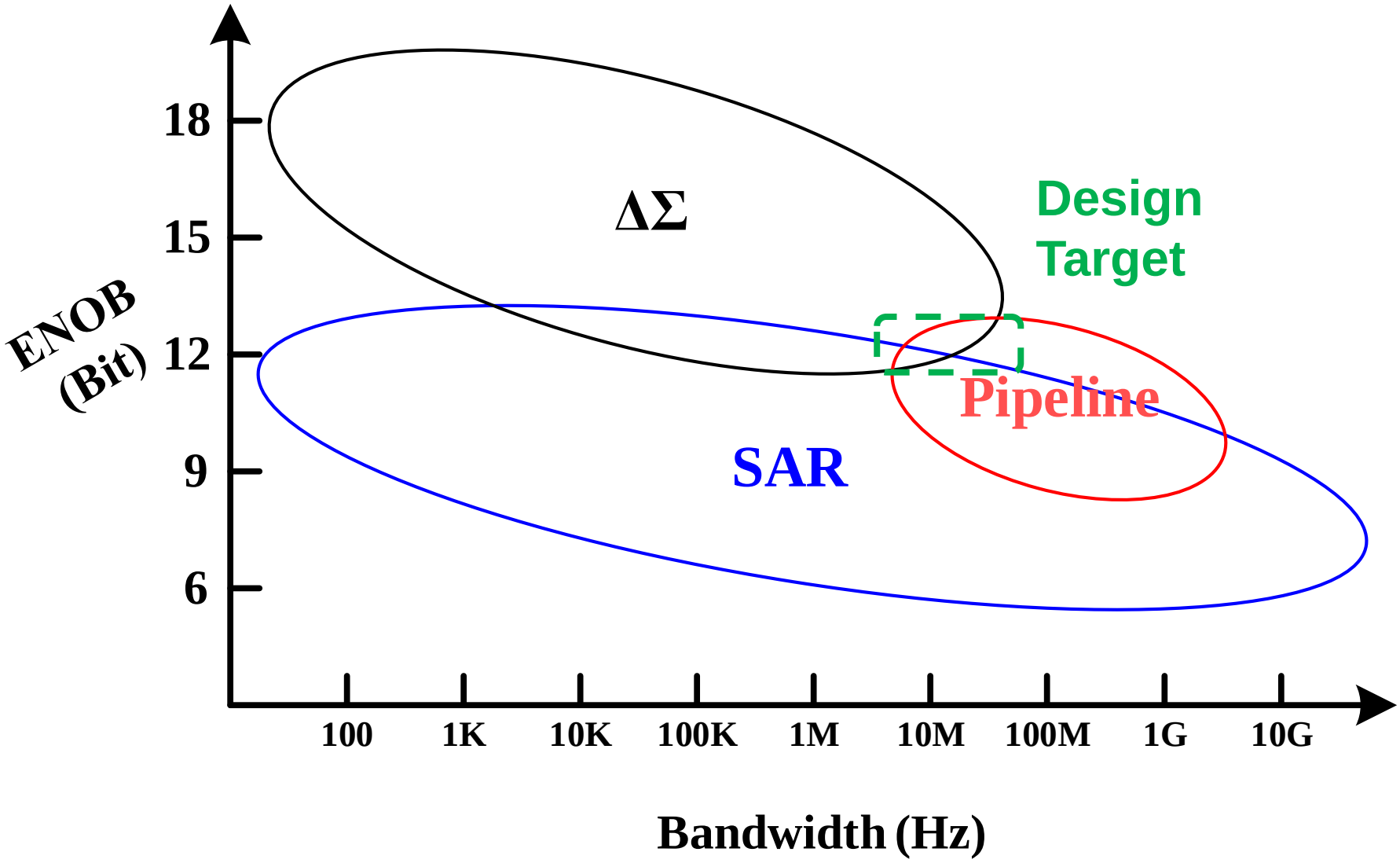
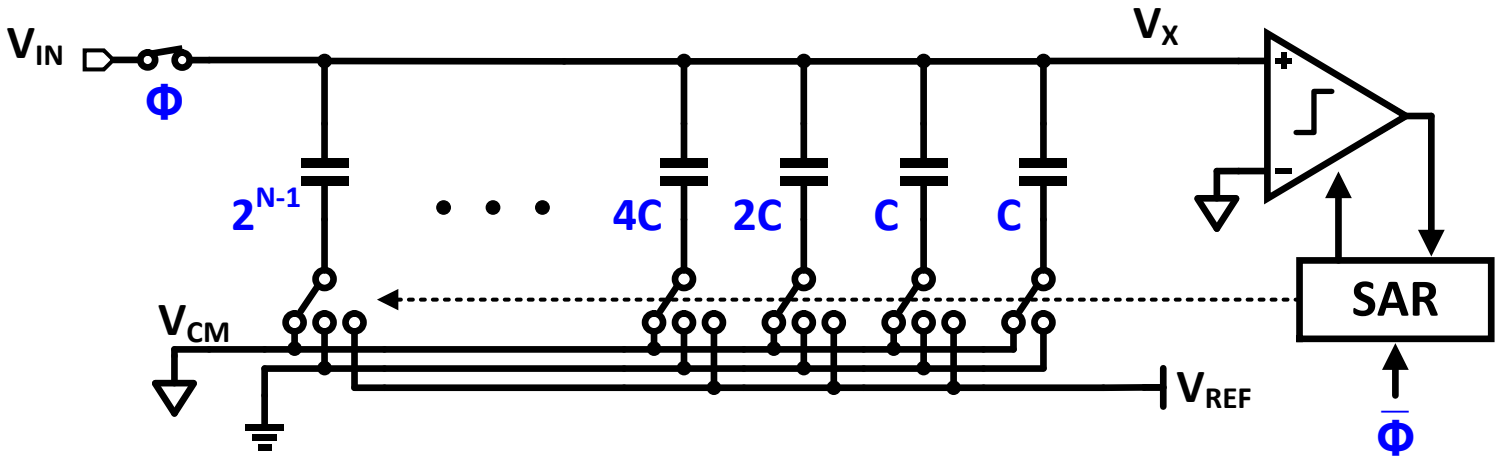
Architecture Selection



Voltage Domain ADCs

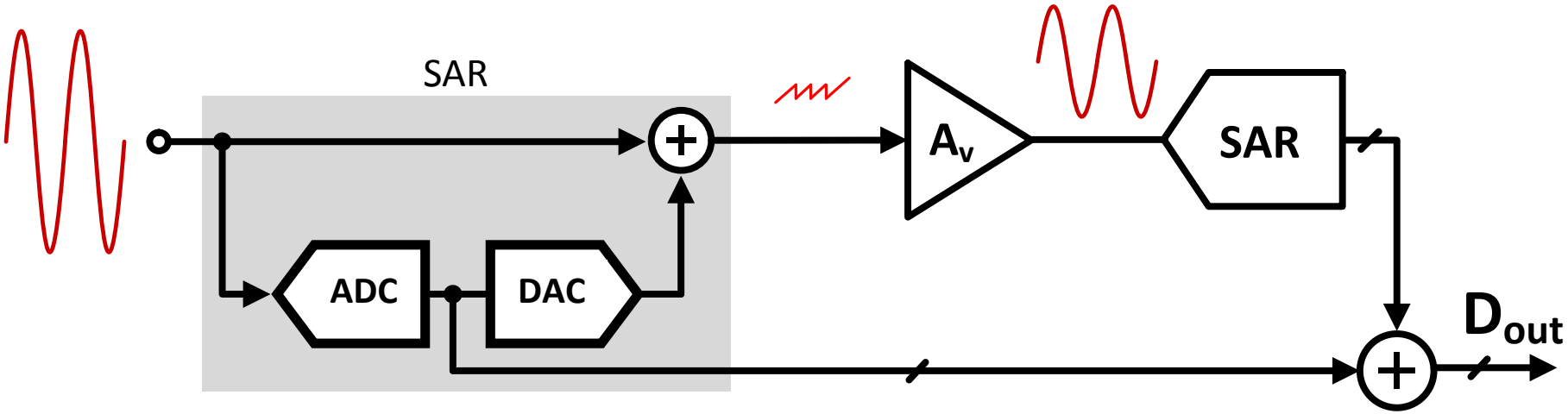
- **Oversampled ΔΣ ADC**
  - **Limited bandwidth**
  - **Integrators in loop filter**
- **Nyquist Pipeline**
  - **Extra power from multiple stages**
  - **Performance residue amplifier**
- **Nyquist SAR**
  - **Simple, highly digital**
  - **Good Scaling Candidate**

SAR Review



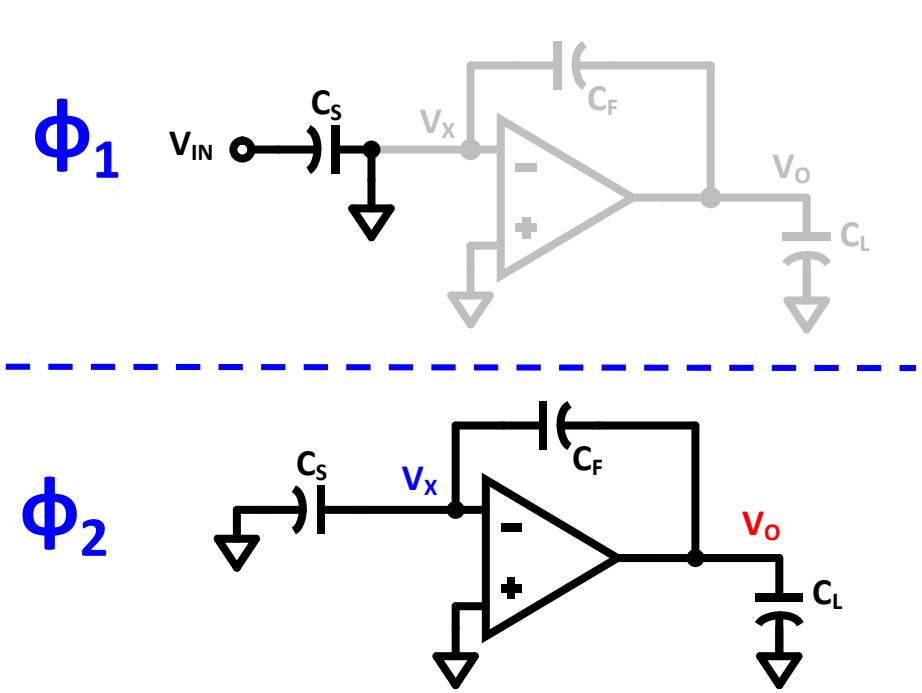
- Residue available after conversion
- Limited in speed and resolution
  - Serial conversion
  - Comparator Noise + DAC complexity

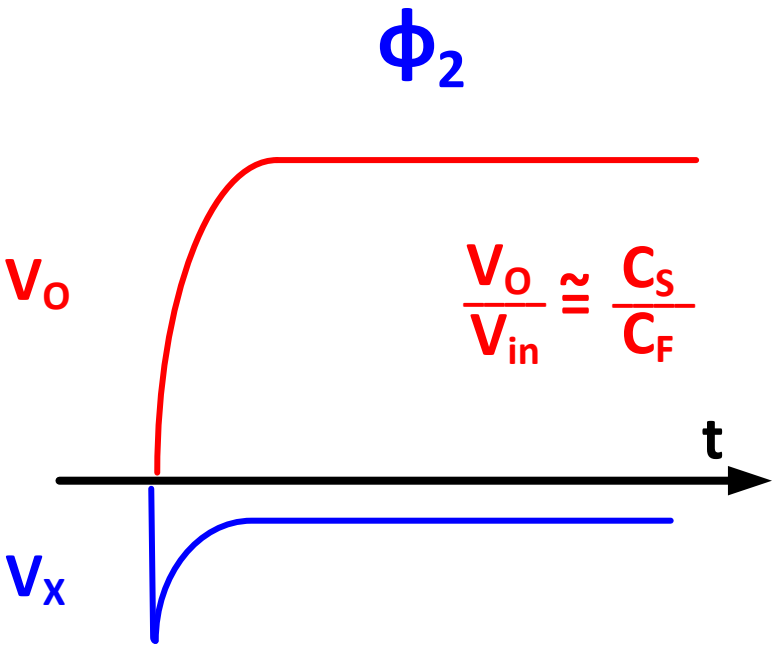
SAR-Assisted Two-Step ADC



- Redundancy → alleviates sub-ADC errors
- Parallel operation → higher speed
- Residue amplifier (A_V) is primary design bottleneck
  - High gain, large swing, wide bandwidth

Voltage Domain Residue Amplifier





- **Two-phase operation**
  - **Transfer charge from C_S to C_F**
  - **Finite gain limits accuracy**
  - **Large capacitive load of second stage**

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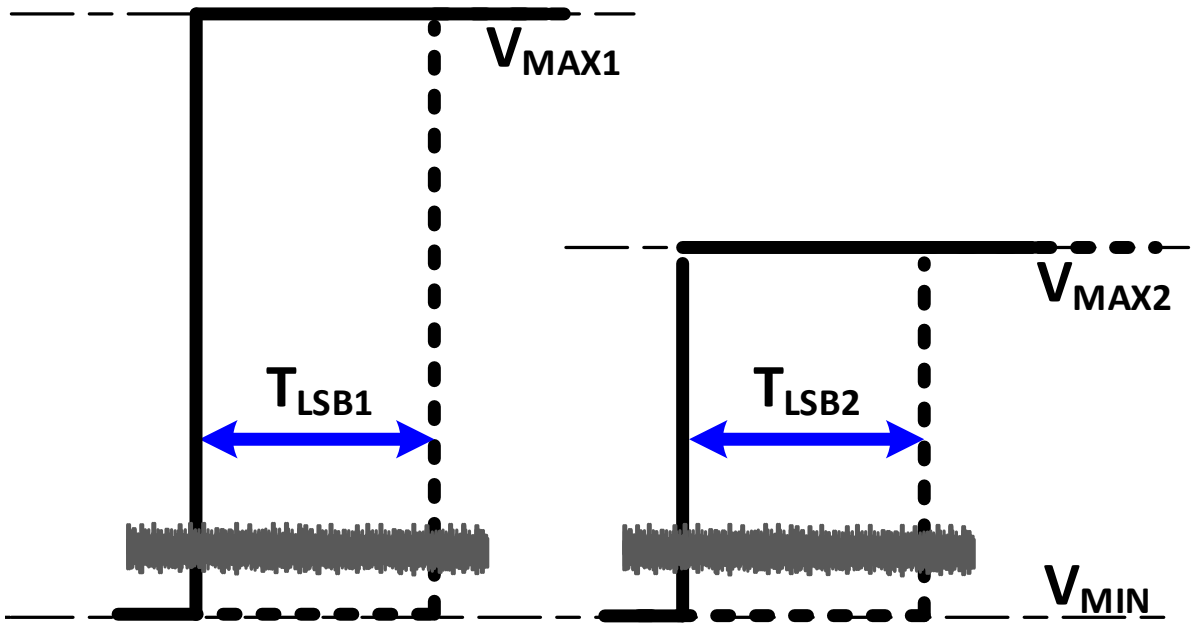
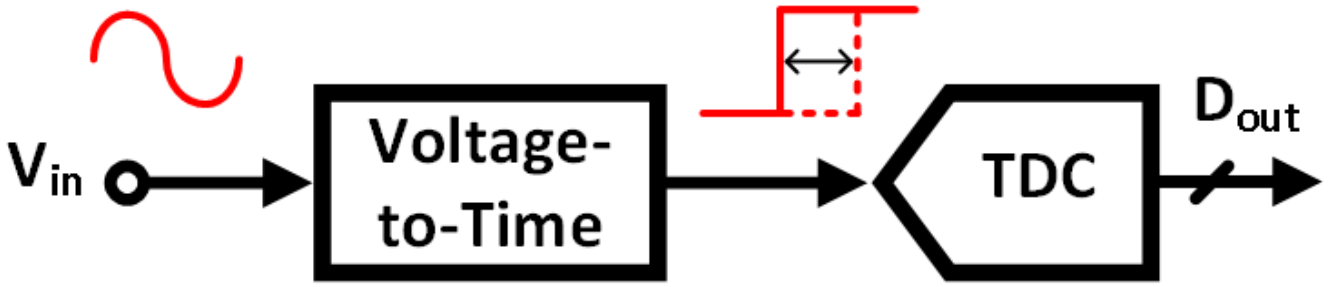
Time Domain Signaling



- **Advantages**
  - **Signal magnitude <u>not</u> limited by supply voltage**
  - **Resolution improves in advanced CMOS**
- **Drawback**
  - **Tradeoff between speed and resolution**

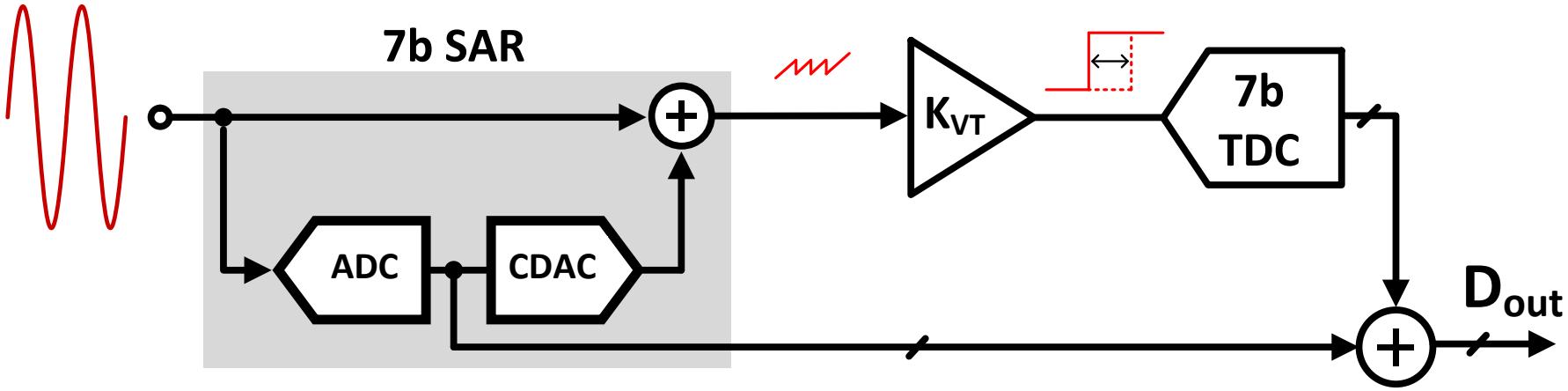
Time-Assisted ADC (Ex.)



- ADC = V/T conversion + TDC
  - Digital quantizer can reduce power, area, scalability
  - V/T must process full scale input
  - TDC must have fine time resolution
    - 20 MHz, 13b → $T_{LSB} \cong 6$ pS

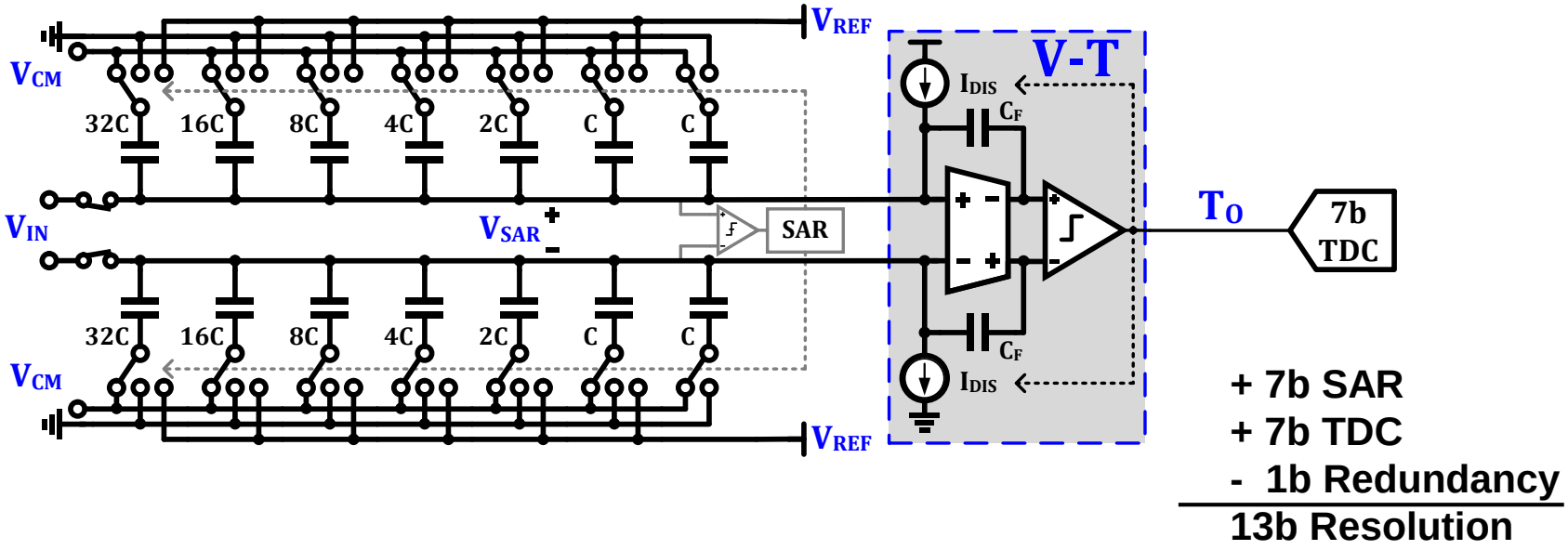
- <u>Idea:</u> combine voltage domain and time-assisted techniques into hybrid architecture

Proposed Two-Step ADC



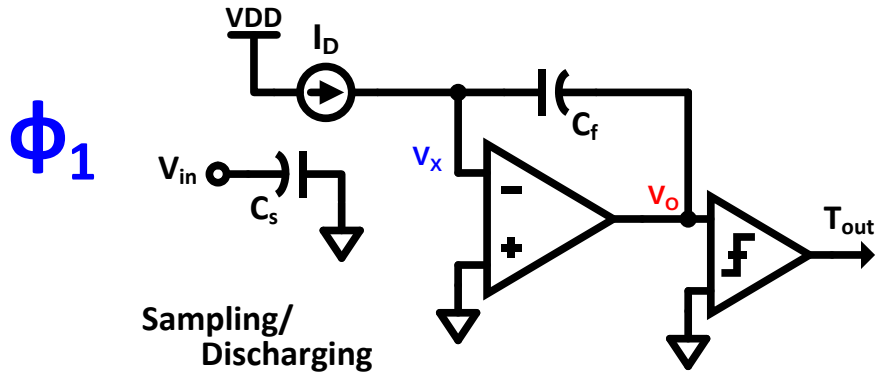
- **Hybrid voltage and time architecture:**
  1. **Coarse SAR quantizer**
  2. **Small residue converted to time pulse signal**
  3. **Scalable time-domain backend quantizer**

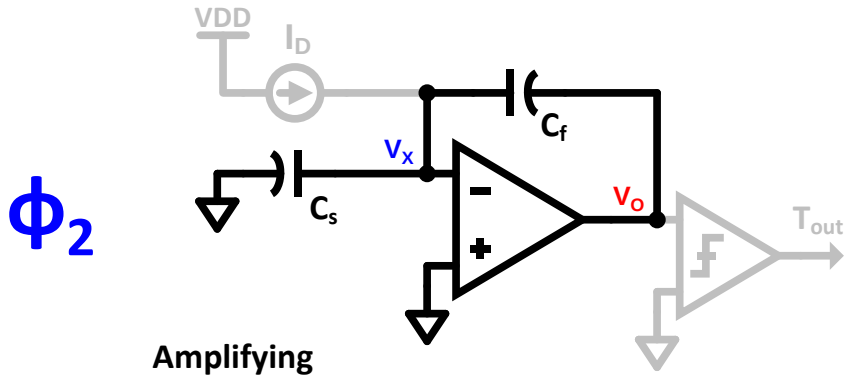
System Implementation

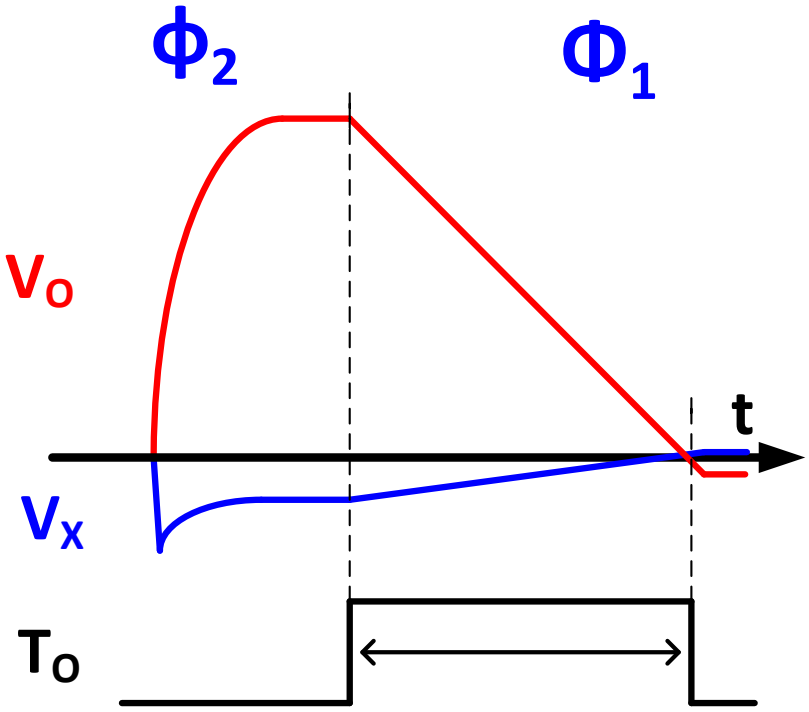


- Hybrid ADC performance
  - Low power, high resolution, moderate bandwidth
  - Favorable tradeoff for scaling CMOS
- Analog requirements of the V-T residue amplifier?

High Speed V-T Residue Amplifier



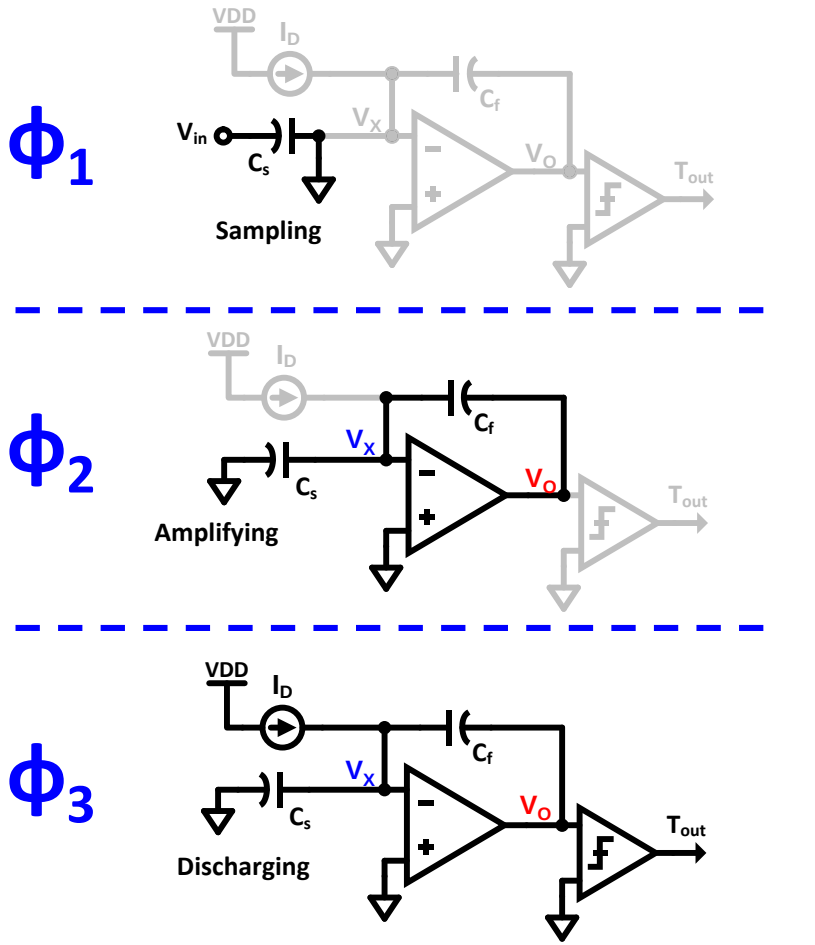


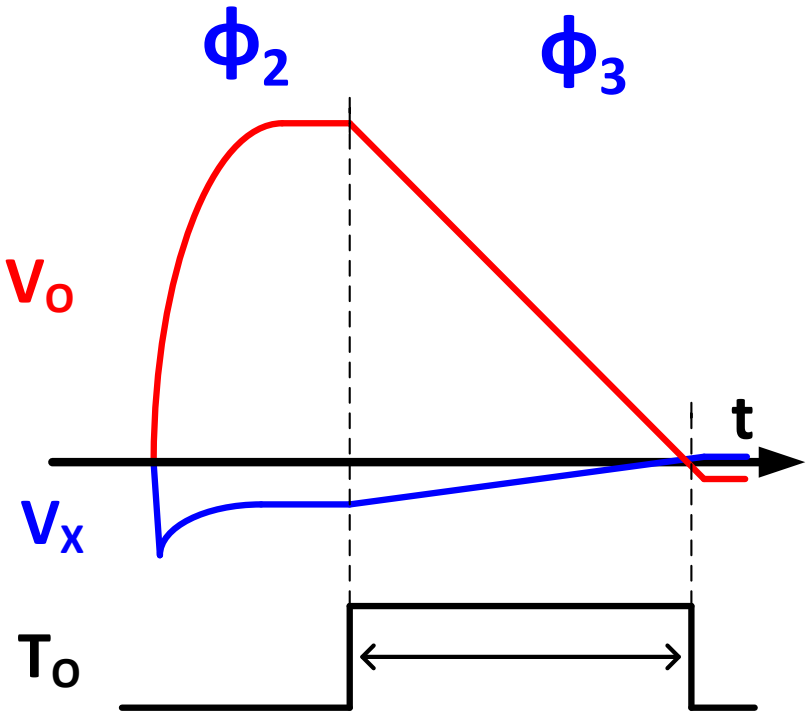


$$T_o = V_{in} \cdot \frac{C_S}{I_D} \cdot \frac{A_0\beta}{1+A_0\beta}$$

- Two-phase operation
  - Time output depends on Amplifier Gain (A_0)

3 Phase V-T Residue Amplifier

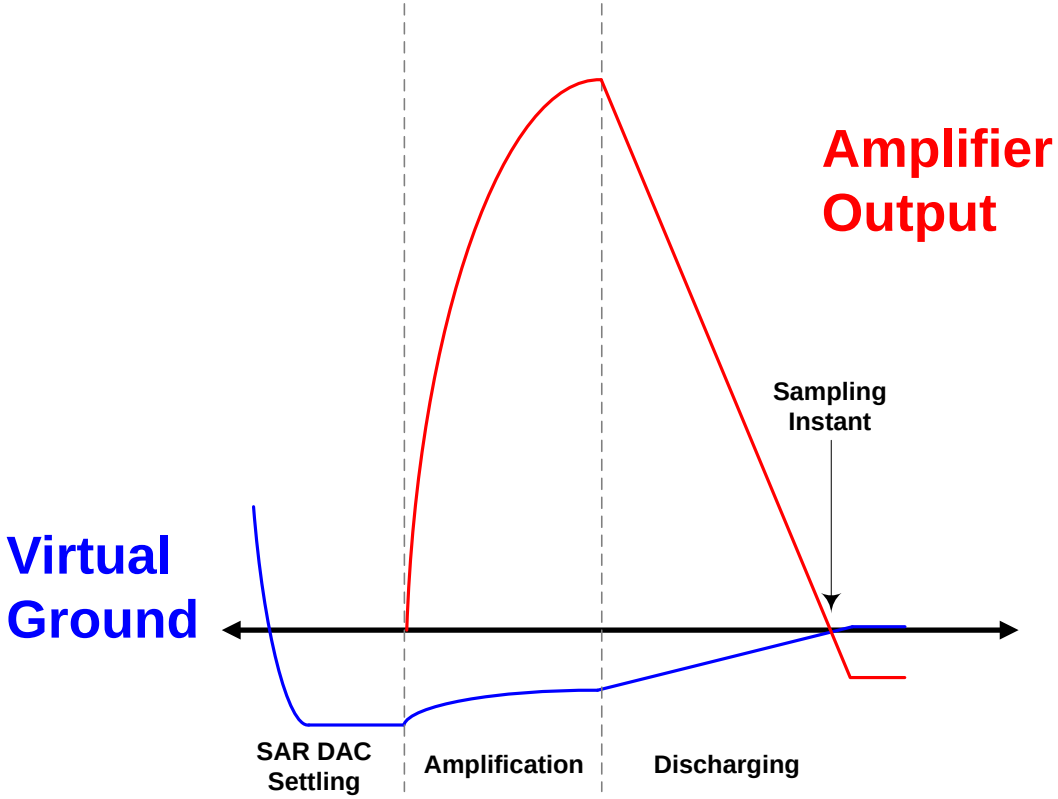




$$T_o = V_{in} \cdot \frac{C_S}{I_D} \cdot \frac{A_0\beta}{1+A_0\beta}$$

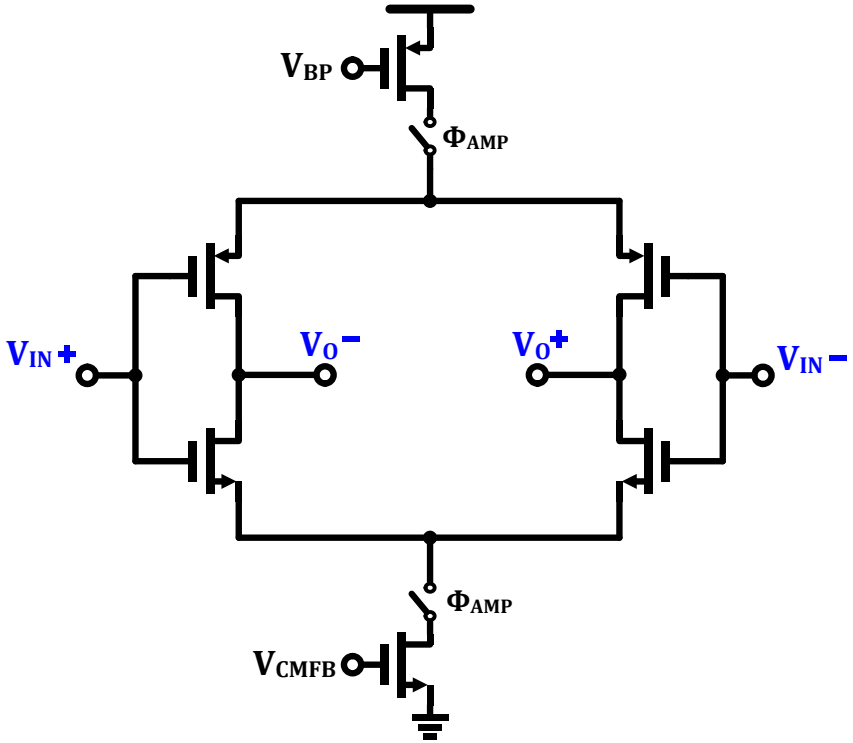
- **Three-phase operation**
  - **C_S and C_F discharged together → no charge loss**
  - **Relaxed amplifier gain and swing**

Residue Sampling



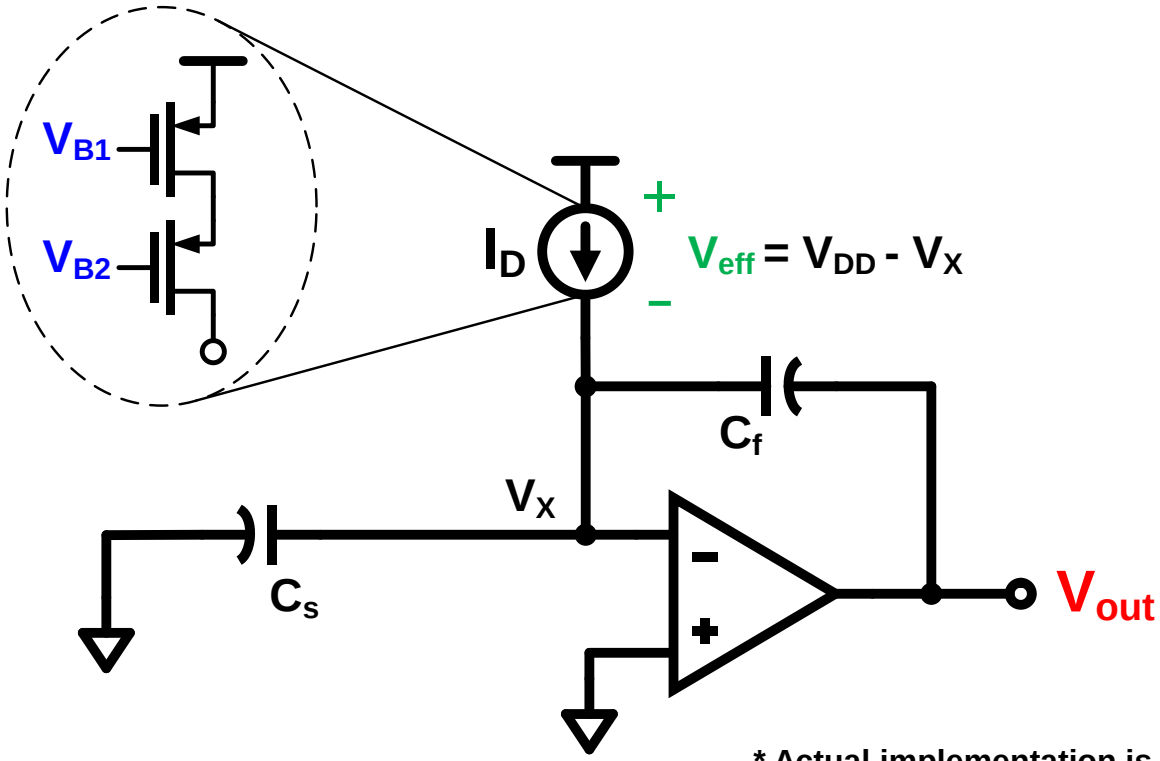
- Sampling is independent of amplifier characteristic
  - Time signal sampling instant → always same output voltage
  - Zero-crossing detector delay → signal independent offset

Residue Amplifier



- **Single Stage Class-AB amplifier**
  - **Wide bandwidth**
  - **25 dB open loop gain**
  - **Dynamic power consumption**

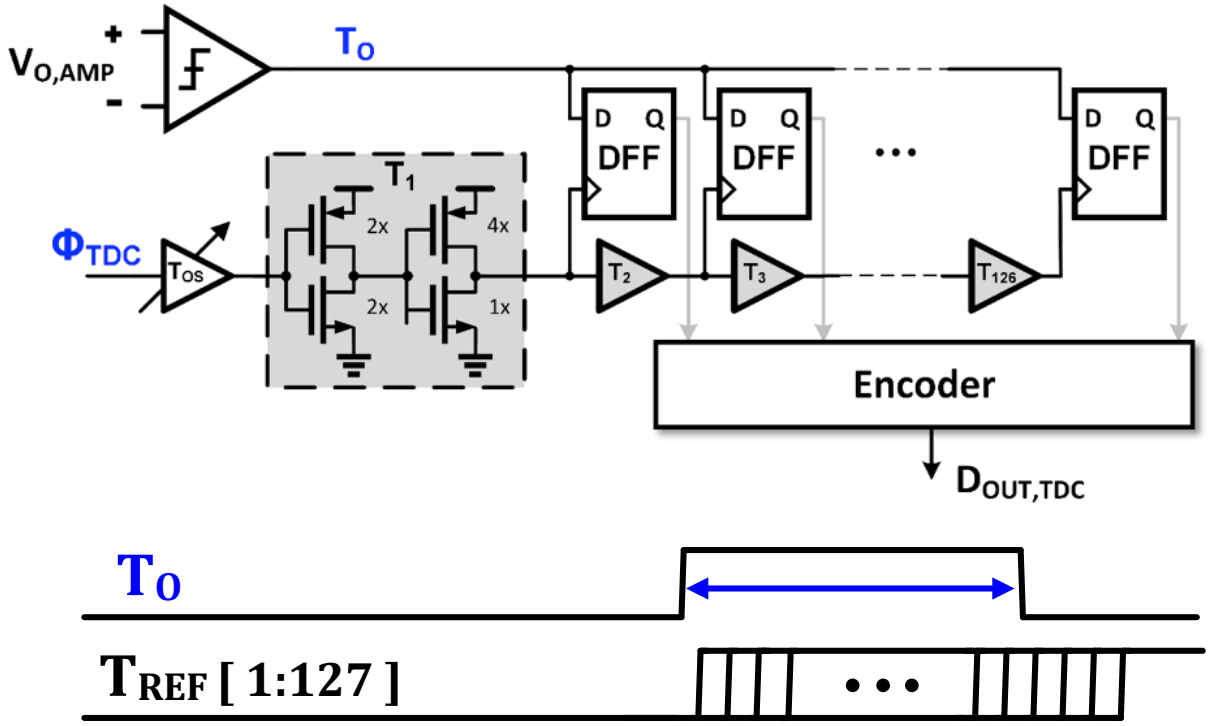
Current Source Design



* Actual implementation is fully differential

- Small voltage swing across current source
- I_D mismatch results in static offset

Time-to-Digital Backend



- Delay line clocks flip flops to sample T_O
- Low supply and small devices
- 335 uW power @ 1.0 V, 20 MHz operation

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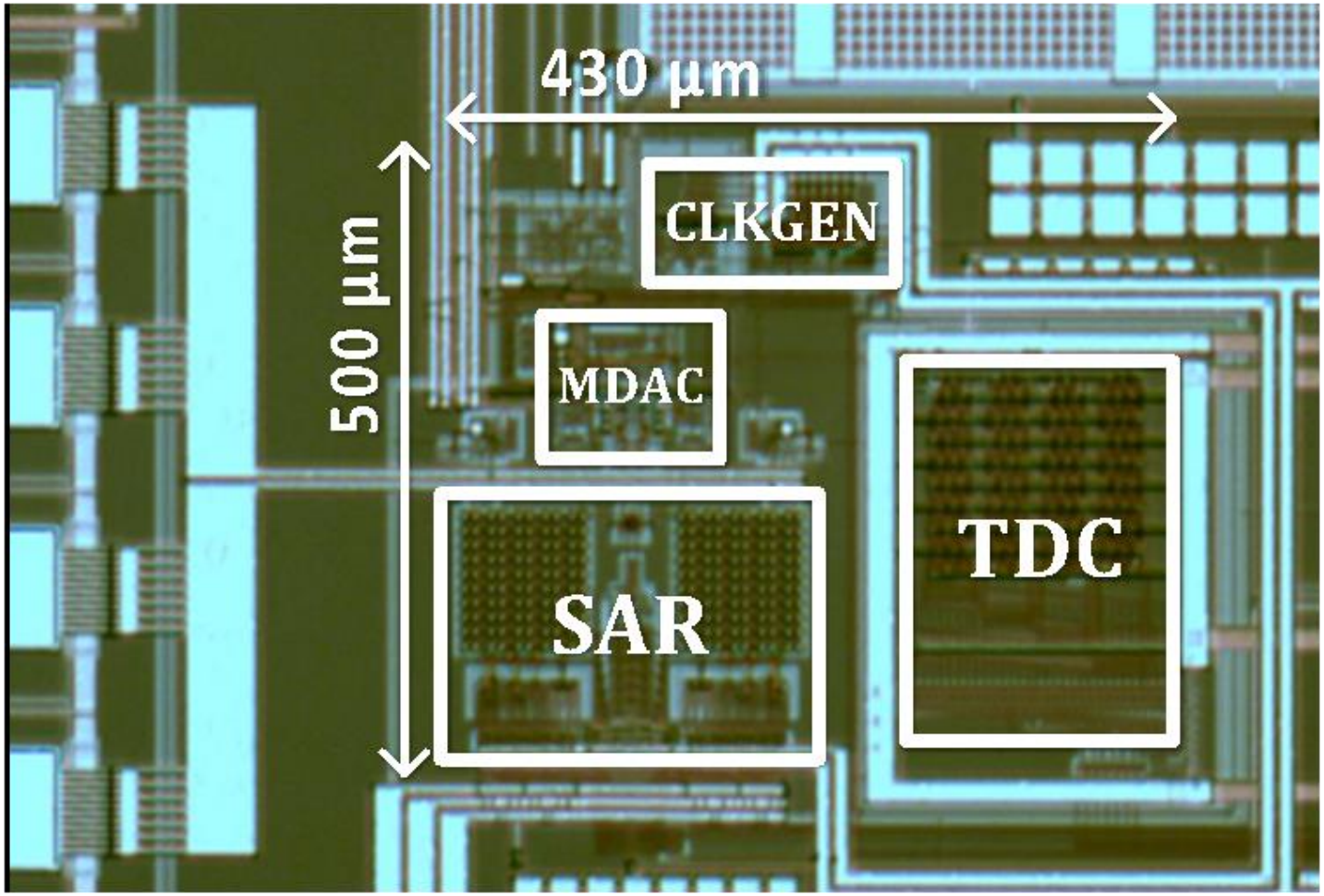
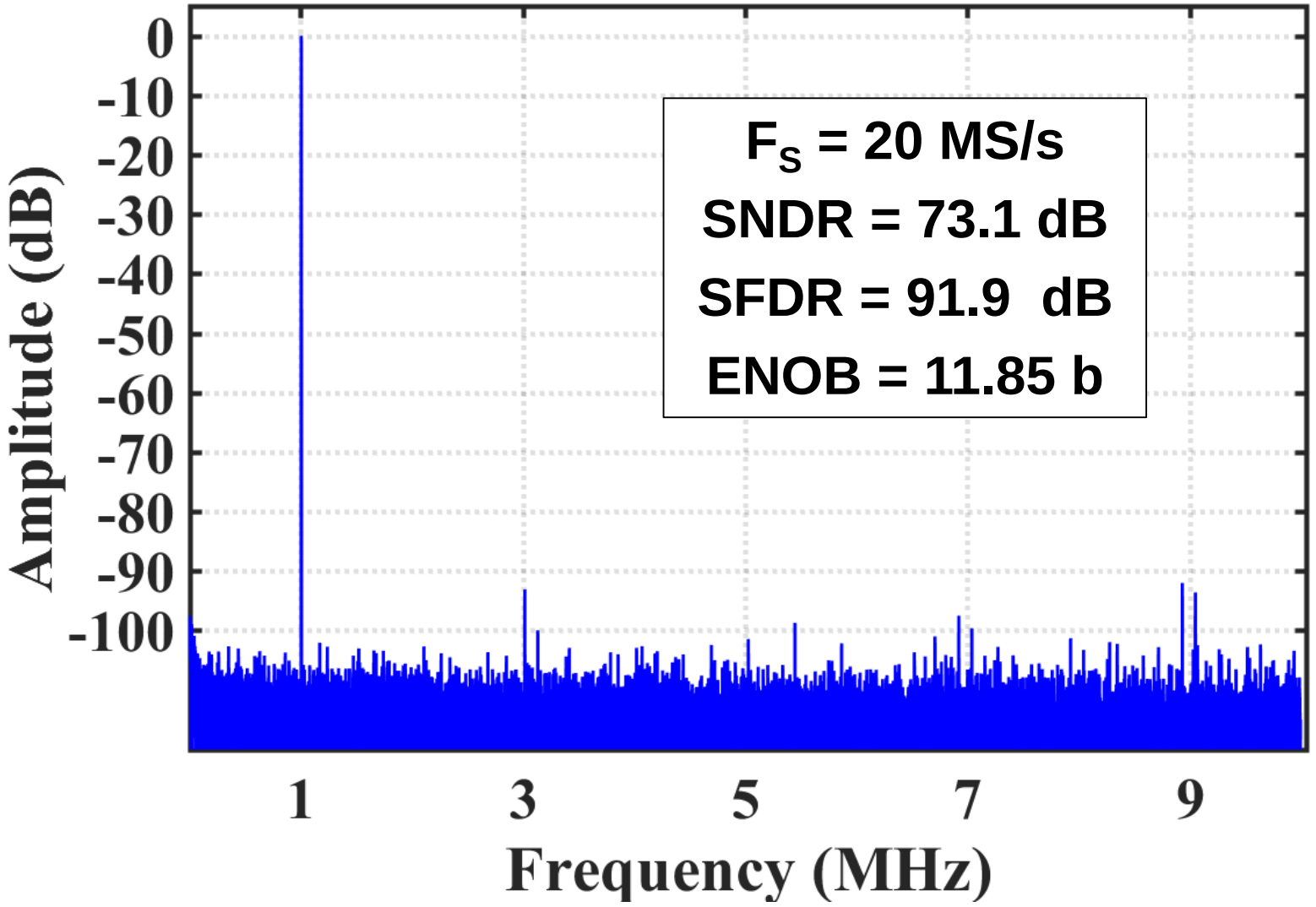
Performance Summary

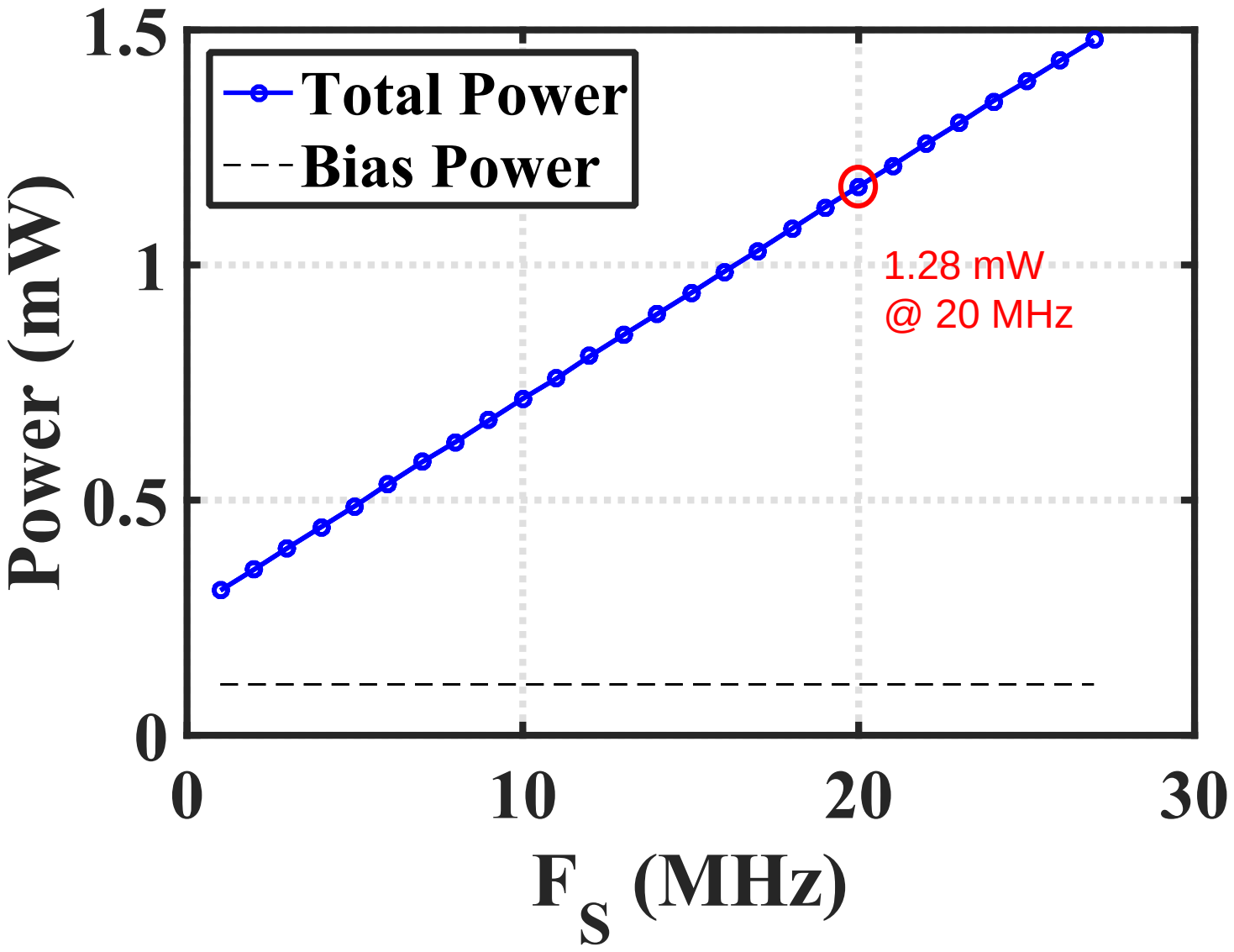


- Active Area = 0.215 mm^2

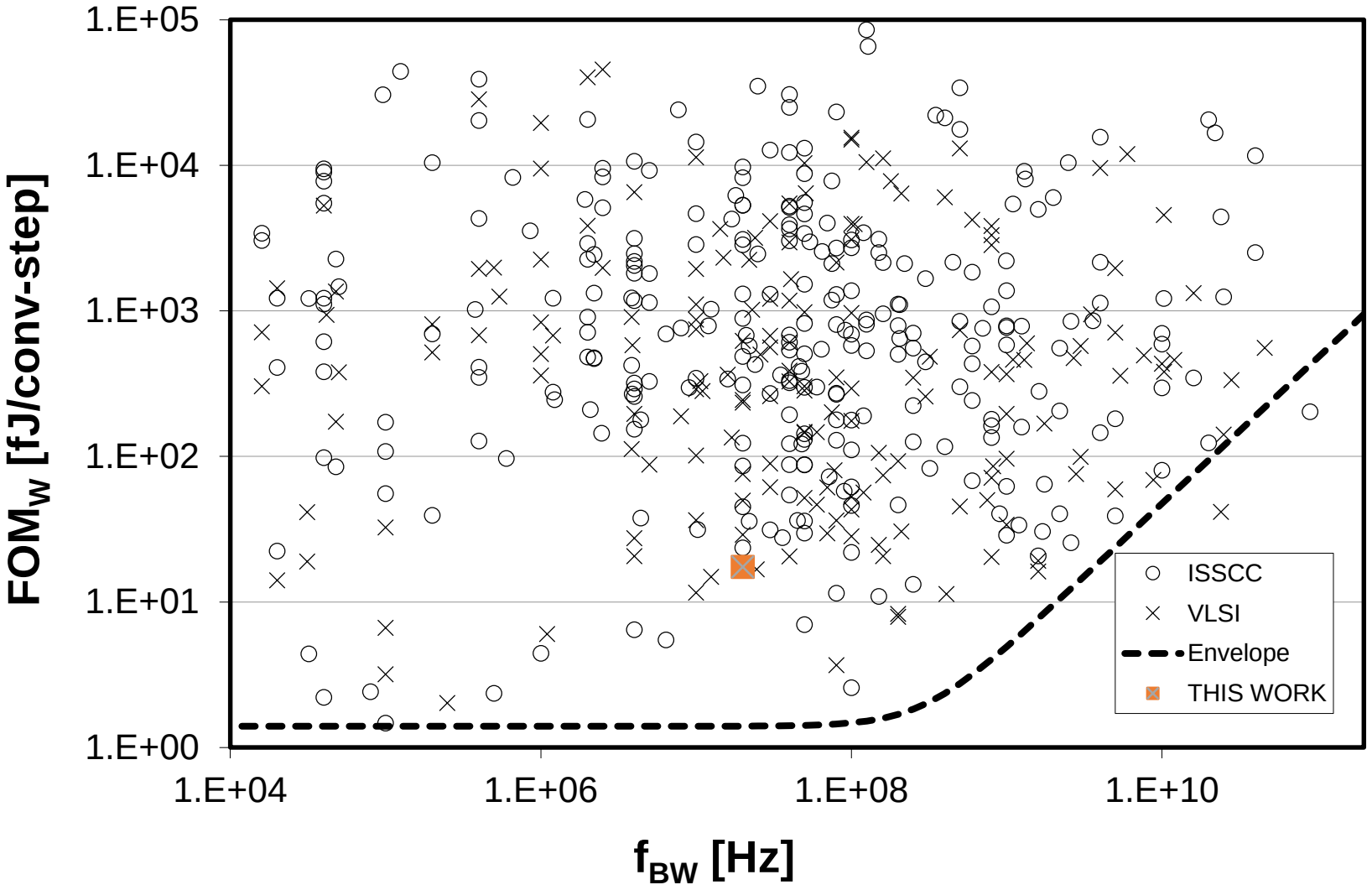
Dynamic Performance



Power Consumption

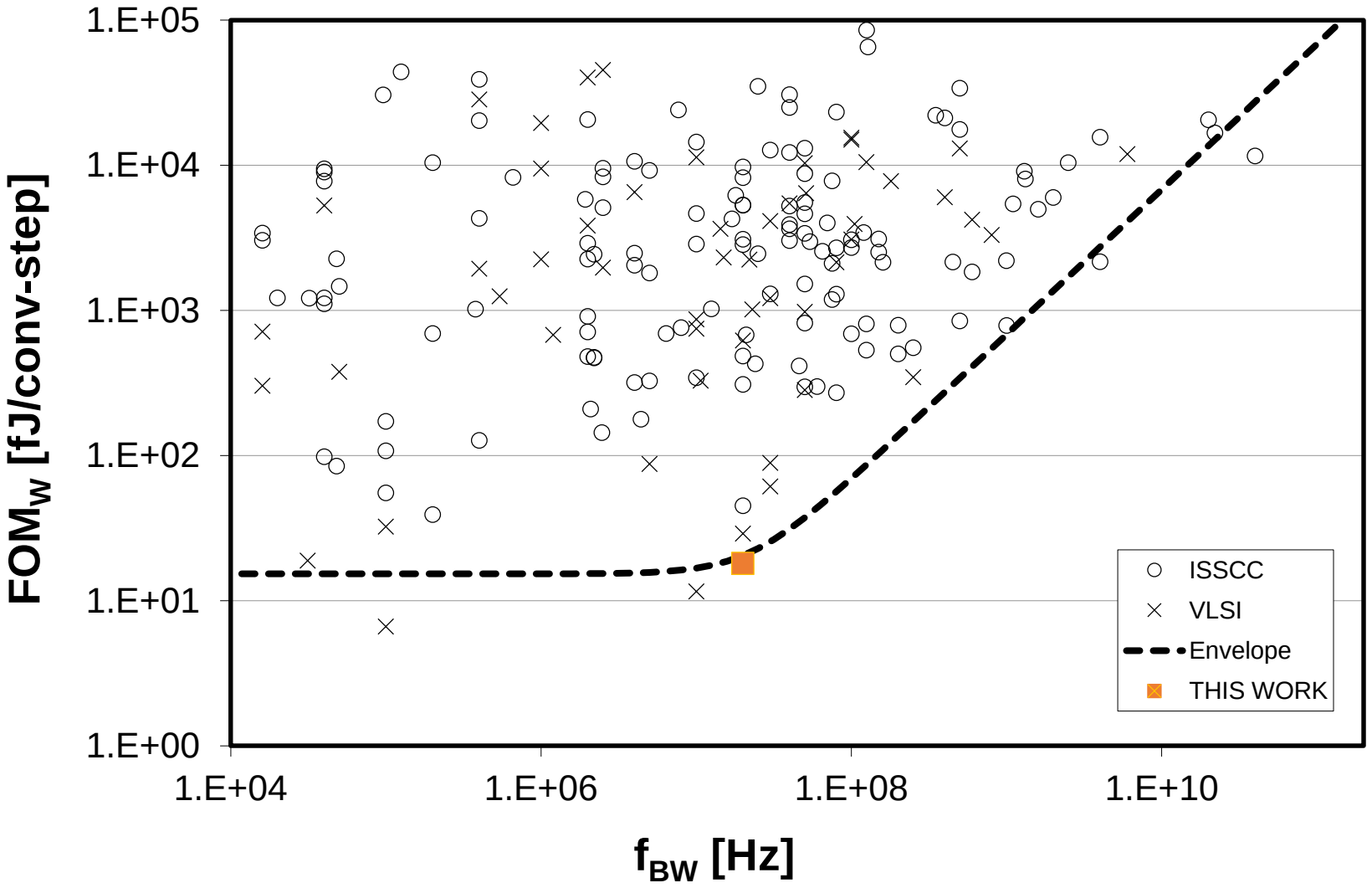


Walden FOM



B. Murmann, "ADC Performance Survey 1997-2016," [Online]. Available: http://www.Stanford.edu/~murmann/adcsurvey.html

180nm Walden FOM



B. Murmann, "ADC Performance Survey 1997-2016," [Online]. Available: http://www.Stanford.edu/~murmann/adcsurvey.html

Conclusion

- **Demonstrated a 13b 20MS/s Two-step ADC:**
  - **High resolution voltage and time quantization**
    - **Power efficient SAR**
    - **Process scalable TDC**
  - **Scaling friendly V-T amplifier**
    - **Relaxed gain**
    - **Low output swing**
  - **Special thanks to AKM for fabrication and packaging**