6.5 A 4b ADC Manufactured in a Fully-Printed Organic Complementary Technology Including Resistors

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Organic transistors (OTFTs) can be printed on thin plastic substrates to obtain mechanically flexible large-area electronics with high throughput. Examples of applications include sensor-augmented RFIDs fabricated on the packaging of retail items and smart surfaces integrating sensors or actuators. Printed OTFTs have been used to design circuits [1-4], however, these implementations have been mainly limited to digital circuits or large-area switch matrices. A major challenge in the design of printed circuits is the relatively high variability in the characteristics of the OTFTs, which is caused by the low degree of spatial correlation typical of printing processes. A relatively high rate of hard faults is also typical in printed electronics (at the state of the art, yield is acceptable only for a circuit complexity of ~100 transistors).

An improved robustness to TFT variability can be enabled using a complementary technology, instead of common p-only solutions. In this paper we exploit a sheet-based complementary printed organic technology [5] to design, implement and measure a flexible and low power 4b ADC. The circuit, an ADC manufactured with printed electronics, can enable applications exploiting sensors that do not require high-speed or high-resolution, like coarse ambient temperature monitoring.

The ADC is fabricated in a printed process flow which integrates top-gate P- and N-type OTFTs together with carbon resistors on a flexible substrate. OTFTs are based on small-molecule organic semiconductors in solution, and show high performance, with typical mobility of 1.5cm^2/Vs and 0.55cm^2/Vs for P- and N-type, respectively [5]. To form the resistors, a carbon ink is screen-printed after the steps related to organic semiconductors patterning and before screen-printing the gate layer. The minimum feature size in this design is 20µm.

The simplified structure of the counting ADC is shown in Fig. 6.5.1. It consists of three blocks: a counter, a 4b "R-2R" DAC, and a comparator. All circuits were simulated based on a compact model for complementary OTFTs [6]. After manufacturing, each block was separately measured, and all of them showed correct functionality. Finally the full ADC functionality was tested using an external counter to simplify the experimental setup. The measurements were performed in air during a period of several weeks, which confirms the robustness of this technology to environmental aggressors.

The choice of a resistor-based DAC has been made because of two main reasons: resistors are expected to have better matching than OTFTs in printing technologies, since fewer process variables can affect the performance of a resistor. In addition, the high resistivity (35kΩ/sq) allows us to use a smaller area compared to capacitor-based options (which also suffer from leakage and thus cannot be operated at too low a frequency). The size of the unit resistors (6MΩ) was chosen to ensure a negligible effect of the on-resistance of the inverters used at the input of the DAC on the ADC's linearity, and without limiting the speed of the circuit (τ=RC$_{load}$=0.1ms). Figure 6.5.2 shows the measured DNL and INL of the DAC. Maximum DNL is 0.24LSB, and maximum INL is 0.42LSB. Assuming the standard deviation of the DNL equal to its maximum measured value, the measured DNL is compatible with a 0.75% mismatch standard deviation ($\sigma_{\Delta R/R}$) between the resistors in the measured DAC, ignoring the effect of the inverter resistance.

Figure 6.5.3 depicts the schematic of the toggle FF (T-FF) with asynchronous reset used in the 4b ripple counter. Due to the requirements of printing, a large distance is specified between n-type and p-type semiconductors. Therefore, the high transistor count of fully static master-slave (MS) FFs makes it difficult to use them in real applications, since the available area of a sheet is only 100cm^2. Fully dynamic FFs [4] may, on the other hand, suffer from soft failures due to the OTFT variability. For this reason, a transmission-gate (TG) FF, which occupies an area four times smaller than a fully static MSFF in our technology, was used for the counter. Figure 6.5.3 shows the performance of the first stage of the counter when an asynchronous reset is applied. The counter outputs (Q1-Q4) for a clock frequency of 67Hz are presented in Fig. 6.5.4.

The schematic of the dynamic comparator is illustrated in Fig. 6.5.5. A non-differential mismatch-insensitive architecture was chosen in order to avoid problems with the large offset that can affect printed circuits, due to the device mismatch typical of these technologies. The first stage is an offset-zeroed inverter-based comparator, which is self-biased and has a rail-to-rail common-mode input range, but needs a quite large input capacitor, due to large parasitic capacitors of the complementary inverter and the charge injection caused by the many switches used [7]. For the second stage, to minimize capacitor area, a comparator based on current copiers [8] has been selected. In this architecture, $C1$ does not need to be very large, since it is in parallel with the gate-source parasitic capacitance of N1. The drawback of the current copier comparator is its limited input range, but this is not an issue in our case as the bias point of the second stage is fixed by the trip point of the inverter. The comparator works as follows: When Clk is high (reset phase), transmission gates S1 and S2 put the inverter in unity-gain and charge the capacitor $C0$ to the voltage difference between the negative input (V_{in-}) and the dc operating point of the inverter (V_{trip}). Since V_{trip} is applied to the gate of P0, the current of P0 is dependent on V_{trip}. This current is copied in the (in this phase) diode-connected transistor N1 (the current copier). When Clk goes low (comparison phase), transmission gate S3 connects the top plate of $C0$ to V_{in+}, and so, the difference between the input voltage values (V_{in+}-V_{in-}) is amplified by the inverter (V_{out1}=A (V_{in+}-V_{in-})). At the same time, S4 opens and the gate-source voltage of N1 is held by the capacitor, $C1$. So, while N1 wants to keep the same value of current as when Clk was high, the gate voltage of P0 is now A(V_{in+}-V_{in}). This situation causes a current-comparison at the output node (Out2), which will bring the output of the comparator to V_{dd} or ground. The measured performance of the comparator is shown in Fig. 6.5.5, where the voltage at nodes Out2 and Out are shown for V_{in}=+400mV and -400mV, and f_{Clk}=70Hz. The output settles in 3ms.

Figure 6.5.6 shows the results of a dynamic measurement of the ADC. Each conversion takes ~240ms (16 clock cycles at 66.67Hz), and the ADC sample rate is thus 4.17Hz. The input signal is full-scale and its frequency is 2.05Hz. First, an ideal staircase was applied to the comparator to evaluate its performance (the graph with ideal DAC). The measured SNDR in this case is 22dB. This value decreases to 19.6dB when the real DAC output (without any calibration) was applied to the comparator. The SNR is about 25.7dB. This measurement demonstrates that the DAC limits the linearity performance of the ADC. The power consumption of the full ADC at 40V supply is 540µW and its area is 24.5cm^2.

A counting ADC fabricated with a printed organic complementary process and featuring an integrated resistive DAC has been presented. Measurements of the ADC show ~2Hz BW, 25.7dB SNR and 19.6dB SNDR, demonstrating the current capability of printed technologies.

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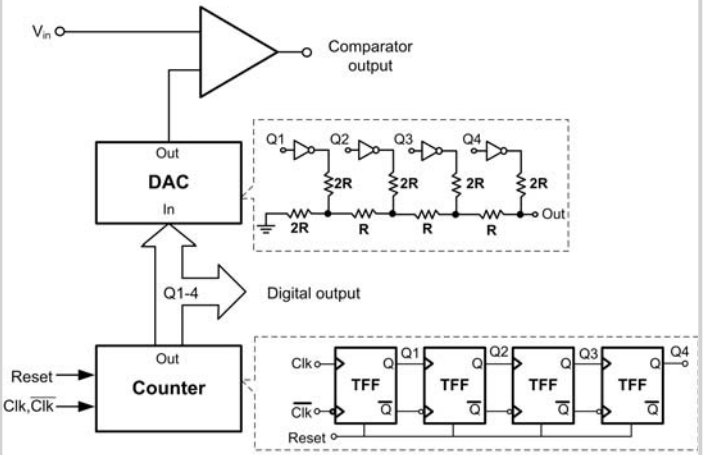

Figure 6.5.1: Simplified ADC architecture. The comparator output determines at which clock the digital output corresponds to the analog input (Vin).

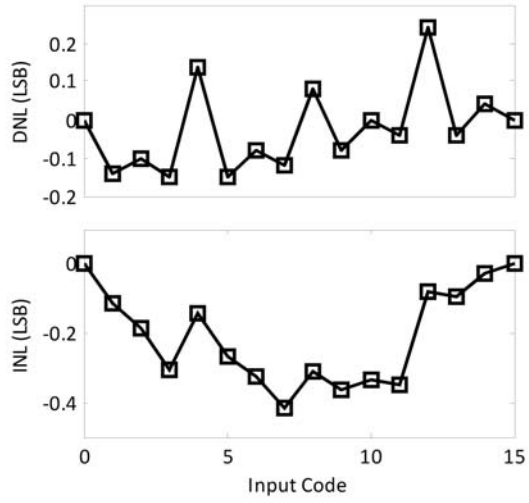

Figure 6.5.2: Measured DNL and INL for the DAC.

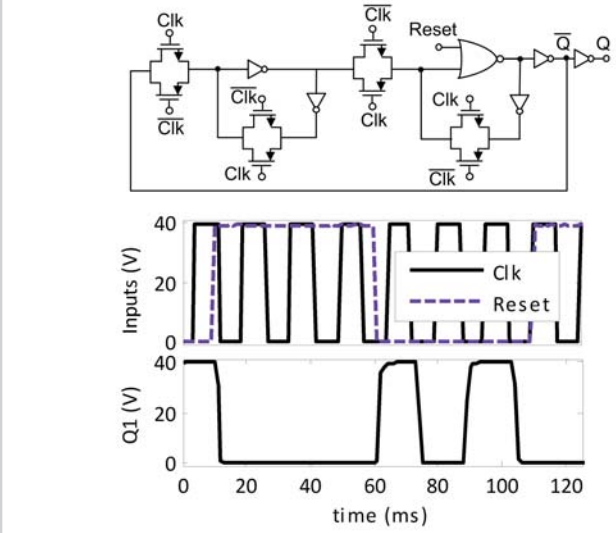

Figure 6.5.3: Schematic of the T-FF used in the counter, and its dynamic measurements (fclk =67Hz).

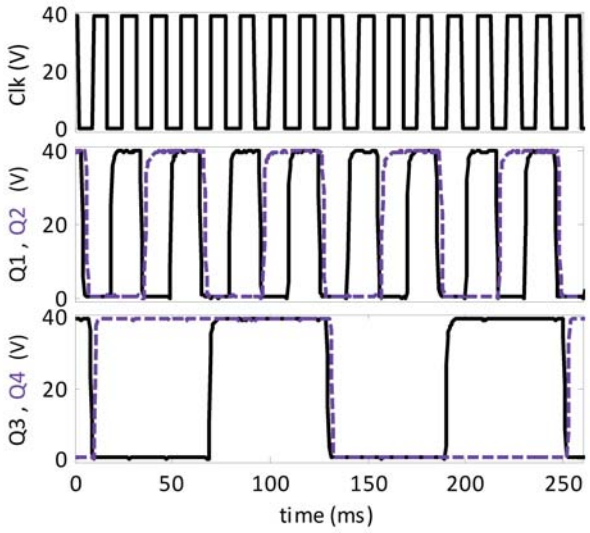

Figure 6.5.4: Counter outputs (Q1-Q4), measured at a clock frequency of 67Hz.

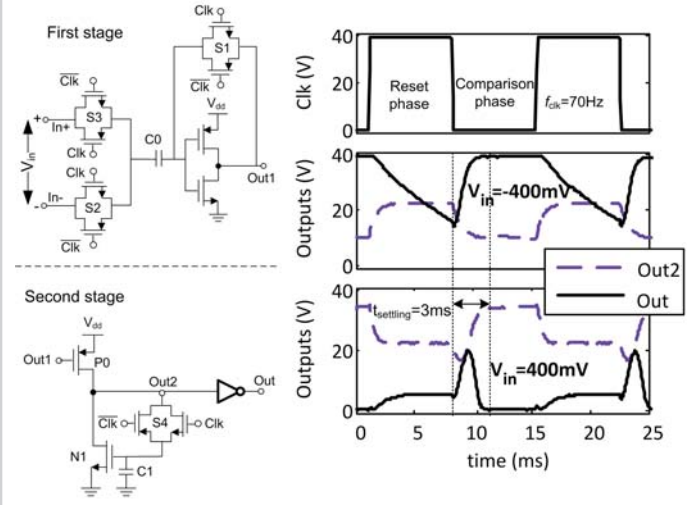

Figure 6.5.5: Schematic of the comparator and its measured performance at Vin=+400 and -400mV.

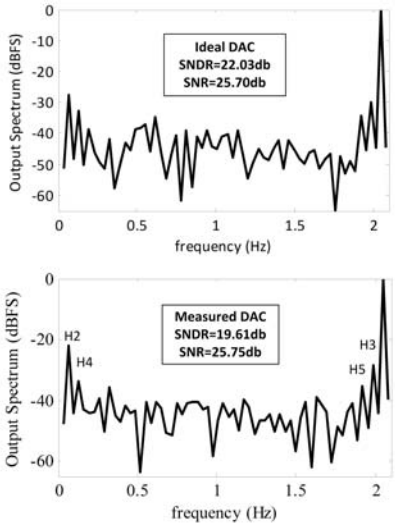

Figure 6.5.6: Measured output spectrum of the ADC, based on ideal DAC and measured DAC (H2-5 show the first harmonics).

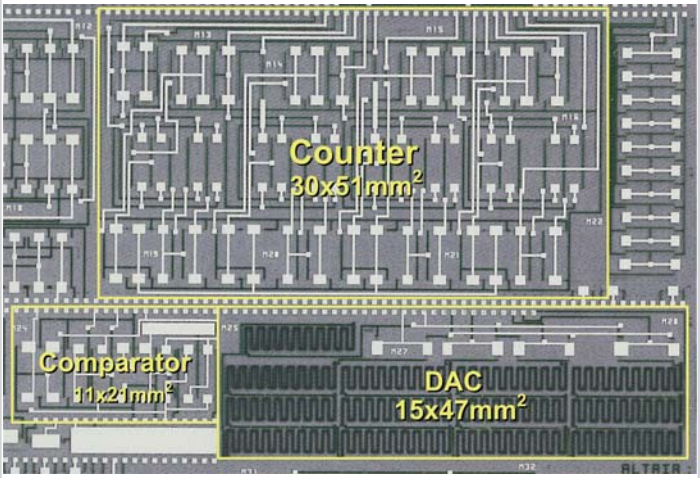

Figure 6.5.7: Photograph of the foil.

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