A Comparative Study of Pre-bond TSV Test Methodologies

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***Abstract*— A comparative study of pre-bond TSV test methodologies is presented in this paper. The study includes the impact of interconnect wires and I/O transmitter and receiver parameters on the sensitivities of the test methods. We study four classes of test methods. Simulation results provided show that two classes, ring-oscillator based [7, 8] and pulse-shrinking based method [15], are insensitive to open and short defects. We also show that there is a trade-off in using the other two methods. The sense-amplifier based method [12, 13, 19] is sensitive to open defects. However, it has limited sensitivity to leakage defects and has limitations in its use for high speed I/Os. On the other hand the pulse counting method [18, 14] is sensitive to both open and leakage defects and can be used for high speed I/Os. However, it consumes more power and requires more time for tests than the sense-amplifier based method. These results can be leveraged to identify usage guidelines for these methods.**

Keywords—Pre-bond TSV test, No-Touch Test, DFT, 3D IC.

I. Introduction

Through-silicon-via (TSV)-based integration is regarded as important method to design three dimension integrated circuits (3D ICs). TSVs are used as vertical inter-die interconnects of a 3D IC [1-3]. The ability to effectively manufacture and screen for defective TSVs is important to the successful deployment of this technology. TSVs are susceptible to a variety of defects, viz.: the formation of voids and cracks, incomplete fill, presence of pinholes in the insulator boundary, missing of landing pads, improper connections between pads and TSVs, electro-migration etc. [4-5]. In manufacturing 3D IC, individual dies are tested prior to stacking and packaging. A packaged IC fails even if the constituent dies are fault-free but one or more TSV is defective. Thus TSV defects adversely affect the chip yield resulting in higher manufacturing cost. This is especially true for advanced process nodes. A pre-bond TSV test is added to address this challenge. In pre-bond TSV tests, TSVs are tested at SORT prior to stacking and packaging [7-9].

In one form of pre-bond TSV test, only one end of the TSV is exposed while other end is inaccessible. Figs. 1(a) and (b) show an example of a pre-bond TSV along with the associated I/O drivers. Accessibility and controllability limitation results in traditional interconnect tests to be in-feasible. For this reason, a number of pre-bond TSV tests, targeting shorts and opens, have been proposed [8-9, 11]. The underlying idea in all these methods is to determine the perturbation of the characteristics of the fault-free TSV in the presence of a defect.

In this work, we present a comparative study of different pre-bond TSV tests methodologies discussed in the literature. The pre-bond TSV test methodologies are classified into four major groups. The simulation based study uses simulation parameters of an advanced process node. It takes into account the effect of the presence of I/O capacitances, and the interconnect wire between the TSV and I/Os. Such practical constraints were not included in most of the published works.

Our objective is to determine the feasibility and practicality of using pre-bond test methods. For that, from each group, we select a representative pre-bond TSV test methodology for our study. We then evaluate and analyze the sensitivity of these methods to the defect parameters for open and short defects.

The main contribution of this paper are the following conclusions from the simulation study.

(1) Two classes of pre-bond TSV test methods [7, 8, 15] have limited detectability for any defects, when practical interconnect wires and I/Os are considered in an advanced process node. The two methods are referred to as the RC-delay-closed-loop-frequency-counting [7, 8] and pulse-shrinking test [15].
(2) The other two classes of pre-bond TSV test methods are equally good at detecting open defects [14, 18, 12, 13, 19]. The method of [14, 18] is referred to as the charge-pump and pulse counting method. The method of [12, 13, 19] is referred to as the sense-amplifier based method.
(3) The charge-pump and pulse-counting is more sensitive to short defect compared to the sense amplifier counterpart.
(4) The sense amplifier-based pre-bond TSV test consumes less power and enables higher speed test than the charge-pump and pulse-counting. However, the sense amplifier method cannot be used for high speed I/Os and circuits.

Based on the above results the following guidelines are proposed. The sense-amplifier based method [12, 13, 19] can be used for very low power designs, using slow speed I/Os where short defects are not significant. For all other scenarios the charge-pump, pulse-counting method [14, 18] is the preferred pre-bond TSV test method to be used. The findings of this study are beneficial for advanced process nodes, where the yield rate of the TSV is a concern and pre-bond TSV tests are necessary. For matured technologies (say 22nm or earlier), post-bond TSV test may be a more cost effective approach.

II. Pre-bond TSV Test Model and Challenges

In this section, we discuss the TSV model under study, and associated challenges to for pre-bond TSV testing.

A. TSV Model Used in the Study

To characterize the electrical behavior of a TSV that is accessible from only one end, we model it as a RC circuit [20]. In our study, the operating frequency and the dimension of the TSV are such that the inductance has negligible effects on the

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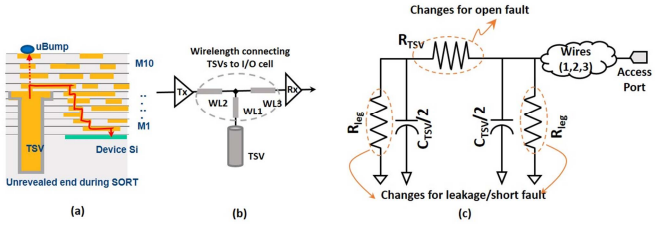

Fig. 1: (a) Pre-bond TSV during SORT, (b) TSV connection with different segments of wirelength (WL), (c) Lumped π-model for TSV.

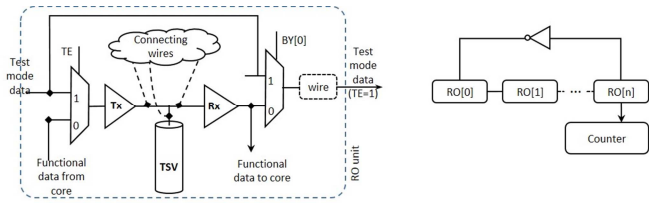

Fig. 2: Set up for ring oscillator based TSV fault detection. (Left) Basic ring-oscillator (RO) unit with TSV and associated logic circuits, (right) *n* number of RO units are connected with one inverter in ring to form experiment set up [8].

TSV delay. Hence, we ignore the inductance impacts. Fig. 1(c) shows the model of a standalone TSV with connecting wires between the TSV and I/O drivers. R_{TSV} represents the resistance of the Cu material of the TSV for the through current. The capacitance of the TSV to the ground is represented as C_{TSV}. In addition, the shunt or leakage resistance of the TSV to the ground is represented by the R_{leg}. For a fault free TSV, the value of the leakage resistance are in the order of several hundred MΩs. The TSV parameters for the state-of-the-art studies are- the R_{TSV} of a Cu-based TSV with diameter of 2-5 µm and height of 15 µm is 8~200 mΩ [15, 20], the C_{TSV} is 10~200 fF [16, 20], and the leakage resistance, R_{leg}, is more than 850MΩ [13, 20].

We consider two kinds of defects and model them as open- and short-faults. Whenever, any open fault (relating to the formation of voids, cracks, incomplete fill) occurs in the TSV, it affects the through current of the TSV and consequently, the value of R_{TSV} increases. The leakage fault (related to the pinholes and thinning of TSV wall) affects the charging and discharging phase of the TSV and consequently, the leakage resistance, R_{leg}, is changed (reduced).

B. Design Constraints and Challenges of Fault Detection

When we consider the practical design constraints, it imposes several challenges to the pre-bond TSV test. First, we consider three segments of wirelength are placed between the TSV and the I/O drivers due to the keep-out-zone (KOZ) of the TSVs. In advanced technologies, it has significant effects on RC-characteristic of the TSV. For example, if lower level metals are used as wires the TSV, the resistance of a 50 µm wire-segment can be 2~3 KΩ for the current technology as outlined by ITRS (replaced by IEDM at present) [17]. For TSVs with large KOZ, the RC delay of the connecting wire dominates the overall delay. As a result, effects of small open and leakage faults are often masked out. Second, the additional challenge for I/O TSVs is the 'masking effect'. In general, values of resistance and capacitances of a fault-free TSVs are small [15, 16, 20]. The variation in delay between a faulty and fault-free TSV is in the order of several ps. However, if the size of the I/O cell drivers are large, then small variation of the RC delay of any faulty TSV is masked out by the large I/O drivers.

C. Problem Statement For Pre-bond TSV Test

We consider a design space consists of a multi-stacked 3D IC, where the TSVs act the vertical communication pillar (signal or I/O). The formation of voids, cracks, incomplete fill of the TSV materials, and misalignments of bonding pads in the TSVs are represented as TSV open-faults, which refers to increase in series resistance of the TSV, R_{TSV} (Fig. 1(c)). The presence of pinholes in the TSV wall, insufficient thickness of insulator layer, and presence of leakages are modeled as TSV short faults. The parametric value of leakage-leg resistance, R_{leg}, reduces depending on the severity of leakages. During SORT, one end of the TSV is buried in the silicon, while other end is accessible. Hence, the test methodology has only access to one segment of the TSV. Considering this and other practical design constraints (as mentioned above), we study different kinds of pre-bond TSV tests. We classify them in several groups and choose one from each group to test the basic working principle. Our aim is to study the efficacy of different methods and establish trade-offs among them.

III. PRE-BOND TSV TEST METHODOLOGIES

Several works have explored the pre-bond TSV testing [7-16]. According to the basic working principle to identify TSV defects, we classify them in four groups viz. (i) RC-delay-based closed-loop frequency counting (ring oscillator), (ii) pulse shrinkage-based method, (iii) sense amplification, and (iv) charge pump and pulse counting. There is another group that depends on the mechanical and thermal characterization of the TSV. These also includes probing to the TSV, thermal imaging, laser scanning and so on. The probing method faces the challenge of matching the size of the probe to that of the TSV-pitch size. The thermal and laser imaging methodologies need on-chip integration of lots of additional components. In this work, we limit our discussion to the TSV tests that use on-chip electrical characterizations only.

A. RC-delay-based Closed Loop Frequency Counting

Among different contactless pre-bond TSV test methods, ring oscillator-based approach is popular [7, 8]. The main idea is to connect a group of TSVs in a closed loop ring with odd number of inverters and measure the oscillation period of the loop. In the first step, TSV and associated I/O drivers (termed as the ring oscillator (RO) unit) are put in bypass mode and oscillation period is calculated. Next, the target RO is connected in the loop one at a time and oscillation is counted. The difference in the counter output between these two steps characterizes the TSV under test. In general, for the TSV with any kind of open-faults, the delay of the loop decreases and the oscillation frequency increases. For leakage faults, opposite effects takes place and the delay increases.

Fig. 2 explains the RO-based TSV fault detection methodology. Fig. 2 (left) shows the diagram of an RO unit and (right) explains overall RO-based set up. The TE (test enable) signal controls the operational and test mode and the BY[n] (the bypass mode controller) regulates whether or not the RO unit is connected with the ring-oscillator loop. In the figure, the placement of connecting wires (marked as dotted lines as it was not included in the original study) is also shown. The connecting wires significantly affect the TSV characteristics

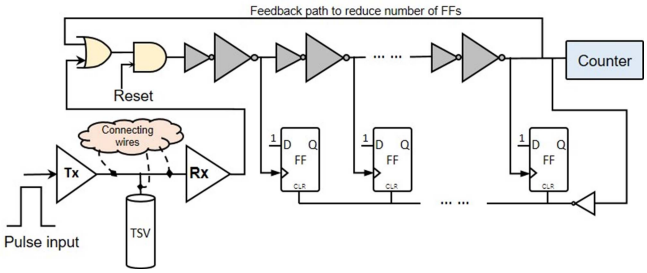

Fig. 3: Pulse-shrinkage-based TSV fault detection methodology. In addition the basic experimental setup [15], the connecting wires to the TSVs and I/O drivers are added during experiment and simulations.

and fault detection resolutions. The modified ring oscillator [21], phase-frequency and delay-locked loop based tests [22] also use the same principle as the ring oscillator. For delay locked loop-based test, the variation in RC-delay is used in a feedback loop to convert into voltage and process it.

Overall, there are three challenges with the RO and/or delay-measurement-based tests. First, the connected wire between the TSV and I/Os have significant effects on the delay. Second, the delay and hence, the oscillation period is affected by PVT variations. Determining a standard signature frequency becomes difficult across PVT variations. Third, the large capacitance of I/Os masks out any variation of the delay (and oscillation frequency) for faulty-TSVs.

B. Pulse Shirnkage-based TSV Tests

In Pulse-Shrinkage (PS) methodology [15], the main idea of detecting any TSV fault is to evaluate the variation in rise- and fall-delay for an input pulse-voltage passing through a 'pulse-shrinkage (PS)' block. A PS block is formed by two inverters with non-uniform size connected in series, the second is being the larger. The resultant effect is known as 'pulse shrinkage' effect. Fig. 3 shows PS-based TSV fault detection test setup. The TSV (and it's I/Os) is connected in front of a series of PS cells. The output of PS cell is connected to the clock input of a FF while their D input is tied to '1'. The output of the final PS cell is connected to an 8-it counter and connected to the input of first PS cell through a feedback path. Additional OR and AND gates are employed at the input first PS cell to enable the control mechanisms. The feedback path reduces the number of FFs required for this set up. The counter output is calculated to obtain digital code for any TSV. If the TSV is faulty, the digital code varies (reduces for open faults while increases for leakage faults) and compared against signature digital code to determine its type of faults. It is to be noted that the above mentioned set up is chosen as suggested by the work in [15].

In order to achieve the best fault-detection resolution from this test, every DFT circuits need to be placed near each TSV, otherwise the variation in rise and fall times are masked out due to the connecting wires and I/Os. Thus the DFT overhead of this method is high in practical scenario. In addition, the performance against PVT variation is a concern as well.

C. Sense Amplification-based Method

Another popular approach is sense amplifier (SA)-based tests. The idea is to model the TSV as a single ended RC network and exploit the difference of charging or discharging time of the RC tree to sample the voltage level of the TSV. In these approaches [12, 13, 19] after a certain time, the voltage level of the TSV is sampled and compared against a reference value to identify the state of the fault. Depending on the design of the sense amplifier and working principle, the timing and sampling circuitries vary widely.

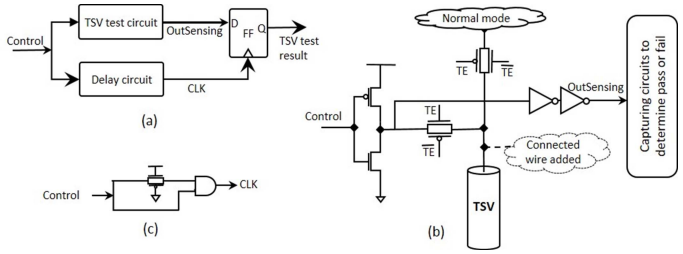

Fig. 4: Sense amplifier based TSV fault detection methodology. (a) Basic block diagram for sense amplifier, (b) TSV test circuit, (c) delay circuit [19].

Fig. 4 shows an example of sense amplifier-based TSV fault detection methodology [19]. The testenable (TE) signal selects the normal or the test mode of the circuit. The Control signal first charges the TSV and when inverted, then let the TSV discharge through the pull down network. The two inverter works as sense amplifier to sample the voltage. The delay circuit generates the sampling signal and captures the voltage level of the TSV after a fixed time. The output of the sense amplifier (OutSensing) is post processed to determine the state of the fault. If either any open fault or strong leakage is present, the TSV discharges quickly and the TSV is marked as faulty at the output of the capturing logic block. The major challenge with this method is the requirement of strict timing matching to sample the voltage level and maintain same fault detection resolution across the PVT variations. Moreover, it also faces the same challenge associated with ring oscillator i.e. small RC-delay variations due to the open or leakage faults are masked out by connecting wires. One important aspect of SA method is the I/O are isolated in the test mode by using a MUX placed in front of them. Such usage of MUX significantly reduces the bandwidth of the I/O operation and this limits the applicability of SA-method for high speed I/Os.

There are several other approaches that are based on the same principle. The measurement of charge and discharge time constants similar to that used in SRAMs is exploited in [12]. Programmable delay time generation and self-timed capturing signal used for charge, float and capturing scheme in [2]. The faulty TSV is used as one leg of a wheat-stone bridge in [11]. For all these test methods, the basic principle remains same and will face the aforementioned challenges as well.

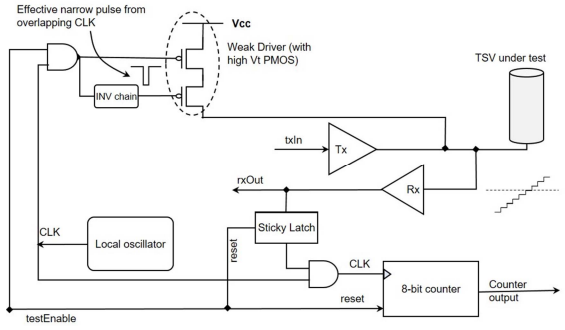

Fig. 5: Overall setup and circuit diagram for Charge Pump and Pulse Counting (CP-PC)-based pre-bond TSV testing methodology. The local oscillator and counter are shared for a group of TSVs to reduce the overhead [18].

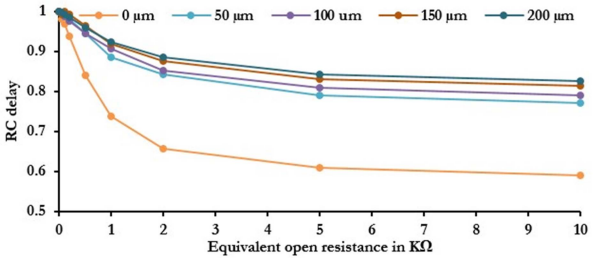

Fig. 6(a): Effects of wirelength on the output delay of the ring oscillator.

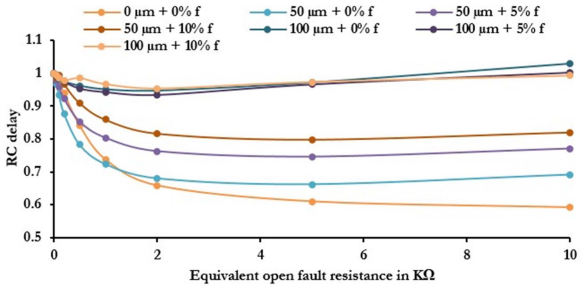

Fig. 6(b): Effects of wirelength and input capacitance on the output delay of the ring oscillator.

D. Charge-Pump and Pulse Counting-based Approach

The basic idea of CP-PC-based [14, 18] TSV testing is to consider the TSV as an one-ended capacitive-network (this is true as the values of R_{TSV} in Fig. 1(c) is really small [12, 15]) and charge it up through a charge-pump. A stream of narrow voltage pulses charges the capacitive network. The number of pulses are counted and compared against fault-free signature value. The counter output depends on the TSV capacitance value and presence of any kind faults. For a TSV with open faults (the capacitance value reduces), less number of pulses are required. On contrary, for any leakage faults, due to presence of low resistance path to the ground, larger amount of through current and increased number of pulses are required.

Fig. 5 shows the overall experimental setup for CP-PC-based TSV testing in this work. The weak-driver determines the amount of charge fed to the TSV network and the overall speed of the test methodology. To minimize the amount leakage current, high-threshold voltage (vt) PMOS is used as the weak driver. An overlapping clock enabled by an inverter chain works as the pulse generator for the weak driver. By varying the design of the inverters, the pulse width at input of the driver can be tuned. The input clock of the weak driver is generated from a local oscillator. The output of local oscillator both feeds the weak driver and the counter. An 8-bit counter counts the number of pulses required to charge up the TSV. Whenever the TSV is charged up, the output of associated receiver (Rx) and sticky latch changes. This freezes the clock of the counter until the sticky latch is reset. It is shown in [18], the performance of this test methodology is resilient to the PVT variations.

IV. Results And Analysis

A. Experimental Setup

We consider the TSV model from Fig. 1(c) in our experiment and an advanced process technology that is used by Intel. The resistance and capacitance of the TSV model is calculated using up to date experiments (for low frequency operation). All the associated DFT circuits are designed with an advanced CMOS process technology. For all simulations across different test methods, the characteristics of the connected wire, I/O drivers, and TSV are kept same.

For the open-fault detection, as a case study, the open fault is assumed to be taken place in the middle of the TSV. If the fault is occurred other than the center portions of the TSV, it can be incorporated with a distributed pi-model. The value of R_{TSV} changes depending on the severity of the open-fault. In our experiments, the value is chosen to vary from 0 KΩ (fault-free) to 10 KΩ (strong open faults). Similarly, for short faults, the leakage resistance of the TSV is varied from hundreds of MΩ (fault-free case) to 10KΩ indicating strong leakage faults. The output is measured and compared with fault-free case. For comparative study, the output are normalized with respect to the nominal output for each case.

B. Evaluation of Ring Oscillator (RO)-based Fault Detection

In this section, we evaluate the performance of RO-based TSV test. The basic idea of RO-based test is to quantify the RC-delay variation in a defective TSV and compare it with fault-free ones. The connected wires and characteristics of I/Os have significant impacts on the RC-delay, thus we analyze their effects separately.

1) Effects of Wirelength

As shown in Fig. 1(b), three segments of wire connect the TSV and I/O drivers. The wirelength varies depending on the keep-out-zone (KOZ) and pitch of the TSV. If the KOZ is large and wirelength is very long, the RC-characteristics of the wire dominates over the TSV-RC delay. In addition, the types of wires (global or local) and the percentage distribution of different amount of wire segments (WL1, WL2, and WL3 in Fig. 1(b)) have significant impacts on the RC-delay as well. A simple pi-model is considered for the connected-wires with average R and C values. The distribution of the total wirelength among WL1, WL2 and WL3 is assumed to be 25%, 50% and 25% respectively. The total wirelength is varied from 0 to 200 µm. For comparative study, the variation of delay is normalized with respect to the fault-free case for each respective wirelength. *It is to be noted that to detect open and shorts faults successfully, a larger variation from the fault-free case (0 KΩ) in the output is desired.* The equivalent open resistance fault is varied from 0 to 10 KΩ to study a wide range of open faults.

From Fig. 6(a), we observe significant variation in the RC-delay for the 0 µm wirelength (without any wirelength is present between TSV and I/O). However, when we consider the connected wirelength, the variation reduces. In advanced process nodes, values of the wire R and C parameters increase significantly and affects the delay. Even for 50 µm wirelength, the variation in RC-delay reduces by more than 15% from the fault-free case for a 10 KΩ equivalent open fault. If the wirelength is increased more, the variation in RC-delay (sensitivity of the method) decreases further. As a case study, we will consider 100 µm wirelength for the rest of the experiments and analysis.

2) Effects of Wirelength and I/O Capacitance

The delay characteristics of the TSV is significantly affected by the I/O capacitances (including receiver capacitance, other parasitic capacitance, or ESD capacitance).

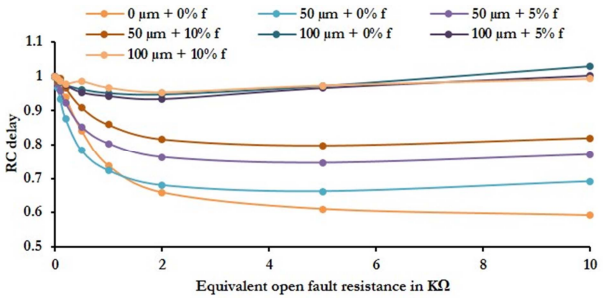

Fig. 7: Effects of wirelength and I/O capacitance on the pulse shrinkage for the PS test method.

In general the I/O capacitance values are comparable to that of the fault-free TSV. As a case study, in this work, we add only 5% and 10% of the total TSV capacitance as the input capacitance of the I/O and study their impacts. Fig. 6(b) shows the normalized variation of output RC delay for two different wirelength and different amount of input I/O capacitance.

From the figure it is demonstrated that as input I/O capacitance increases, the variation in output or the sensitivity of the SA-method diminishes. If the I/O input capacitance is increased to 10% of the TSV total capacitance value, we see that there is almost no variation from the fault-free case. Under such scenario, the SA-method will fail to distinguish any kind of faulty TSV from the fault-free one.

C. Evaluation of Pulse-Shrinkage (PS)-based Tests

For PS-based TSV test, the variation in the rise and fall time of the input voltage pulse is measured using the pulse-shrinkage cells (as shown in Fig. 3) to obtain counter outputs. Hence, for this method, we evaluate the variation in the shrinkage amount of the input pulse. Fig. 7 shows the normalized pulse shrinkage amount (normalized with respect to the fault-free case) for different amount of equivalent open-fault resistance. We have considered different amount of wirelength and input I/O capacitances similar to the SA-based approach explored earlier.

From the figure, it is seen that the variation in the output or the pulse shrinkage amount doesn't follow any predictable pattern as the equivalent open resistance increases. Two things happen here. The connected wirelength masks out small variation in the pulse shrinkage amount. The connected I/Os also impose similar effects. Thus the applicability of this method is limited in practical integration environment.

D. Evaluation of Sense Amplifier (SA)-based Tests

The SA-based approach measures the RC-delay variations for identifying the faulty TSVs. Fig. 8 shows the variation of the output delay for different amount of equivalent open fault-resistance with varying amount of wirelength. The output delay is normalized with respect to the fault-free case. From Fig. 8, it is seen that the output RC-delay decreases progressively from the fault-free case as the equivalent open-fault resistance increases. As the interconnect length increases from 0 to 100 µm, the variation reduces as expected. However, it still shows significant variations that can be captured and applied to the sampling circuit (in Fig. 4) to detect any open-defects in the TSV. Unlike the RO-based approach, the main distinction is that the RC-delay doesn't get nullified by the impact of I/Os as they are isolated by MUXes placed in front of the I/O drivers.

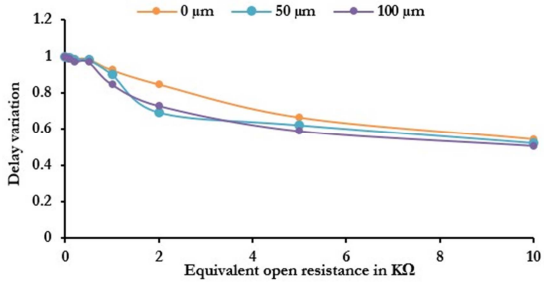

Fig. 8: Effects of wirelength on the sense amplifier sampling delay variation for SA test method.

Challenges of applicability: There are three important challenges with the SA-based approach that needs to be addressed. First, the MUX that used front of I/Os significantly reduces the bandwidth, leading to the limited applicability for high speed I/Os. Second, the performance of the sampling and output-capturing circuits need to be very precise to identify the TSV defects. The variation of delay between the fault-free and defective TSVs is in the order of few ps. In order to detect defects in the TSV, the sampling and capturing circuit need to overcome any kind PVT variations induced challenges. Finally, for both open and leakage faults, the RC-delay decreases for the SA-based tests. Hence, the method can't distinguish between open and leakage faults.

E. Evaluation of CP and PC-based Fault Detection

For the charge-pump and pulse counting-based method, the number of pulses are counted in the counter output to determine the state of the faults present in the TSV. Fig. 9 shows the variation of output counter values for different amount of wirelength and I/O input capacitances. The counter output for different equivalent open faults is normalized with respect to the fault-free case. As seen from the figure, the output counter value decreases as the equivalent open fault-resistance increases from the fault free case. The output counter value, on average, changes by 2% from the fault-free case for per KΩ open-fault resistance. In addition, even with 100 µm and 10% of the TSV capacitance as I/O capacitance, the counter output doesn't reduce much. Unlike the SA or RO methodology, the CP-PC method doesn't depend on the RC-delay. As long as the total amount of additional capacitance from the wirelength and I/Os is not bigger than the capacitance of the TSV, the method shows significant detectability.

F. Detection of Short-faults: SA vs CP-PC

From the above discussions, we found that two test methods (SA and CP-PC tests) successfully detect open defects. In this section, we evaluate the performance of these two methods for leakage-fault detection. The leakage faults are represented as

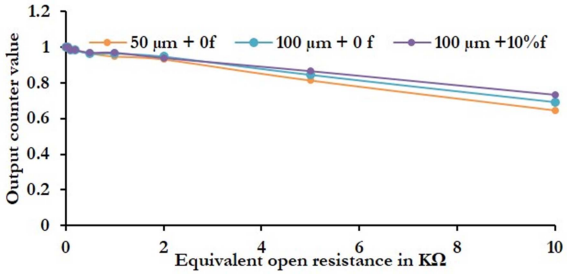

Fig. 9: Variation of normalized (w.r.t. fault-free TSV) counter output values for resistive open faults in the TSV for CP-PC method.

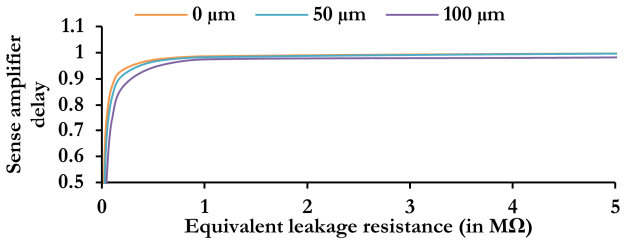

Fig. 10(a): Variation of sense amplifier sampling delay for leakage/short faults in the TSV for SA method.

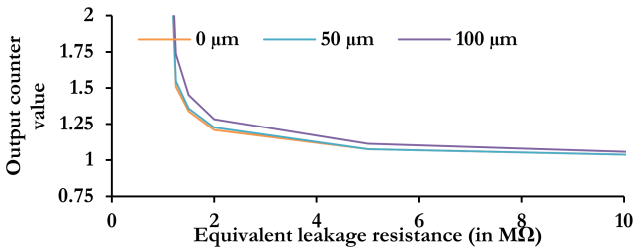

Fig. 10(b): Variation of normalized (w.r.t. fault-free TSV) counter output values for leakage/short faults in the TSV for CP-PC method

the equivalent resistance of the TSV-leg (Fig. 1(c)). Low value of leakage resistance refers to strong short or leakage faults.

Fig. 10 (a) and Fig. 10(b) show the variation of RC-delay and output counter values for different wirelength with varying amount of TSV leakage resistance for SA- and CP-PC tests respectively. As seen from Fig. 10(a), unless the leakage resistance is lowered than 0.5 MΩ, the RC-delay remains almost constant. However, if the leakage becomes stronger, delay decreases significantly (TSV discharges quickly). For a fault-free TSV, the value of leakage resistance is on the order of hundreds of MΩ. Hence, we conclude that the SA-based method can detect leakage fault only when it is catastrophic (leakage resistance is less than 0.5 MΩ). From Fig. 10(b), we see that for the CP-PC method, the counter output increases as the leakage resistance decreases. The counter output increases sharply as soon as the leakage resistances reduces to 5 MΩ. Hence, the CP-PC-based test has better leakage fault detection capability compared to the SA-based approach.

G. Overhead Comparison

We evaluate the power overhead for SA- and CP-PC tests. Depending on the shared DFT mechanism in advanced process technology node under study, the CP-PC based test consumes three times more power than the SA method. This is because, the CP-PC test uses short voltage pulses with a weak pull-up driver to charge up the TSV and requires lots of clock cycles to charge it completely. The SA-method charges the TSV directly with a pull-up transistor. The test time of the CP-PC based approach is also higher compared to the SA-based approach.

H. Comments on the Design Guidelines

From the above analysis, we summarize four key features and design guidelines for the pre-bond test methodologies. First, with practical integration environment in an advanced technology node, tests that measure the RC-delay of the TSV to determine the state of the fault are not effective to identify faulty TSVs. Second, the SA and CP-PC based approaches are the two methodologies that can detect both the open and leakage faults. However, the SA method can't distinguish between open and leakage faults. It also has lower leakage fault detection capability than the CP-PC counterpart. Third, for the high speed I/Os, the SA-based approach will reduce the bandwidth. Finally, the CP-PC-based approach has a higher power overhead and test time cost compared to SA method.

V. Conclusion.

We studied different pre-bond test schemes and classified them according to their basic principle. By considering practical design constraints, we investigated their efficacy in an advanced process technology node and found two classes out of four have limited sensitivity to identify any TSV defects. Remaining two methods can identify both leakage and open defects in the TSV, however, both of them have their own limitations. The results presented in this work provide a usage guideline of these methods.

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