

25.6 A 15Gb/s 0.5mW/Gb/s 2-Tap DFE Receiver with Far-End Crosstalk Cancellation

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The increasing demand for high-bandwidth interconnection between integrated circuits requires large numbers of I/Os per chip as well as high data rates per I/O. Key limitations in meeting these requirements include channel characteristics and I/O power consumption. Even in short interconnects, the channel attenuation at very high data rates is significant, and using receiver equalization can greatly improve the link performance [1-5]. However, compensating a high level of loss requires many taps of equalization, which can significantly reduce the power efficiency of the link. Parallel data transmission increases the aggregate data rate, but compact traces placed in close proximity suffer from a high level of crosstalk interference. This problem is exacerbated when transmit pre-emphasis techniques are exploited to boost the high frequency gain. While the use of differential signaling can mitigate the effect of crosstalk, it requires twisting pairs leading to area and bandwidth penalties.

In this paper, we present a low-power receiver that supports high data rates over bandwidth-limited and coupled links. The receiver employs a half-rate 2-tap speculative DFE architecture with a far-end cross-talk (FEXT) cancellation technique. Figure 25.6.1 shows the top-level architecture of the DFE receiver. Conventionally, analog taps of the equalizer are implemented using current-mode summers, thus the power consumption of the DFE increases proportionally with the number of taps. In the proposed architecture, a switched-capacitor S/H is employed to sample the input signal and combine it with the feedback coefficients at the front-end of the receiver [1], as shown in Fig. 25.6.2 (S/H/summer). In this design, the switched-capacitor network is modified to support two taps of DFE without any signal loss. This technique can be further extended to realize more number of taps. The extra power due to sampling capacitors, switches and voltage-mode DACs is very small. The S/H/summer operates in two phases as shown in Fig. 25.6.2. In the first, sample/sum phase, the input is sampled into capacitor C_1 and the first tap coefficient (αV_{REF1}) is added to (or subtracted from) this sample. During this phase, as will be discussed later, the crosstalk canceling signal is stored into capacitor C_2 . In the second, sum/hold phase, the result of the first phase is added to the second tap coefficient (βV_{REF2}) and applied to the slicer. A delayed version of the clock (CK_d) is used to sample the input in the first phase to minimize the input dependent charge injection. Considering the trade-off between the kT/C noise and the required RC time-constant of the S/H, the sampling capacitor is optimized to be 20fF. Two 4b current-steering DACs generate the equalization coefficients (αV_{REF1} , βV_{REF2}) while drawing <900 μ A (Fig. 25.6.2). A 1pF capacitor at the output of the DAC reduces the high frequency switching noise. A combined slicer/MUX, shown in Fig. 25.6.1, is used to implement the loop unrolling and resolve the current bit based on the previous bit. In order to cancel the kickback from latch output to the sensitive sampling nodes, small metal capacitors cross-couple the output and the input. These capacitors also reduce the loss of the S/H/summer due to the charge sharing between the sampling capacitors (C_1 , C_2) and the slicer/MUX input parasitic capacitor.

The interference from the adjacent aggressor line (FEXT) appears at the front-end of the receiver and is proportional to the derivative of the transmitted signal. The FEXT signal can have the same or opposite polarity as the aggressor signal if the link is capacitive or inductive, respectively. The incoming aggressor signal is sent through an adjustable high-pass filter, shown in Fig. 25.6.3, to approximate FEXT for different levels of coupling. This method does not involve resolving the aggressor signal to compensate for its effect on the victim signal. The effect of FEXT can be removed by addition of the mimicked FEXT signal (V_{X-TALK}) to the sampled input signal during the sum/hold phase. As addition and subtraction have minimal power overhead in this architecture, the extra hardware results in only 5% (33 μ W/Gb/s) extra power dissipation, primarily due to the additional clock buffers. As the effect of FEXT signal and the mimicked FEXT signal are sampled at the same time, this scheme is not sensitive to the phase offset between the aggressor and the victim. The measurements were performed for varying lengths of the victim and the aggressor traces to prove this fact. The

design in [6] cancels the crosstalk-induced jitter but it does not compensate for the crosstalk-induced amplitude ISI and consumes 80mW and occupies 0.014 μ m².

The prototype is fabricated in 45nm SOI technology. Figure 25.6.6 shows the performance of this design and compares it to a DFE-IIR receiver for Si carrier channel compensation [2], an FFE-DFE receiver [3] and 5- and 2-tap current-integrating DFE receivers [4, 5]. To evaluate the performance of the receiver at high data rates, first an input data with low level of ISI was used. The receiver operates error-free (BER<10⁻¹²) up to 20Gb/s with an input sensitivity of ± 100 mV_{ppd} which reduces to ± 50 mV_{ppd} at 15Gb/s. The input-referred offset was measured to be 20mV at 15Gb/s. The equalization capability of the receiver was tested by transmitting data over 5, 10 and 20inch FR-4 PCB traces. The channels characteristics including the connecting SMA cables are shown in Fig. 25.6.3. With 15Gb/s PRBS7 data, the received eye is closed for all these channels. The closed eyes are shown as insets in Fig. 25.6.4. The 5inch channel exhibits a loss of 14.5dB at 7.5GHz. Employing the 2-tap DFE, while consuming 7.5mW from a 1.2V supply, 34% horizontal eye opening (BER=10⁻⁸) with BER<10⁻¹² in the center is achieved. The DFE receiver, consisting of clock buffers, S/H/summer, slicer/MUX and DACs, occupies an area of 220 \times 65 μ m². The DFE was also tested with 10 and 20inch channels. 13Gb/s data was transmitted over the 10inch channel with 17dB of loss at 6.5GHz. Under these conditions the DFE achieved 43% horizontal eye opening while dissipating 6.1mW. Over a 20inch link with 21dB roll-off at 5.5GHz the DFE receiver operates at 11Gb/s with a 37.5% eye opening while consuming 5.5mW.

The crosstalk cancellation scheme is evaluated by transmitting uncorrelated victim and aggressor data over a 5inch long, 32mil-wide coupled trace with 40mil separation on an FR-4 board. The amount of coupling (FEXT) at 6.25GHz is -15dB (Fig. 25.6.3). The channel also has 12.5dB of loss at 6.25GHz, which results in a closed input eye. With no aggressor, the DFE generates a 47.5% open eye at BER<10⁻⁸. Applying the aggressor closes the eye completely. The crosstalk canceller restores the horizontal eye opening to 24%. The table in Fig. 25.6.5 summarizes the performance of the crosstalk cancellation technique. The 2-tap DFE receiver with the FEXT cancellation capability consumes less than 0.5mW/Gb/s of power. The proposed architecture is well-suited for implementation in highly scaled technologies. Experimental results validate the feasibility of the DFE receiver for ultra-low-power high-data-rate highly parallel I/O links.

Acknowledgements:

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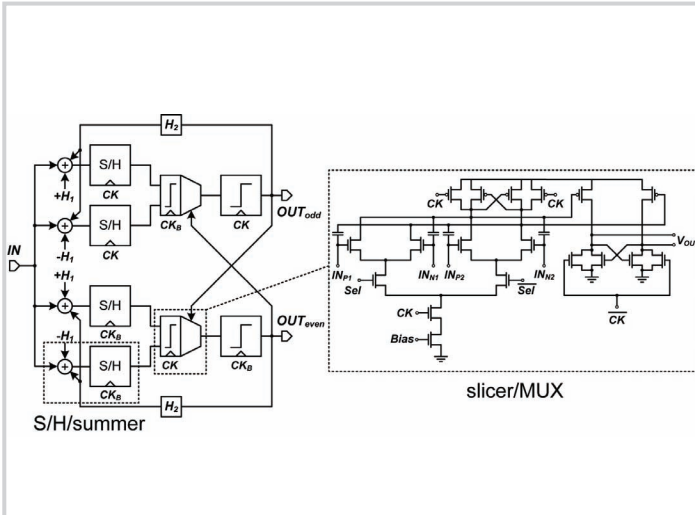


Figure 25.6.1: Top-level architecture of the 2-tap DFE, and the slicer/MUX circuit schematic.

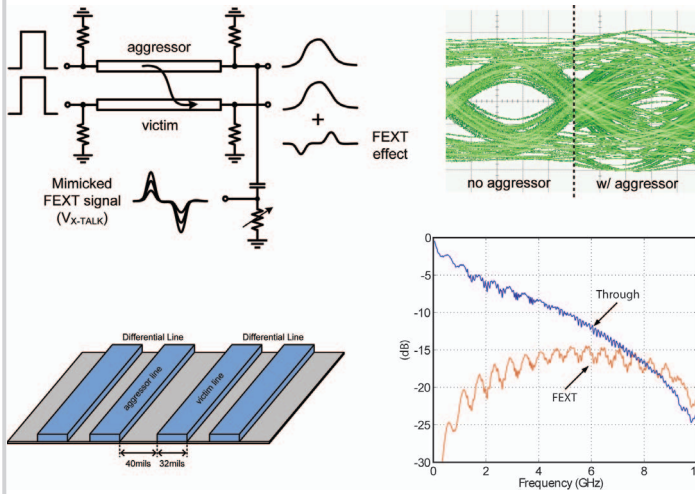


Figure 25.6.3: FEXT cancellation technique.

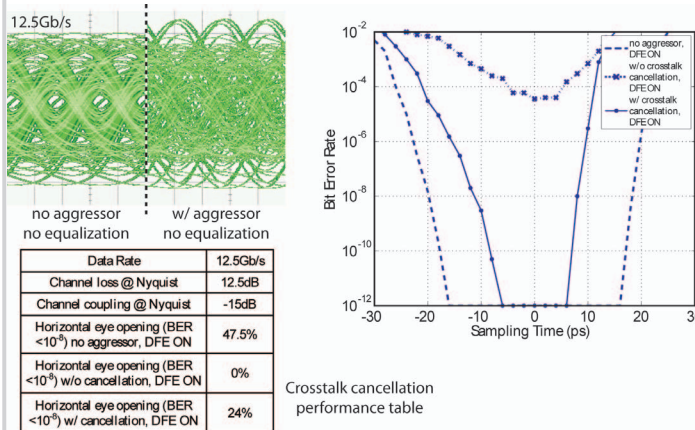


Figure 25.6.5: Crosstalk cancellation performance.

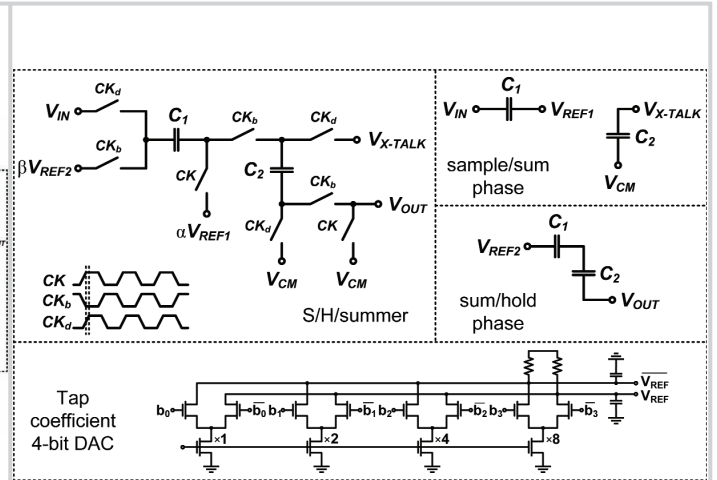


Figure 25.6.2: Front-end S/H/summer block operation (single-ended version is illustrated for simplicity), and the coefficient generating DAC.

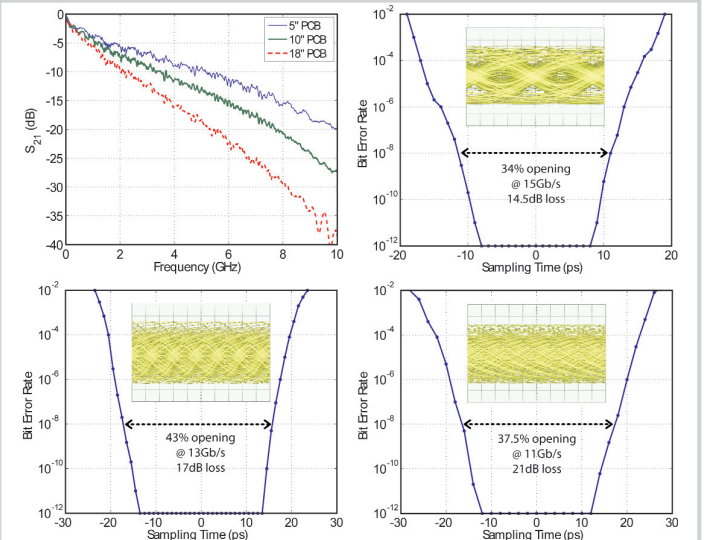


Figure 25.6.4: Channels S₂₁ plot, closed eye at the input of the receiver, and equalized bathtub curve at different data rates.

Reference	This work*	[2]	[3]	[4]	[5]			
Process	45nm SOI	65nm bulk CMOS	90nm bulk CMOS	45nm SOI	90nm bulk CMOS			
Architecture	2-tap speculative DFE	DFE-IIR	1 st -tap FFE 3-tap DFE	5-tap DFE	2-tap DFE			
Supply (V)	1.2		1.4	1.0				
Power (mW)	7.5	6.1	5.5	6.8	69	11	10.1	9.3
Data Rate (Gb/s)	15	13	11	10	16	12	9.0	7.0
Channel loss @ Nyquist (dB)	14.5	17	21	23.2	22	15	25	15
Horizontal eye opening (BER <10 ⁻⁸)	34%	43%	37.5%	45%	30%	32%	44%	45%
FOM (pJ/bit/dB)	0.034	0.028	0.024	0.029	0.196	0.061	0.045	0.088
Sensitivity	±50mV _{ppd} (20mV offset)		±32mV _{ppd}	N/A	±93mV _{ppd}		±31mV _{ppd}	
Area	0.014 mm ²		0.017mm ²	0.063mm ²	0.004mm ² **		0.019mm ²	

* Excluding FEXT cancellation

** Excluding DACs for the five taps

Figure 25.6.6: Performance summary and comparison with prior art.

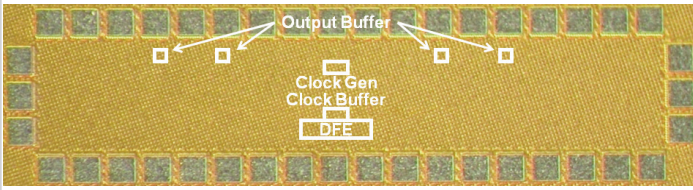


Figure 25.6.7: Die micrograph.