A Nail-size Piezoelectric Energy Harvesting System Integrating a MEMS Transducer and a CMOS Interface Circuit

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Abstract—Piezoelectric vibration energy harvesting has drawn much interest to power distributed wireless sensor nodes for Internet of Things (IoT) applications where ambient kinetic energy is available. For certain applications, the harvesting system should be small and able to generate sufficient output power. Standard rectification topologies such as the full-bridge rectifier are typically inefficient when adapted to power conditioning from miniaturized harvesters. Therefore, active rectification circuits have been researched to improve overall power conversion efficiency, and meet both the output power and miniaturization requirements while employing a MEMS harvester. In this paper, a MEMS piezoelectric energy harvester is designed and co-integrated with an active rectification circuit designed in a CMOS process to achieve high output power for system miniaturization. A MEMS energy harvester of $0.005\,\text{cm}^3$ size, co-integrated with the CMOS conditioning circuit, outputs a peak rectified DC power of $40.6\,\mu\text{W}$ and achieves a record DC power density of $8.12\,\text{mW/cm}^3$ when compared to state-of-the-art harvesters.

Index Terms—Keywords: Energy harvesting, MEMS, energy conversion, piezoelectric transducer, rectification, power conditioning.

I. Introduction

The Internet of Things (IoT) continues to expand in both number and variety and the deployment of wireless sensor networks (WSN) has been developed to interconnect the physical and cyber worlds. Harvesting ambient vibration energy for self-powered wireless sensors has received much research interest in recent years [1]–[11]. Among the various vibration energy harvesters, piezoelectricity has been widely used due to its high power density and integration with conventional CMOS circuits [12]–[14]. During real-world implementations, miniaturization of the entire integrated energy harvesting system has been one of the key challenges. In addition, the output power from miniaturized harvesters also need to meet requirements to continuously power the sensors and periodically

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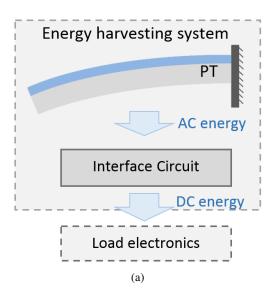
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send wireless data [15]–[17]. However, output power and the generated voltage from a miniaturized piezoelectric transducer (PT) are usually much lower than macroscopic PTs. Hence an efficient interface circuit is needed to increase the power extraction efficiency while ensuring that miniaturization benefits are not compromised [18], [19]. A complete vibration energy harvesting system consists of a PT and an interface circuit, which rectifies, manages and regulates the harvested energy to provide a stable DC power supply for load electronics [20]. An system block diagram is shown in Fig. 1a and a miniaturized energy harvesting prototype is fabricated and shown in Fig. 1b. The size of the prototype is $1\,\text{cm} \times 1\,\text{cm} \times 0.4\,\text{cm}$ and it consists of a cantilevered MEMS (Microelectromechanical Systems) PT, a CMOS interface circuit, an inductor and several capacitors.

In order to rectify the raw power generated from a PT, a full-bridge rectifier (FBR) is widely employed due to its simplicity and stability [20], [21]. Fig. 2a shows the circuit diagram of a full-bridge rectifier and the associated waveforms. The PT while vibrating is modeled as a current source I_P in parallel with a capacitor C_P. Power rectification is typically achieved by a FBR, which consists of four diodes, into a storage capacitor C_S. The signal V_{PT} in the waveform is the voltage across the PT. From the waveform, it can be seen that V_{PT} needs to attain either $V_S + 2V_D$ or $-(V_S + 2V_D)$ in order to transfer energy into C_S, where V_D is the forward voltage drop of the diodes. Hence, V_{PT} needs to be flipped between these two voltage levels for each half period and the energy used to flip V_{PT} is wasted, which is illustrated as fully shaded areas in the I_P graph. Assuming the open-circuit voltage amplitude generated from the PT is V_{OC}, the condition for a FBR to start operating is:

$$V_{OC} > V_S + 2V_D \tag{1}$$

If equation (1) is not satisfied, all generated energy is wasted (internally dissipated in the harvester front-end). Even if it is marginally satisfied, most of energy is wasted and the power efficiency is extremely low in this case. A FBR may have acceptable power efficiency while employing a macroscopic PT, which can generate relatively high open-circuit voltage. However, MEMS (microelectromechanical system) energy harvesters have been widely employed for miniaturization in the past decade [22]–[25]. if a MEMS PT is employed, the generated voltage can be much lower. For example, assuming
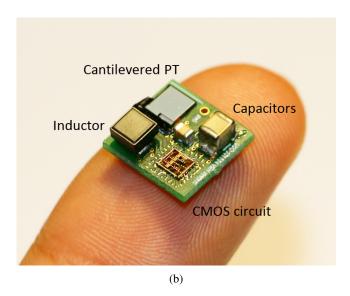
(a)

(b)

Fig. 1: System block diagram and a fabricated prototype of a complete vibration energy harvesting system (a) system block diagram (b) prototype of size $1\,\text{cm} \times 1\,\text{cm} \times 0.4\,\text{cm}$.

(a)
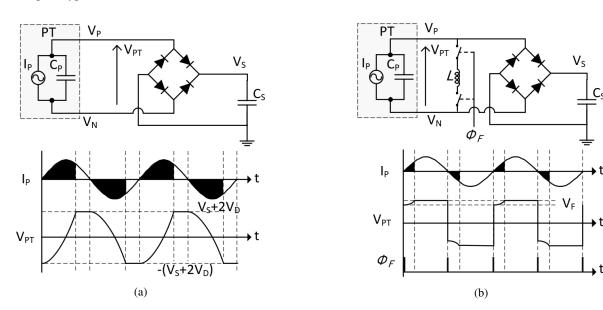
(b)

Fig. 2: (a) Full-bridge rectifier and associated waveforms. (b) SSHI circuit and associated waveforms.

$V_S = 3\,\text{V}$ and $V_D = 0.3\,\text{V}$, V_{OC} needs to attain $3.6\,\text{V}$ (or $7.2\,\text{V}$ peak-to-peak) to be able to turn on the diodes, which can be difficult to achieve for a MEMS PT at low vibration levels. Therefore, in order to increase the extracted power, many active interface circuits have been proposed in recent years [26]–[36]. Most of these circuits employ inductors and synchronous switches to perform nonlinear energy extraction, such as synchronized switch harvesting on inductor (SSHI), synchronous electric charge extraction (SECE), etc [37]–[45].

In this paper, a MEMS PT is fabricated and integrated with a SSHI interface circuit implemented in a $0.35\,\mu\text{m}$ CMOS process. The system shows a significant performance improvement while using the SSHI circuit on the MEMS harvester compared with using a FBR rectifier and it provides useful rectified DC power and system integration in a compact volume ($0.4\,\text{cm}^3$).

II. OUTPUT POWER MODELING

A. Full-bridge rectifier

This section models the full-bridge rectifier (FBR) and analyzes the the DC power transferred into the capacitor C_S. The circuit diagram of a FBR is shown in Fig. 2a. While the PT is vibrating, the current source can be expressed as $I_P = I_0 \sin(\omega t)$, where ω is the excitation frequency. Hence, the charge generated in a half period is:

$$Q_{total} = \int_0^{\frac{T}{2}} I_0 \sin \omega t \mathrm{d}t = \frac{2I_0}{\omega} \quad (2)$$

If the PT is in an open circuit, the open-circuit zero-peak amplitude can be calculated as:

$$V_{OC} = \frac{1}{2}\frac{Q_{total}}{C_P} = \frac{I_0}{\omega C_P} \quad (3)$$

As a certain amount of charge is wasted to flip V_{PT} between $V_S + 2V_D$ and $-(V_S + 2V_D)$, the remaining charge transferred into C_S can be expressed as:

$$Q_{FBR} = Q_{total} - 2(V_S + 2V_D)C_P \quad (4)$$

Hence, the energy flowing into C_S is:

$$E_{FBR} = V_S Q_{FBR} = 2C_P V_S(V_{OC} - V_S - 2V_D) \quad (5)$$

Therefore, the extracted power in this half period is:

$$P_{FBR} = \frac{E_{FBR}}{T/2} = 4C_P V_S f_P(V_{OC} - V_S - 2V_D) \quad (6)$$

It can be found that the maximum power point (MPP) of P_{FBR} is obtained when $V_S = \frac{V_{OC}}{2} - V_D$. The peak power transferred to C_S is:

$$P_{FBR(max)} = 4C_P f_P(\frac{V_{OC}}{2} - V_D)^2 \quad (7)$$

Assuming the forward voltage drop of the diodes, V_D, is ignorable, the peak power can be rewritten as:

$$P_{FBR(max)} = C_P f_P V_{OC}^2 \quad (8)$$

B. SSHI circuit

In order to minimize the wasted charge due to flipping the voltage V_{PT} across the PT, the synchronized switch harvesting on inductor (SSHI) interface circuit has been proposed and implemented to increase the power extraction efficiency [44]. The circuit diagram and the associated waveforms are shown in Fig. 2b. In the SSHI rectifier, an inductor is employed to form an RLC oscillation loop to flip V_{PT}. The pulse signal ϕ_F is synchronously generated and its pulsewidth is adjusted to be a half-pseudo period of the RLC system. During the pulse ϕ_F, V_{PT} is flipped with a loss V_F, which can be expressed as:

$$V_F = (V_S + 2V_D)(1 - e^{-\frac{\pi}{\sqrt{\frac{4L}{R^2 C_P} - 1}}}) = (V_S + 2V_D)\eta_F \quad (9)$$

where the threshold V_F is illustrated in Fig. 2b, which represents the voltage loss after one flip. R is the total resistance in the RLC loop, which consists of the DC resistance of the inductor, the ON resistance of switches and other parasitic resistance in wires and contacts. η_F is the voltage loss ratio between 0 and 1 and it is expressed as $\eta_F = 1 - e^{-\frac{\pi}{\sqrt{\frac{4L}{R^2 C} - 1}}}$. As V_F is the voltage loss after one flip in a half period, the remaining charge flowing into C_S is:

$$Q_{S(SSHI)} = Q_{total} - C_P V_F = C_P(2V_{OC} - V_F) \quad (10)$$

Hence, the extracted power is:

$$\begin{aligned} P_{SSHI} &= 2f_P C_P V_S(2V_{OC} - V_F) \\ &= 2f_P C_P V_S(2V_{OC} - (V_S + 2V_D)\eta_F) \end{aligned} \quad (11)$$

The power attains its MPP when $V_S = \frac{V_{OC}}{\eta_F} - V_D$ and the maximum power can be calculated as:

$$P_{SSHI(max)} = 2C_P f_P \eta_F(\frac{V_{OC}}{\eta_F} - V_D)^2 = \frac{2}{\eta_F} C_P f_P V_{OC}^2 \quad (12)$$

where V_D is ignored. Comparing the MPP values in equations (8) and (12), the performance improvement of using a SSHI circuit compared to a FBR can be expressed as:

$$\frac{P_{SSHI}}{P_{FBR}} = \frac{2}{\eta_F} \quad (13)$$

It can be found that the performance improvement does not depend on excitation level (V_{OC}), but η_F. Hence, we need to increase L or decrease C_P or R to obtain a higher performance from a SSHI circuit. The inductance L can be increased in a wide range of inductor selections; however, the DC resistance on an inductor should always be considered since larger L in a given volume usually introduces higher DC resistance. The resistance R can be decreased from the inductor selection and the design of the circuits, especially the analogue switches controlling the inductor shown in Fig. 2b. The C_P is the inherent capacitance of the PT; hence, it can only be deceased during MEMS design.

III. SSHI CIRCUIT IMPLEMENTATIONS

This section presents the circuit implementation of a SSHI rectifier and the system architecture is shown in Fig. 3, which consists of a zero-crossing detection block, a pulse generation block and two analog switches. The full bridge rectifier is formed by four off-chip Schottky diodes and the forward voltage drop is around $V_D \approx 0.3\,\text{V}$. The zero-crossing block aims to find the zero-current moment of I_P, which is the right moment to flip V_{PT}. In order to find this moment, two continuous-time comparators are employed to compare the both electrodes of the PT, V_P and V_N, with a reference voltage V_{ref}. While I_P is close to zero, the diodes of the FBR are just about to turn OFF. At this moment, one of V_P and V_N is close to $-V_D$ and the other one is close to $V_S + V_D$. The reference voltage V_{ref} is set slightly higher than $-V_D$ to detect the moment while one of V_P and V_N leaves $-V_D$ and this is the moment while I_P is close to zero. The outputs of the two comparators are ANDed and the signal SYN is a synchronous signal which consists of a rising edge at each zero I_P moment. A pulse signal ϕ_F is then generated according to each rising edge of SYN to control the analog switches to flip V_{PT}. The pulse of ϕ_F should be adjusted to be a half pseudo-period of the RLC oscillation system to achieve the maximum voltage flipping efficiency.

The pulse generation block aims to generate the fixed-width pulse signal, ϕ_F from SYN and the circuit diagram is shown in Fig. 3. This pulse generator is a AND gate where the signal SYN is ANDed with the delayed and inverted version of itself. The delay is achieved using two weak inverters charging up capacitors. The total capacitance formed by 6 on-chip capacitors can be adjusted by a 6-bit signal controlling the six switches C_5 to C_0. This 6-bit signal can be set externally
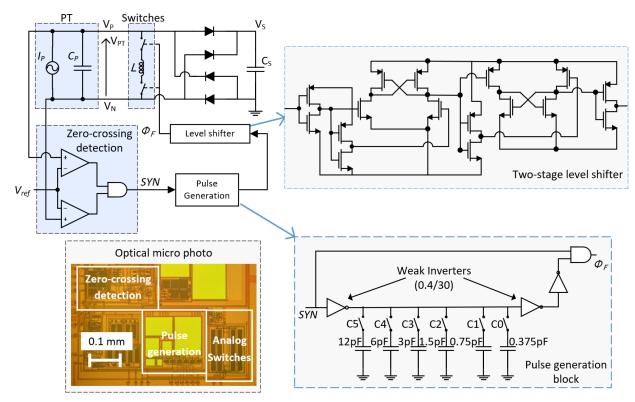
Fig. 3: SSHI circuit system architecture and circuit implementations.

to adjust the capacitance. With the help of this block, a pulse ϕ_F is generated with its pulsewidth adjusted to a half pseudo-period of the RLC oscillation loop, which approximately equals to $2\pi\sqrt{LC}$. This pulse signal then closes the RLC loop to flip the voltage V_{PT}. The next section presents the design and the modeling of a piezoelectric energy harvester in MEMS process, which is integrated with the CMOS SSHI circuit in following experiments for power measurements. The SSHI is designed and fabricated in $0.35\,\mu$m HV CMOS process and the optical die photo is shown in Fig. 3. The active area of the SSHI circuit is around $0.15\,\text{mm}^2$.

IV. MEMS VIBRATION ENERGY HARVESTER

The MEMS vibration energy harvester employed for the integration was an in-house device developed using the most fundamental cantilever topology and an AlN (aluminum nitride) on SOI (silicon on insulator) process.

The FEA (finite element analysis) simulation of the 3.5 mm wide and long cantilever design is shown in figures 4a to 4c. The fundamental mode resonant frequencies of the micro-cantilever where 50% of the beam length is occupied up by end mass is predicted at 202 Hz as shown in figure 4a.

The micro-cantilevers can be driven to experience approximately 300 MPa of peak stress (a typical design limit for silicon resonators) at 120 g of acceleration loading on the shuttle mass and a peak displacement amplitude of about 1 mm as shown in figure 4b. This level of shuttle travel is relatively large for typical MEMS oscillators, which requires a deep cavity chip carrier to accommodate the silicon device. The induced stress across the beam length is shown in figure 4c

The MEMS fabrication process is shown in Fig. 4d. The fabricated devices were made up of a stack of materials consisting of: 10 μm thick doped silicon as the device layer with 0.5 μm thick AlN piezoelectric layer on top and a further 1 μm thick Al top electrode layer on top of AlN. The proof mass was achieved using un-etched regions of the 400 μm thick silicon handle wafer underneath the device silicon. The device is placed in a custom laser-cut, leadless chip carrier for testing.

V. EXPERIMENTS

This section presents the measured output power of the MEMS cantilevered PT with a resistive load, a full-bridge rectifier (FBR) and a SSHI circuit. First, the mechanical specifications, optimal resistive load and AC output power consumed in a matched resistive load are measured. The cantilevered MEMS PT is assembled into a custom laser-cut leadless chip carrier (LCC44); the chip carrier and the MEMS cantilever are shown in Fig. 1b. During the measurements, the chip carrier containing the PT is placed on a shaker excited at the natural frequency of the PT. In order to measure the AC output power consumed in a impedance-matched resistive load, the natural frequency should first be found. Fig. 6a shows the measured open-circuit voltage amplitude, noted as V_{OC}, over a range of excitation frequencies. From this figure, the natural frequency of the micro cantilever is found to be around 199 Hz. After finding the natural frequency, the PT is then excited at its resonance and connected to a variable resistor to find the optimal resistive load matching the internal impedance of the PT. The power consumed in the variable resistor is
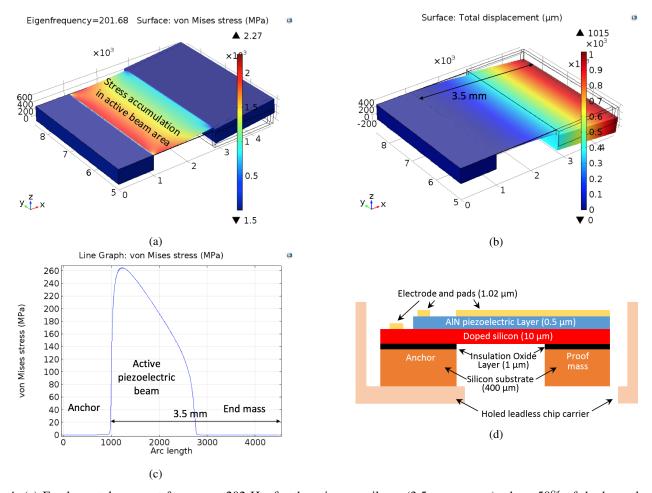
(a)

(b)

(c)

(d)

Fig. 4: (a) Fundamental resonant frequency, 202 Hz, for the micro-cantilever (3.5 mm square) where 50% of the beam length is occupied by end mass. (b) Peak displacement of ∼1 mm for the micro-cantilevers when driven to a peak stress of 300 MPa with 120 g response acceleration loading on the shuttle mass. (c) Induced stress distribution along the cantilever length. (d) A cantilevered MEMS PT with MEMS process showing different layers with corresponding thickness.
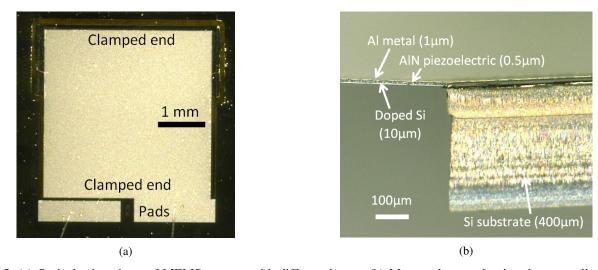

(a)

(b)

Fig. 5: (a) Optical microphoto of MEMS process with different layers. (b) Measured open-circuit voltage amplitude.
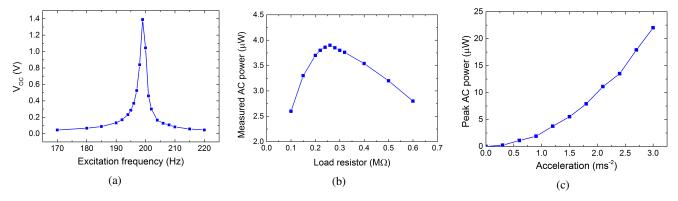
Fig. 6: (a) Measured output power in different resistive loads ($V_{OC} = 2\,\mathrm{V}$). (b) Measured AC peak power consumed in a $260\,\mathrm{K\Omega}$ resistive load. (c) Measured peak AC power for different acceleration levels.

calculated and the results are shown in Fig. 6b. The resistance is swept from $100\,\mathrm{k\Omega}$ to $600\,\mathrm{k\Omega}$ and the AC power is found to attain its peak while the load is at around $260\,\mathrm{k\Omega}$. Then, the load resistor is kept at $260\,\mathrm{k\Omega}$ by changing the excitation level to find the AC output power under different excitation levels. The results are shown in Fig. 6c and the peak AC output power is found to be $22.1\,\mu\mathrm{W}$ at $3\,\mathrm{m/s^2}$.

The MEMS PT is then integrated with a FBR and a SSHI circuit to measure the rectified DC power. The FBR is implemented with four off-chip Schottky diodes and the SSHI circuit is implemented in a CMOS process. The forward voltage drop of the diode is measured at around $0.2\,\mathrm{V}$. Fig. 7 shows the measured waveforms of signals V_{PT}, SYN and ϕ_F while using the FBR and using the SSHI circuit with three different inductor values. While using a passive FBR, the voltage V_{PT} is slowly flipped by the generated energy to overcome the thresholds. In this case, most of generated energy is wasted and only the energy while the V_{PT} attains its top and bottom limits can be extracted. In the following three figures, the SSHI circuit is employed with different inductor values. It can be seen that the voltage V_{PT} is correctly flipped for this half period and the signal SYN is synchronously generated to flip V_{PT}. While using an inductor with higher inductance, the voltage flipping efficiency is increased, which has been studied in equation (9).

Fig. 8a shows the output power under a given excitation level while varying the output DC voltage V_S, which is the voltage across the energy storage capacitor C_S connected at the output of the FBR and the SSHI circuit. During the measurements, the excitation level is $1.2\,\mathrm{m/s^2}$, which corresponds to an open-circuit voltage amplitude at $V_{OC} = 2\,\mathrm{V}$. Under this excitation level, the FBR can achieve its MPP (maximum power point) while $V_S = 0.9\,\mathrm{V}$ and the peak power is $1.8\,\mu\mathrm{W}$. While integrating the SSHI circuit with a $0.1\,\mathrm{mH}$ inductor, the peak power is increased to $6.2\,\mu\mathrm{W}$ when $V_S = 3\,\mathrm{V}$. The peak output power achieves $8.8\,\mu\mathrm{W}$, $11.6\,\mu\mathrm{W}$ and $14.1\,\mu\mathrm{W}$ while the inductor is chosen at $220\,\mu\mathrm{H}$, $470\,\mu\mathrm{H}$ and $1\,\mathrm{mH}$, respectively. Compared to the FBR, the output power of integrating the SSHI with the MEMS energy harvester is increased by $3.4\times$, $4.9\times$, $6.4\times$ and $7.8\times$, respectively, under the $1.2\,\mathrm{m/s^2}$ excitation with a $1\,\mathrm{mH}$ inductor. According to the performance improvement equation obtained

in (13), the voltage flip loss ratios for these four inductor values can be calculated as $\eta_{0.1\,\mathrm{mH}} \approx 0.59$, $\eta_{0.22\,\mathrm{mH}} \approx 0.41$, $\eta_{0.47\,\mathrm{mH}} \approx 0.31$ and $\eta_{1\,\mathrm{mH}} \approx 0.25$, respectively. Comparing with the waveforms obtained in Fig. 7, the measured voltage flip losses for different inductor values approximately match the theoretical values obtained with (13).

Fig. 8b shows the output power under a range of excitation levels up to $3\,\mathrm{m/s^2}$, which corresponds to an open-circuit voltage of $V_{OC} = 5.2\,\mathrm{V}$. During the measurements, the output voltage is fixed at $V_S = 4\,\mathrm{V}$. From the results, it can be seen that the FBR can only extract energy under high excitation levels from $2.5\,\mathrm{m/s^2}$ as it sets a high threshold due to the high V_S value. Hence, the peak output power while using a FBR is only $7\,\mu\mathrm{W}$. While the SSHI circuit is employed, the output power is significantly increased to $32\,\mu\mathrm{W}$ with a $100\,\mu\mathrm{H}$ inductor. This value is further increased to $40.6\,\mu\mathrm{W}$ with a $1\,\mathrm{mH}$ inductor due to higher voltage flipping efficiency. Therefore, the SSHI circuit improves the energy extraction performance by $5.8\times$ compared to the FBR.

Table I compares the work presented in this paper with prior publications. The second column shows the techniques used in each work and the following columns show the piezoelectric transducers used in experiments, operating frequency, internal capacitance of PTs, peak output power and the volume of PTs, respectively. The last column shows the power density ($\mathrm{mW/cm^3}$) by dividing the peak output power by the PT size. From the table, it can be found that the proposed the work presented in this paper shows the highest power density at $8.12\,\mathrm{mW/cm^3}$, which is higher than all other prior cited works. The high power density is achieved due to the custom MEMS PT and the highly efficient SSHI interface circuit. The compact design of the energy harvesting system also allows it to be implemented in miniaturized self-powered systems.

VI. CONCLUSION

This paper presents the integration of a MEMS piezoelectric energy harvester and a CMOS SSHI interface circuit to provide a peak DC output power of $40.6\,\mu\mathrm{W}$ with a record power density at $8.12\,\mathrm{mW/cm^3}$. The piezoelectric transducer (PT) is fabricated in a MEMS process with AlN as the piezoelectric material and the CMOS circuit is implemented in a $0.35\,\mu\mathrm{m}$
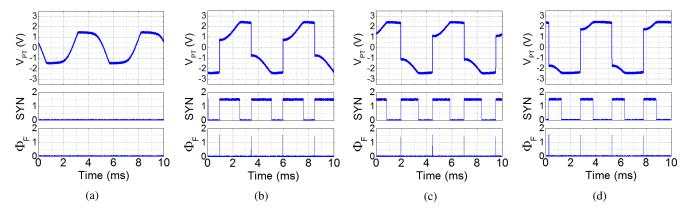
Fig. 7: (a) Full-bridge rectifier ($V_{OC} = 2.5\,\text{V}$, $V_S = 1\,\text{V}$). (b) SSHI circuit with $100\,\mu\text{H}$ inductor ($V_{OC} = 2\,\text{V}$, $V_S = 2\,\text{V}$). (c) SSHI circuit with $220\,\mu\text{H}$ inductor ($V_{OC} = 2\,\text{V}$, $V_S = 2\,\text{V}$). (d) SSHI circuit with $1000\,\mu\text{H}$ inductor ($V_{OC} = 2\,\text{V}$, $V_S = 2\,\text{V}$).
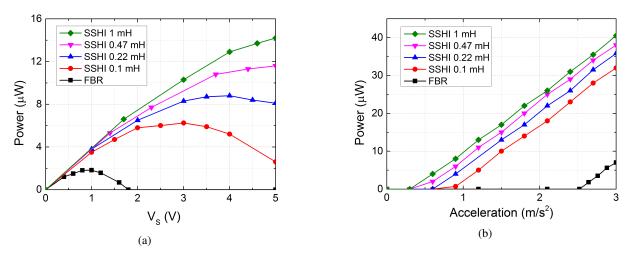

Fig. 8: (a) Measured output power using FBR and SSHI circuits with different inductor values in a range of V_S values with $V_{OC} = 2\,\text{V}$. (b) Measured output power using FBR and SSHI circuits with different inductor values in a range of excitation levels from $0\,\text{m/s}^2$ to $3\,\text{m/s}^2$ with $V_S = 4\,\text{V}$.

HV (high-voltage) CMOS process. Due to the integration of a MEMS PT and a CMOS circuit, the overall system volume of an energy harvesting system can be significantly decreased to sub-cm^3 scale including all off-chip components. In addition, with the MEMS PT and the CMOS circuit, the measured DC output power is as high as $40.6\,\mu\text{W}$ with the power improvement of $5.8\times$ compared to a passive FBR. This demonstration shows a pathway towards miniaturized vibration-powered wireless sensor solutions as an enabling technology for the Internet of things paradigm.

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TABLE I: Performance comparison with state-of-the-art

Reference	Technique	Piezoelectric transducer	Frequency	Piezoelectric capacitance	Peak power	PT size	Power density
[37]	SSHI	Mide V22B	225 Hz	18 nF	$68\,\mu$W	0.185 cm^3	0.37 mW/cm^3
[34]	SSHC	Mide V21BL	92 Hz	45 nF	1.2 mW	0.59 cm^3	2 mW/cm^3
[46]	PSCE	Mide V22B	173 Hz	19.5 nF	$477\,\mu$W	0.185 cm^3	2.58 mW/cm^3
[44]	SSHI	Custom MEMS	155 Hz	8.5 nF	$95\,\mu$W	0.027 cm^3	3.5 mW/cm^3
[32]	SSHI	Mide V22B	134 Hz	26 nF	$500\,\mu$W	0.185 cm^3	2.7 mW/cm^3
This work	SSHI	Custom MEMS	199 Hz	2.82 nF	$40.6\,\mu$W	0.005 cm^3	8.12 mW/cm^3

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