An Enhanced Planned Obsolescence Attack by Aging Networks-on-Chip

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Abstract—Despite of a controversial practice, having the key components of a product undergo accelerated aging has been a very effective approach for planned obsolescence. All previous studies on planned obsolescence merely focused on the aging process itself; however, if a malfunctioned product due to aging is still under its warranty, the manufacturer suffers from financial losses in the form of customer refund and/or product repair. In this paper, we reveal an enhanced planned obsolescence attack that takes the warranty issue into consideration. More specifically, aging of an NoC-based many-core chip is set to be slow before the warranty expires, and its aging process gets accelerated afterwards. Such controlled aging is achieved by manipulating the routing algorithm that influences the lifetime distribution of the NoC nodes. The routing-induced aging process is also integrated with a profit model to evaluate the profit gained from chip aging. Experimental results show that, with the proposed planned obsolescence attack and the profit model, the manufacturer can increase its profit margin by 15.54%, 25.69%, and 53.36%, respectively, compared to devices under a scheme without any attack, a scheme that aggressively accelerates chip aging, and a scheme that employs a measure to mitigate chip aging. Overall speaking, the proposed attack can give the manufacturer a clear advantage over customer who can barely notice the existence of such business practices, and consequently, some advanced countermeasure schemes need to be developed to balance the interests of the two parties.

Index Terms—Planned obsolescence, aging, networks-on-chip (NoCs)

1 Introduction

Planned obsolescence in industrial design and marketing is a notorious strategy to deliberately set product to malfunction within a certain period of time [1]. Quite a few consumer electronics vendors have been reported of engaging in such practice of obsolescence by downgrading their old products to drive customers to move to their newer versions of products [1].

A manufacturer often favours this type of obsolescence by either deliberately crafting malicious programs or inserting hardware backdoors that can be exploited to accelerate aging of key components, such as cores and some of the critical links in many-core chips [1], [2]. For many-core systems connected by networks-on-chip (NoCs), aging the interconnection is more destructive than wearing out the cores [3], [4]. A fault in one core might not result in failure of the entire chip, as the problem can be tackled by scheduling the affected tasks to other fault-free cores to take advantage of high degree of redundancy in a many-core chip. However, the malfunction of key component in NoCs, like a critical router which carries most traffic or connects to the memory controllers, may render the whole system faulty, even though each core may still be working as expected. Up to date, there are few research works tackling planned obsolescence attacks on NoC routers [1], [2]. The work presented in this paper thus attempts to study such attacks from the viewpoint of the most critical routers in NoC, the so-called hotspot nodes.

Targeting a hotspot node and making it age faster can certainly cause a product to obsolete fast. However, if the chip wears out before its warranty expires, the manufacturer is obligated to refund consumers or replace/repair the product, which undermines the purpose of planned obsolescence. In a simple word, blindly accelerating aging does not serve the best interest of the manufacturer. Instead, manufacturer prefers to have its component/product work perfectly at the customer end when it is still under the warranty, but it would wear out as soon as the warranty expires. Fig. 1 shows the expected behavior of the chips from the manufacturer's perspective. The lifetime of a chip is here determined by the variation of transistor threshold voltage, ΔV_{th}, which gradually increases as the aging of the transistors [2]. When ΔV_{th} exceeds an acceptable threshold, it may introduce serious timing violations that will cause the chip to malfunction [5]. For a manufacturer, the planned obsolescence curve (the blue curve) is thus preferred, and the aggressive aging curve (the green curve), on the other hand,

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really hurts the manufacturer by eroding its profitability and reputation.

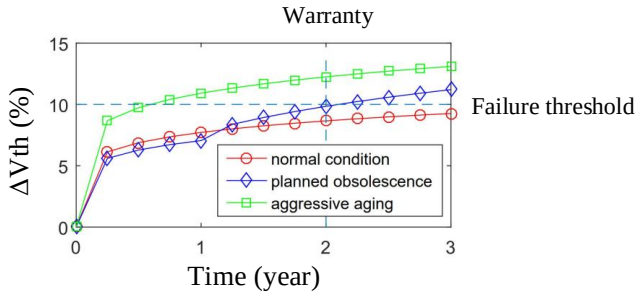


Fig. 1. Different scenarios of aging.

In this paper, we integrate the planned obsolescence attack with a profit model. We study how the manufacturer can maximize its profit by designing an improved planned obsolescence attack that both exploits the vulnerability of chip aging and considers the warranty period. We target the hotspot nodes among the NoC routers as failure of such a node causes the whole chip to disconnect and malfunction. The routing algorithm is used as the control knob to either accelerate or decelerate aging of NoC due to the stealthiness of the routing algorithm (further analyzed in Section 2.4). With the warranty in mind, the manufacturer sees modest aging process before a specific time as defined by the warranty (further analyzed in Section 5.2.2), the aging process is accelerated after it is past the time threshold.

The contributions of the paper are fourfold.

- A profit model is built to determine the profit of the manufacturer. The variables are drawn from the statistics of questionnaires or random variables.
- The routing algorithms for both aging acceleration and deceleration are proposed. Targeting the vulnerability of NoCs, the proposed algorithms accelerate or decelerate aging while keeping the minimal routing of the packets.
- Experimental results show that the proposed aging acceleration routing algorithm decreases the mean time to failure (MTTF) of the hotspot node by about 47.54%, and the proposed aging deceleration routing algorithm increases the MTTF of the hotspot node by about 18.46%.
- Experimental results show that the profit with the proposed planned obsolescence attack is 15.54%, 25.69%, and 53.36% higher than the normal condition, acceleration only and deceleration only schemes, respectively.

Note that the effects of a planned obsolescence attack launched by the manufacturer can be unnoticed by customers for a long period of time. One major focus of this work is thus to provide an in-depth analysis that will expose such attack to customers who otherwise will be kept in the dark. In possession of this critical knowledge, customers can take all the necessary measures or countermeasures that they are entitled to for the best protection of their interest.

The rest of this paper is organized as follows. Section 2 introduces the preliminaries and reviews the related works. Section 3 describes the manufacturer strategy. The details of the aging acceleration and aging deceleration routing algorithms are described in Section 4. Section 5 evaluates the experimental results. Finally, Section 6 concludes the paper.

2 Preliminaries and Related Work

2.1 Device Level Aging Effects

NoC suffers from various device level aging effects, including negative bias temperature instability (NBTI) [6], [7], hot carrier injection (HCI) [8], [9], and electromigration (EM) [10]. These aging effects cause transistor and/or wire links wear-out.

Negative bias temperature instability (NBTI) manifests an increase in p-type transistor's threshold voltage (V_{th}) which can be modelled by [11],

$$\Delta V_{th} = be^{-\frac{nE_a}{KT}}(\frac{\alpha}{1-\alpha})^n t^n \quad (1)$$

where b is a fitting constant, n is the time exponent, E_a is the apparent activation energy, k is the Boltzmann's constant, T is the run-time temperature, α is the duty cycle, and t is the operating time.

A direct consequence of NBTI-induced threshold shift is the decrease in transistor's drain current and transconductance, which introduces extra delay in the critical path [7]. As so, NBTI has been known as the most destructive aging effect upon NoC routers [3].

Hot carrier injection (HCI) in MOSFETs occurs when a carrier from silicon channel is injected into the gate dielectric layer [9], and it can permanently change the switching characteristics of the transistor, including V_{th} shifting and switching frequency degradation. In general, HCI poses a great reliability challenge to n-type transistors [8].

As the primary aging factor in interconnect wires [3], electromigration (EM) refers to gradual displacement of metal wire atoms. EM can cause open and short circuits and it only gets worse at advanced technology nodes as wires are progressively becoming thinner and accordingly, current densities are higher. As NoCs typically come with a large number of long and thin wires, they are susceptible to EM related aging [10].

2.2 Aging at NoCs

It has been shown in [3] that the routers in an NoC age at different paces. Consider a mesh-based NoC that supports XY routing. Routers located at the center of the chip handle more network traffic than other routers. Referred as "hotspot nodes", these centrally located routers tend to experience accelerated aging due to the exponential nature of the NBTI effect, making them the most vulnerable components of the system.

Using Alpha Power Law and the AC stress model given in Eqn. (1), the lifetime (measured by mean time to failure, MTTF) of a router is given as [4],

$$MTTF = [b_{NTBI}e^{\frac{nE_a}{KT}}(\frac{\alpha}{1-\alpha})^n]^{1/n} \quad (2)$$

where b_{NTBI} is a fitting constant.

Note that an NoC system's lifetime is bounded by the hotspot node, which is the router with the lowest MTTF

[12]. That is, the MTTF of the entire chip system, MTTF_{sys}, can be written as,

$$MTTF_{sys} = \min_{\forall i \in [1,N]} MTTF_i \quad (3)$$

where N is the number of routers.

The normalized MTTF distribution of an 8×8 2D mesh network is shown in Fig. 2 (a), where one can see that the central routers age at a much higher pace than many other routers. Besides these routers at the central locations, it can also be seen from Fig. 2 (b) that for those routers connected to the memory controller, even if they are off the central location, they qualify to become the hotspot nodes as they handle a lot of data traffic from and to the memory, and thus undergo rapid aging as well.

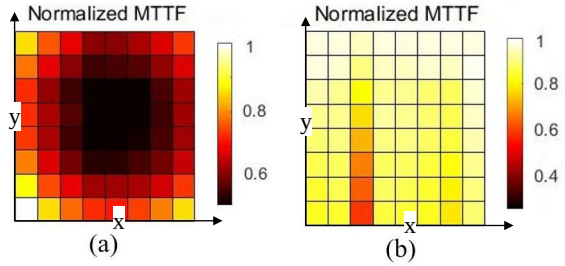


Fig. 2. (a) The hotspot nodes identified as the central routers of NoC and (b) the hotspot nodes identified as the routers directly connected to the memory controller.

Lifetime and reliability of the routers in an NoC are so such dependent on the underline routing algorithm [12]. Fig. 3 shows the routers' normalized MTTFs of two cases: the NoC adopting deterministic XY routing *vs*. the NoC adopting adaptive odd-even (OE) routing [13]. In the case of XY routing, the ratio of the highest and lowest MTTFs of the routers is 2:1, while this ratio jumps to 2.5:1 in the case of OE routing. Apparently, a routing algorithm can have a noticeable impact on the hotspot router's MTTF, and accordingly, it impacts the reliability of the entire chip in the way suggested in Eqn. (3).

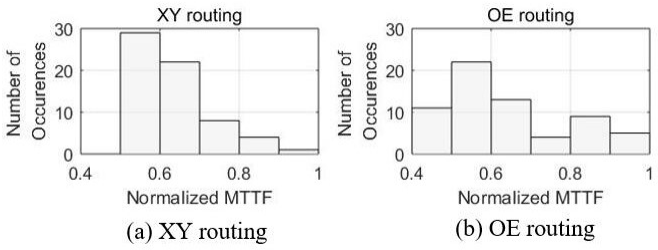


Fig. 3. The routers' MTTFs under two routing algorithms (a) XY and (b) OE routing, respectively.

In the literature, aging-aware adaptive routing algorithms [12], [14] have been proposed to slow down the aging of NoCs. The basic idea is to distribute the traffic uniformly across all the routers, to avoid overburdening a few hotspot routers. LAXY [3] is an oblivious routing algorithm that statically partitions the NoCs routers into two classes, and routers in each class adopt their own routing algorithms. Doing so will help balance the network traffic and consequently mitigates routers' aging.

2.3 Aging Attack on NoCs

Malicious users or intended manufacturers can launch attacks to deliberately accelerate chip aging. There are a few techniques and approaches that are available to achieve accelerated aging. Targeting circuit logic components, Karimi *et al*. [2] crafted a malicious program that generates identified input patterns to expedite aging in the pipeline stages of a core. Although this type of aging attack can cause a few processors to age prematurely, its effects are still limited due to high degree of redundancy in many-core systems. When a processor core is down, its role can be simply and quickly replaced by many others.

Aiming at the memory hierarchy wear out, Patrick *et al*. [15] developed an attack that causes inconsistency in nonvolatile flip-flops in the repeating checkpointing process by interrupting the power supply. Wearing out the memory leads to malfunction of the corresponding core, but it still can be solved by task scheduling in NoC.

Unlike processor cores and memory, NoC, as the communication backbone to connect all the processor cores, is a perfect target for aging. Bringing down even a small fraction of the NoC can have devastating effect on the entire chip. Aging the TSV interconnect in NoC has been suggested in [1], while this technique is limited to 3D IC only. A more catastrophic effect can be achieved by aging routers, as malfunction in one router can be amplified by impacting all the processors and the neighboring routers that it directly connects to.

Since router is an essential component, but happens to be a more vulnerability component in an NoC, this paper focuses on routers considered as the hotspot nodes to be the aging attack targets. As alluded before, the routing algorithms can be explored to either accelerate aging (making most traffic traverse the hotspot node) or decelerate aging (evenly distributing network traffics among all the routers), routing computation of routers can be maliciously elaborated. A manufacturer controls the chip aging by launching this type of aging attack to maximize the profit.

2.4 Stealthiness of Aging Attack

Various denial of service (DoS) attacks targeting NoC routers or links [26], [27] have been studied in the literature. These DoS attacks target either the data packet to be delivered directly or the routing paths. In some cases, packets might get dropped, or packet payloads are tampered by a malicious router. In other cases, packets are forced to make illegal routing turns that may get the system into deadlocks. Despite their intended target, these attacks cause traceable harms and damages to the NoC and ultimately the entire chip. For instance, the program may produce wrong results, or the system may come to a sudden halt or an exception is raised. Such manifestations and traces can be explored for the purpose of attack detection and mitigation. In a sharp contrast, none of these effects will be registered in an aging related attack that is found to be much stealthier. As a matter of fact, the aging attack revealed in this paper takes much longer time to be sensed by a product's end user, or even it will not be realized at all throughout the lifetime of a product.

Stationary malfunction launched by the deterministic attack after the warranty arouses suspicion. For example, if each user finds his/her device malfunction just after the warranty expires, they will accuse the manufacturer. In this manner, probabilistic failure caused by aging makes this planned obsolescence attack hard to be detected.

3 The Manufacturer Strategy

When a profit-driven manufacturer needs to develop an aging strategy for its product, a workable profit model is required to calculate profits under different scenarios. As alluded before, it serves the manufacturer's best interest to make sure that the product functions as promised when it is under warranty, and customers are willing to moving to a new version of the product, for the reasons of product malfunction or something else, soon after the warranty expires. To have such a desirable product lifecycle, the manufacturer may have to develop a capability to accelerate and decelerate the aging of its product at different phases of a product's life cycle. In this section, we first present a profit model concerning the refund cost under warranty. To maximize the profit as predicted by this model, aging acceleration and deceleration strategies will be presented, and a product can switch between the two through an aging controller module as described in this section.

3.1 The Profit Model

The profit of the manufacturer for the i^{th}-version devices can be written as,

$$W_i = (P_i - C_i) \times S_i \tag{4}$$

where P_i, C_i, and S_i are the price, the cost, and the number of sold copies of the i^{th}-version devices, respectively. The sales volume S_i is written as,

$$S_i = \sum_{l=1}^{i-1} \rho_{i-l} \times S_{i-l} + S_0 \tag{5}$$

where ρ_{i-l} is the probability that customers who bought the $(i-l)^{th}$-version of the devices would switch to the new-version, and S_0 is the number of new clients who have never bought any previous version of the product.

Let event B be the occurrence of an event that a customer buys a new version of the device, and let event A be the occurrence of an event that a customer's old version device is worn out. In this case, ρ_{i-l} in Eqn. (5) can be further written as,

$$\rho_{i-l} = \rho(B|A) \times \rho(A) + \rho(B|1-A) \times \rho(1-A) \tag{6}$$

where $\rho(B|A) \times \rho(A)$ is the probability that a customer buys a new version of device given that his/her old-version device malfunctions, and $\rho(B|1-A) \times \rho(1-A)$ is the probability that a customer buys a new device, even though his/her old-version device still functions.

Taking the warranty into account, one can see that, with the version g as its latest model, the profit for the i^{th}-version can be calculated as,

$$W_i = \{\sum_{l=1}^{g} [p_{Ml} \times x_{i-l} + p_{Wl} \times (1 - x_{i-l})] \times S_{i-l} + S_0\} \times (P_i - C_i) - \sum_{m=1}^{w} \sum_{n=0}^{w-m} (x_{i-m} \times S_{i-g+n}) \times C_i \tag{7}$$

where x_i is the failing rate of the i^{th}-version of the device, S_0 is the number of new customers, w is the product warranty and p_{Ml} and p_{Wl} are the respective $(i-l)^{th}$-version device's probabilities, $\rho(B|A)$ and $\rho(B|1-A)$ as defined in Eqn. (6).

The failing rate x_{i-l} in Eqn. (7) is assumed to follow the Gaussian distribution denoted as G(μ,σ^2). Here the mean μ is obtained from Eqn. (3), and the variance σ^2 is a random variable. By setting $\alpha = 0.5$ as the testing condition, x_{i-l} is generated by randomly sampling from G(μ,σ^2). For the proposed planned obsolescence, the value of x_{i-l} depends on the triggering condition of aging acceleration.

3.2 The Aging Controller Module in NoC

The aging controller module is designed to use router aging acceleration during a time trigger threshold, and router aging deceleration after the time trigger threshold, which is set according to the terms of the warranty agreement (analyzed in Section 5.2.2).

Placed at each router, the control module, shown in Fig. 4, consists of the trigger and the routing computation (RC) submodules. When the product is still under warranty, the routers will adopt a routing strategy that helps decelerate aging. This module continuously compares the trigger threshold with the system clock, and forces routers to switch to a different routing strategy to accelerate aging, once the trigger threshold is reached.

As NoC is the communication infrastructure for high performance many-core chips [22]–[24], in what follows, we assume that the NoC under attack cannot be powered off when the chip is powered on.

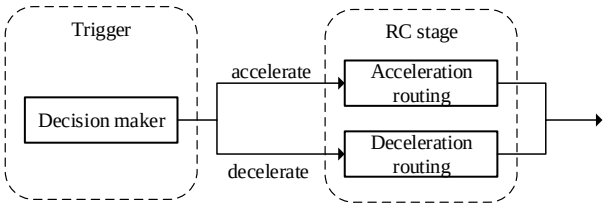


Fig. 4. Architecture of the control module

4 Routing Algorithms

The NoC is assumed to have a mesh topology. Without loss of generality, and for simplicity, a network with $n \times m$ routers (nodes) can be represented in a matrix format with each entry corresponding to a router, as shown in Fig. 5. Assume $r_{i,j}$ is the hotspot node and it is not located at the periphery of the network. The network matrix can be partitioned into nine regions with $r_{i,j}$ at the center and surrounded by other eight regions (defined in Table 1). If the hotspot node, $r_{i,j}$, is located at the periphery of the network

(*i.e.*, $i = 0$, or $j = 0$, or $i = n - 1$, or $j = m - 1$), one or a few regions will have no router.

The same routers can be taken differently when there are multiple hotspot nodes. For instance, if routers $r_{0,0}$ and $r_{3,3}$ are the hotspot nodes, then $r_{1,1}$ falls into region NE of hotspot node $r_{0,0}$ and into region SW of $r_{3,3}$.

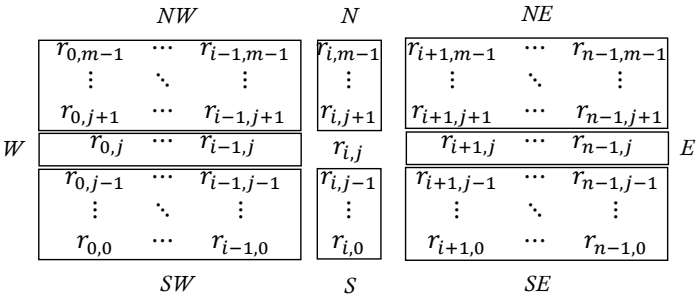


Fig. 5. Network partition.

TABLE 1
Definition of Region Partition

Region	Definition
NW	For each $r_{x,y}$, $0 \le x < i, j < y \le m-1$.
N	For each $r_{x,y}$, $x = i, j < y \le m-1$.
NE	For each $r_{x,y}$, $i < x \le n-1, j < y \le m-1$.
W	For each $r_{x,y}$, $0 \le x < i, y = j$.
E	For each $r_{x,y}$, $i < x \le n-1, y = j$.
SW	For each $r_{x,y}$, $0 \le x < i, 0 \le y < j$.
S	For each $r_{x,y}$, $x = i, 0 \le y < j$.
SE	For each $r_{x,y}$, $i < x \le n-1, 0 \le y < j$.

Hotspot nodes can be obtained from traffic profiling by the manufacturer. In case that traffic profiles cannot be readily obtained, data traffic can be collected on the fly with the help of system software like operating system, and hotspot nodes, in this case, can be dynamically located as they handle more data traffic than any other routers in the NoC.

4.1 Routing Algorithm for Aging Acceleration

For aging acceleration, even if there are multiple hotspot nodes, we only need to target one single hotspot node, as the chip's lifetime is bounded by the one with the lowest MTTF. Targeting multiple hotspot nodes for aging purpose brings no additional benefit for the sake of aging.

Once the trigger module activates the aging acceleration signal, the RC module selects the aging acceleration routing algorithm to route data packets, which stipulates the packets' routing paths to include the hotspot node. That is, the hotspot node is set as the temporary destination of a packet, and the packet is first transmitted to this hotspot node by XY routing, after which it will be delivered to the destination node.

As shown in Algorithm 1, the aging acceleration routing algorithm consists of a decision step (lines 1 to 4) and a routing step (line 5). The decision step checks whether a packet can traverse the hotspot node to satisfy three conditions, including minimal routing, turn model, and stealthiness.

To ensure the minimal routing in a network given in Fig. 5, a packet needs to travel along a path such that at every intermediate node, the next node will be the one bringing the packet one hop closer to the destination (line 1).

Following the west-first turn model [16], only the west side of the network participates in the aging acceleration (line 2). That is, the source node of a packet is restricted to locate in the regions of NW, W, SW, N, and S.

A threshold is set for the manufacturer to balance between the effectiveness and the stealthiness of aging acceleration. A packet is forced to pass through the hotspot node only if the threshold is not greater than the Manhattan distance between the source node and the hotspot node (line 3). This approach can help alleviate the congestion around the hotspot node that otherwise can cause serious performance degradation and undermine the attack stealthiness.

When all the above listed conditions are satisfied, the hotspot node is regarded as the temporary destination (line 4). The packet is first routed to the hotspot node by XY routing, and then from the hotspot to the final destination again by XY routing. If a packet is determined not to pass the hotspot node, it will be routed from the source to the destination directly.

Algorithm 1: Aging Accelerating Routing Algorithm

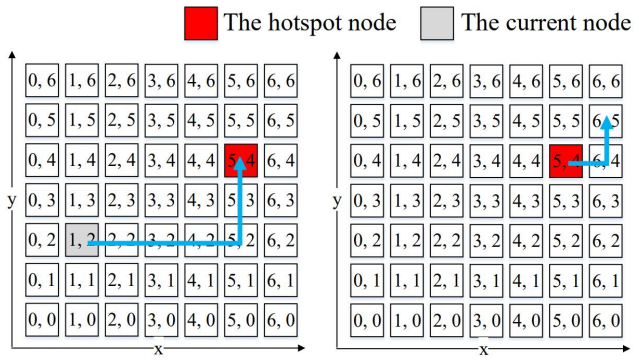
Input:
Cur: The address of the current node.
Hot: The address of the hotspot node.
Src: The address of the source node.
Dst: The address of the destination node.
Output: *Dir*: The output direction of the packet.
Result: Find the direction for the packet path that first travels to the hotspot node, and then to the destination.

```
/* Decision module                                    */
1 if (Minimal routing condition is satisfied) and
2 (Src.x ≤ Hot.x) and
3 (|Src.x - Hot.x| + |Src.y - Hot.y| ≤ thr) then
4     Dst ← Hot;
/* Routing module                                     */
5 do XY routing;
```

An example is shown in Fig. 6. Here the NoC is a 7×7 network, and the destination and the source nodes are (6, 5) and (1, 2), respectively. The current node is marked in grey, and the hotspot node is (5, 4). The threshold is set as 7. When the packet arrives at node (1, 2) in Fig. 6 (a), as all the three conditions for aging acceleration are satisfied, the packet will be sent to the hotspot node first. According to the XY routing algorithm, the routing module sets the output direction as East and forwards the packet to node (2, 2); the packet traverses nodes (2, 2), (3, 2), (4, 2), (5, 2), (5, 3), and finally arrives at node (5, 4) in Fig. 6 (b). From the hotspot node (5, 4), the packet is routed to its destination node (6, 5) in this case, following the path defined by XY routing.

4.2 Routing Algorithm for Aging Deceleration

For aging deceleration, all the hotspot nodes have to be considered together. Yet the whole chip's lifetime is bounded



(a) The packet arrives at (1, 2). (b) The packet arrives at (5, 4).

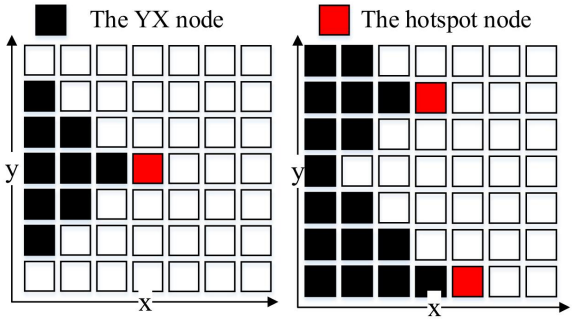
Fig. 6. An example illustrating aging acceleration routing.

by the one with the lowest MTTF, and the life time of each individual hotspot node has been extended for the longevity of the chip.

Once the trigger module activates the aging deceleration signal, the RC module selects the aging deceleration routing algorithm, which diverts packets to be routed along the paths away from the hotspot nodes.

A specific region that runs YX routing algorithm, named as YX region, is composed of nodes given by Eqn. (8), assuming the hotspot node is (x_0, y_0). When there are multiple hotspot nodes, the YX region is formed for each hotspot node, as shown in Fig. 7. The YX region forms a triangle shape, and it shall be able to generate more evenly distributed traffic as indicated in [3]. To ensure the routing is deadlock-free, the YX region is formed from only the west of the network, and follows the west-first turn model [16].

$$|y_0 - y| < x_0 - x \tag{8}$$



(a) Single hotspot node (b) Multiple hotspot nodes

Fig. 7. Examples of the YX region.

As shown in Algorithm 2, the aging deceleration routing consists of a decision step (lines 1 to 5) and a routing step (lines 6 to 9). The decision step checks whether the packet is located at the YX region or not (line 1). By applying the west-first turn model, the destination node of a packet is restricted to locate in the regions of NE, E, and SE (line 2).

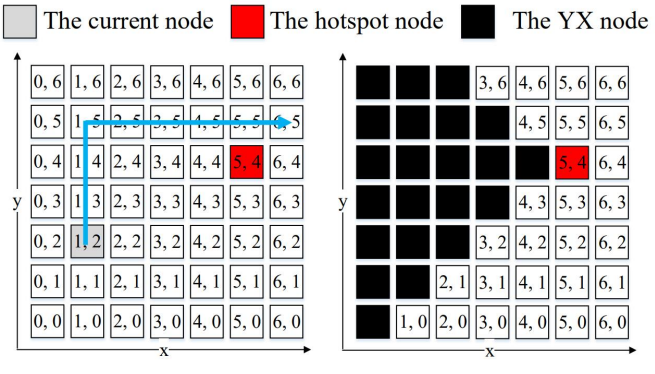
If both the conditions are satisfied, the YX routing signal is sent to the routing module to make the packet divert from the hotspot node. Otherwise, the routing module directly runs XY routing.

Algorithm 2: Aging Deceleration Routing Algorithm

Input:
Cur: The address of the current node.
Hot: The address of the hotspot node.
Dst: The address of the destination node.
Output: *Dir*: The output direction of the packet.
Result: Find the direction for the packet path that bypasses the hotspot node as possible.

```
/* Decision module                                   */
1 if (Cur is located in the YX region) and
2 (Dst.x > Hot.x) then
3 |  flag ← 1;
4 else
5 |  flag ← 0;
/* Routing module                                    */
6 if flag = 1 then
7 |  do YX routing;
8 else
9 |  do XY routing;
```

An example is shown in Fig. 8. Here the NoC is a 7×7 network, and the destination and the source nodes are (6, 5) and (1, 2), respectively. The current node is marked in grey, and the hotspot node is (5, 4). The YX region is shown in Fig. 8 (b). When the packet arrives at node (1, 2) in Fig. 8 (a), the packet will follow YX routing, as both conditions for aging deceleration are satisfied. According to the YX routing algorithm, the routing module sets the output direction to be North and forwards the packet to node (1, 3); the packet traverses nodes (1, 3), (1, 4), (1, 5), (2, 5), (3, 5), (4, 5), (5, 5), and finally arrives at node (6, 5).



(a) The packet arrives at (1, 2). (b) The YX region.

Fig. 8. An example illustrating aging deceleration routing.

5 Experimental Evaluation

5.1 Experimental Setup

The parameters in the aging model in Section 2.2 are listed in Table 2. To obtain the probabilities whether the customers will buy the devices under different scenarios or not in Section 3.1, a survey is conducted that each person is asked to answer the questions listed in Table 3. 116 people (college students and faculty members) were surveyed and their

ages range from 18 to 36. We apply the statistical data to fit Eqn. (7), and the probabilities are also shown in Table 3.

TABLE 2
MTTF Model Parameters

Parameter	Value	Description
b_{NBTI}		Fitting number of MTTF
n	0.166	Time exponent
E_a	0.49	Activation energy (eV)
k	1.380649e-23	Boltzmann's constant ($J/^\circ K$)
T		Temperature ($^\circ K$)
a	0.5	Duty cycle

TABLE 3

Poll Question

Will you buy a new version smart phone if it malfunctions in 1/2/3 year/years?
Will you buy a new version smart phone if your current one is still functional after 1/2/3 year/years?

Profit Model Parameters

Parameter	Value	Description
p_{M1}	57.14%	The probability that the customers will buy the devices, knowing it will malfunction in 1 year.
p_{M2}	66.67%	The probability that the customers will buy the devices, knowing it will malfunction in 2 years.
p_{M3}	80.95%	The probability that the customers will buy the devices, knowing it will malfunction in 3 years.
p_{W1}	19.05%	The probability that the customers will buy the devices when it is still working within 1 year.
p_{W2}	38.09%	The probability that the customers will buy the devices when it is still working within 2 years.
p_{W3}	14.29%	The probability that the customers will buy the devices when it is still working within 3 years.

The experiments are simulated using an event-driven many-core simulator [16]. The architecture comes with a shared-memory, and each core has a private L1 cache, and a shared L2 cache bank; all the cores are connected to routers in NoC. The detailed simulator configuration is shown in Table 4. McPAT [18] is also integrated into the simulator to measure the power consumption of each router, followed by using HotSpot for computing the temperature. MTTF is evaluated by the aging model given in Eqn. (3). The simulation is performed using both random benchmarks and a few real benchmarks. The random benchmarks are generated randomly, while the real benchmarks used for performance evaluation are shown in Table 5, which are selected from PARSEC [19] and SPLASH-2 [20].

Fig. 9 illustrates the different configurations of the hotspot nodes and the YX regions for different simulation scenarios. For the random benchmarks, the hotspot node is generally considered as the central node of the network, which is typically the most vulnerable component of the chip. The YX region is set in the west of the hotspot node, and the west-first turn model [16] is adopted under this scenario. For the real benchmarks, the memory controllers of the simulator are connected with the routers (2, 0), (5, 0), (2, 7) and (5, 7). As the profiling data from pre-simulation indicate (2, 0) is the most congested node for any real

TABLE 4

Configuration of the Many-core Simulator for Trace Extraction

Number of processors	64 (MIPS ISA 32 compatible)
Fetch/Decode/Commit size	4 / 4 / 4
ROB size	64
L1 D cache (private)	16 KB, two-way, 32B line, two cycles, two ports, dual tags
L1 I cache (private)	32 KB, two-way, 64B line, two cycles
L2 cache (shared) MESI protocol	64 KB slice/node, 64B line, six cycles, two ports
Main memory size	2 GB, latency 200 cycles
Frequencies available	1 GHz, 800 MHz, 500 MHz, 330 MHz

On-chip Network Parameters

NoC size	8×8
Number of routers	64
NoC flit size	72-bit
NoC latency	router 1 cycle, link 1 cycle
NoC VC number	1
NoC input buffer size	12
NoC output buffer size	12

TABLE 5
Benchmarks Used in the Simulation

PARSEC	blackscholes, bodytrace, canneal, ferret, fluidanimate, streamcluster, vips, x264
SPLASH-2	raytrace

benchmarks, it is set as the only hotspot node. The YX region is correspondingly set on its east for maximizing aging deceleration effect, and the negative-first turn model [16] is adopted under this scenario. Different benchmarks still lead to the same hotspot node under same CMP configuration. Thus, the critical node can be set as the default target from the pre-simulation.

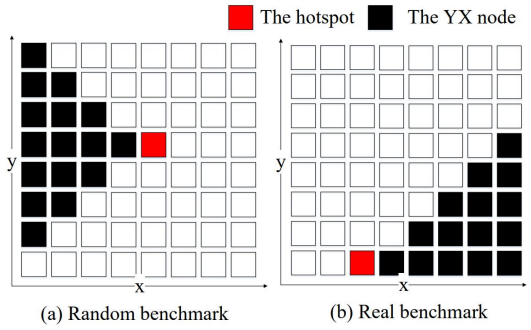


Fig. 9. The configuration of the hotspot nodes and the YX regions.

The threshold needed in the aging acceleration routing algorithm is predetermined to balance the aging effect and latency. Fig. 10 shows the impact of the threshold on the MTTF and latency. One can see that the latency soars as the threshold is greater than 4. In the following experiment, the threshold is thus set to be 4.

5.2 Experimental Results

As alluded in Section 2.4, stealthiness is so critical to sustain and thus ensure the success of any ongoing planned obsolescence attack, which is so different from other DoS attacks

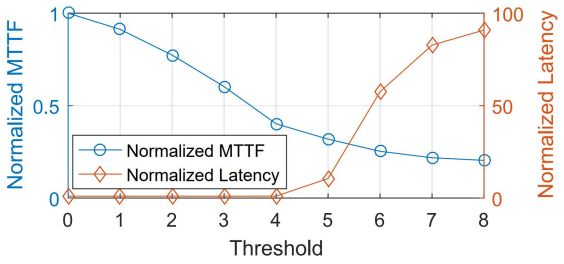


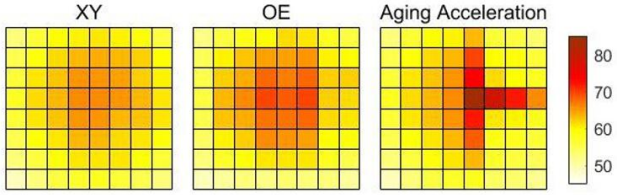
Fig. 10. Normalized MTTF and latency with respect to threshold.

that emphasizes timing error for effectiveness. Network throughput and latency would give a clear indication of stealthiness, and the effectiveness of the proposed attack is measured by MTTF, which is of no concern to other DoS attacks.

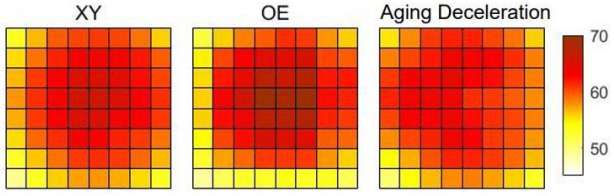
In what follows, we will first present the results related to the effectiveness and stealthiness evaluation of the proposed aging attack in Section 5.2.1. The profit evaluation results are reported and analyzed in Section 5.2.2, and finally we will examine the overheads in Section 5.2.3.

5.2.1 MTTF and Performance Evaluation

The results of the simulation implemented running random traffic are first analyzed. The temperatures of the proposed two routing algorithms are compared against XY and OE routing algorithms. Fig. 11 (a) shows that the proposed aging acceleration routing algorithm can increase the chip temperature by 17.17°C and 14.66°C higher than XY and OE routing algorithms, respectively. Fig. 11 (b) shows that the proposed aging deceleration routing algorithm can help reduce the chip temperature by 4.91°C and 7.42°C over XY and OE routing algorithms, respectively.



(a) XY, OE and the proposed aging acceleration routing algorithm.



(b) XY, OE and the proposed aging deceleration routing algorithm.

Fig. 11. The temperature distribution of NoCs with different routing algorithms.

The normalized traffic volume passing through hotspot nodes of the two proposed routing algorithms are shown in Fig. 12 (a). The proposed aging acceleration routing algorithm increases the traffic volume of the hotspot node by 128.22% and 106.79% over XY and OE routing algorithms, respectively. The proposed aging deceleration routing algorithm decreases the traffic volume of hotspot node by 12.33% and 33.76% over XY and OE routing algorithms, respectively.

The normalized MTTF results of the two proposed routing algorithms are shown in Fig. 12 (b). The proposed aging acceleration routing algorithm downgrades the MTTF by 59.35% and 52.89% over XY and OE routing algorithms, respectively. The proposed aging deceleration routing algorithm improves the MTTF by 8.88% and 26.19% over XY and OE routing algorithms, respectively.

The normalized network throughput and latency results of the two proposed routing algorithms are shown in Fig. 12 (c) and Fig. 12 (d), respectively. The proposed aging acceleration routing algorithm and the proposed aging deceleration routing algorithm have almost the same throughput and latency as XY and OE routing algorithms. Therefore, the attack is stealthy, *i.e.*, no salient performance degradation can be observed by users.

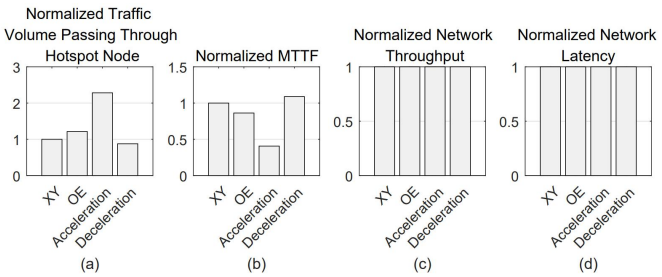


Fig. 12. (a) The normalized traffic volumes passing through hotspot nodes, (b) the normalized MTTFs, (c) the normalized network throughputs, and (d) the normalized network latencies of NoCs with different routing algorithms running random benchmark.

The variations of ΔV_{th} (*i.e.*, change of transistor threshold voltage) over time are evaluated for different scenarios, that is, normal condition (without any attack), the proposed planned obsolescence attack (deceleration first and acceleration after the trigger threshold), acceleration only, and deceleration only schemes, as shown in Fig. 13. In this evaluation, the chip can be considered as faulty when ΔV_{th} exceeds 10%. The NoC under the proposed planned obsolescence malfunctions 14.51% and 23.79% faster than the NoC under normal condition and deceleration only, respectively. Compared to the acceleration only case, the proposed planned obsolescence slows down the aging by 48.95%.

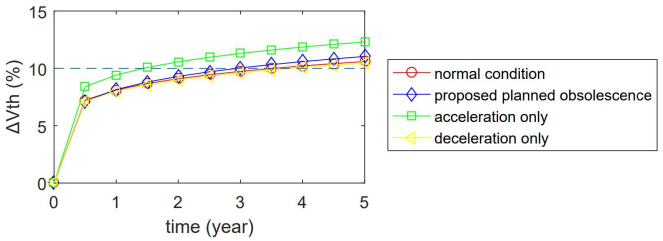


Fig. 13. The variations of ΔV_{th} over time.

Fig. 14 shows the results of the proposed two routing algorithms with XY and OE routing algorithms running the real benchmarks. The normalized traffic volume passing through hotspot nodes of the two proposed routing

algorithms are shown in Fig. 14 (a). The proposed aging acceleration routing algorithm increases the average traffic volume of hotspot node by 62.88% and 85.07% over XY and OE routing algorithms, respectively. The proposed aging deceleration routing algorithm decreases the average traffic volume of hotspot node by 15.41% and 3.98% over XY and OE routing algorithms, respectively.

The normalized MTTF results of the two proposed routing algorithms are shown in Fig. 14 (b). The proposed aging acceleration routing algorithm downgrades MTTF by 47.54% and 53.64% on average over XY and OE routing algorithms, respectively. The proposed aging deceleration routing algorithm improves MTTF by 18.46% and 4.69% on average over XY and OE routing algorithms, respectively.

The normalized network throughput and latency results of the two proposed routing algorithms are shown in Fig. 14 (c) and Fig. 14 (d), respectively. The proposed aging acceleration and the aging deceleration routing algorithms have almost the same throughput and latency as XY and OE routing algorithms, as a result of the two factors. First, both the aging acceleration and deceleration algorithms fall into the family of minimal-path routing, meaning that packets follow the shortest path, linking the source to the destination. Second, since PARSEC and SPLASH-2 applications have light traffic loads [25], the data traffic will not cause congestion in the NoC.

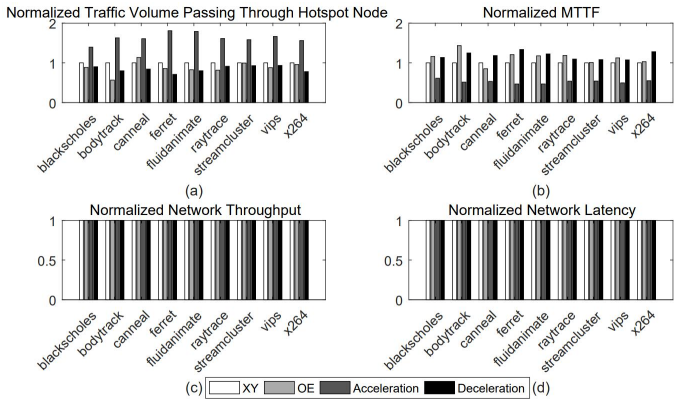


Fig. 14. (a) The normalized traffic volumes passing through hotspot nodes, (b) the normalized MTTFs, (c) the normalized network throughputs, and (d) the normalized network latencies of NoCs with different routing algorithms running different real benchmarks.

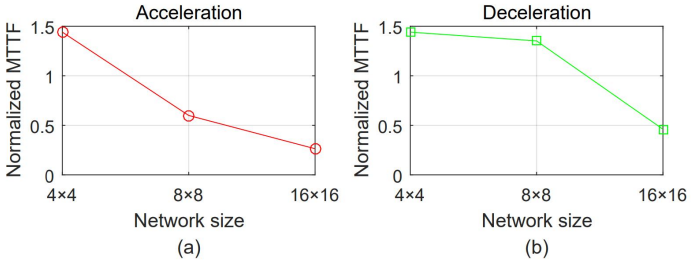


Fig. 15. The normalized MTTF results of the proposed (a) aging acceleration and (b) aging deceleration routing algorithms *vs.* the network size

In Fig. 15, the normalized MTTFs of the networks running proposed aging acceleration and deceleration routing algorithms (with respect to that of the case featuring an 8×8 network with XY routing algorithm) are obtained for various network sizes. One can see that as the network size scales up, the minimal MTTFs of the NoC running both acceleration and deceleration routing algorithms decrease. This is because in a larger network, more traffic tends to flow through the hotspot nodes making them age faster. When the network size is 8×8, both the acceleration and deceleration effect reach the peak, 40.006% greater and 35.19% less than XY routing, respectively.

5.2.2 *Profit Evaluation*

Table 6 lists the configuration of parameters in the profit model in Eqn. (7), using the probabilities in Table 3. The profits are evaluated for different scenarios, that is, normal condition (without any attack), the proposed planned obsolescence attack, acceleration only (with a planned obsolescence attack using only the aging acceleration routing in Section 4.1), and deceleration only (with a planned obsolescence attack using only the aging deceleration routing in Section 4.2) schemes.

TABLE 6
Profit Model Parameters

Parameter	Value	Description
P (*USD*)	8500	The price of the device
C (*USD*)	3000	The cost of the device
S	250000	The number of the old customers who have bought the devices within the last g versions
S_0	$0.4 \times S$	The number of the new customers who have not bought the devices within the last g versions
w (*year*)	2	The warranty of the device
g (*year*)	3	The generations considered in the model
σ^2	0.25	The variance that influences the failing rate x_{i-l}

The Range of Profit Model Variables

Parameter	Range
S	(100000, 400000)
P (*USD*)	(5000, 10000)
C (*USD*)	(1000, 3500)
σ^2	(0, 3)
w (*year*)	(0, 2)

The trigger threshold when the aging acceleration routing algorithm launches, referred in Section 3.2, is analyzed and the relationship between the trigger threshold and the manufacturer profit is shown in Fig. 16. The profits are normalized with respect to that with the case with the configuration in Table 6. From Fig. 16, one can see that when the trigger threshold is set to be 1 year, the normalized manufacturer profit reaches the maximum. In the following evaluation, the trigger threshold is configured as 1 year.

Fig. 17 shows the profits when varying the sales volume, the price, the cost, the variance, and the warranty. These profits are normalized with respect to the profit of case as summarized in Table 6.

From Fig. 17 (a), one can see that the profit with the proposed attack increases at a much faster rate than the other schemes under different sales numbers. When the sales volume is 400000, the profit of the proposed planned obsolescence attack is 15.54%, 25.69%, and 53.36% higher

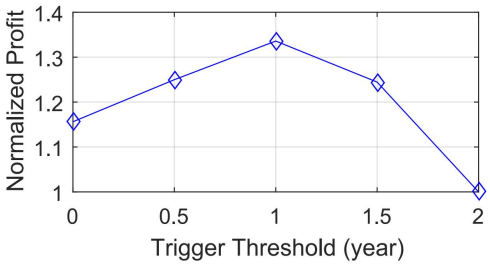


Fig. 16. The relationship between the trigger threshold and the normalized manufacturer profits.

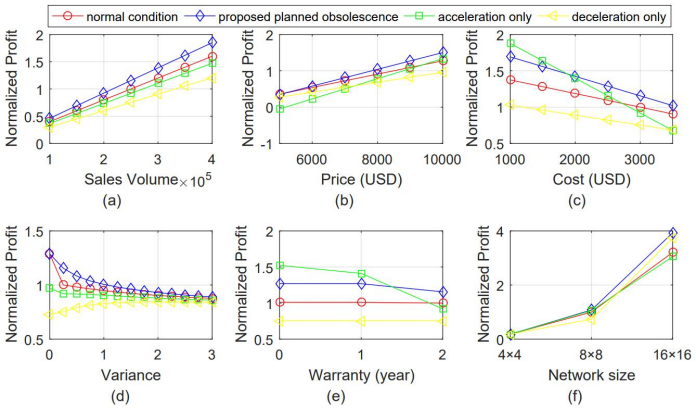


Fig. 17. Normalized manufacturer profits under different scenarios by varying (a) the sales volume, (b) the price, (c) the cost, (d) the variance, (e) the warranty, and (f) the network size.

than that of the normal condition, acceleration only, and deceleration only schemes, respectively. The increased profit can be attributed to the combined effect that the proposed attack helps reduce refund and at the same time increases the sales volume to new customers. If a manufacturer only engages in aging acceleration only scheme, it actually loses money to the normal condition(*i.e.*, not engaging in such activity), if when refunding is factored in to observe the warranty.

From Fig. 17 (b), one can see that, for the price of $10,000, the profit of the proposed planned obsolescence attack is 17.69%, 12.48%, and 56.56% higher than the normal condition, acceleration only, and deceleration only schemes, respectively.

When the cost is $3,500, the profit of the proposed planned obsolescence attack is 12.68%, 50.17%, and 49.12% higher than the normal condition, acceleration only, and deceleration only schemes, respectively, as shown in Fig. 17 (c). The profit with the proposed attack is 32.60% and 77.02% higher than the acceleration only and deceleration only schemes, respectively when the variance converges towards 0 (Fig. 17 (d)). The curves of all the schemes tend to be the same as the variance increases.

From Fig. 17 (e), one can see that without taking the warranty into account (when the warranty is 0), the profit of the acceleration only scheme is higher than the others, and the profit with the acceleration only scheme decreases as the warranty increases. When the warranty is 2 years, the profit is 8.07% and 20.44% lower than the normal condition and the proposed planned obsolescence attack, respectively. The profit of the proposed planned obsolescence attack is 15.54%, 25.69%, and 53.36% higher than the normal condition, acceleration only, and deceleration only schemes, respectively.

From Fig. 17 (f), one can see that the profit at the presence of the proposed attack increases as the network size increases. Among these four schemes, the proposed planned obsolescence attack leads to the maximal profit in both the 8×8 and 16×16 networks.

5.2.3 Overhead Analysis

The hardware cost of the proposed router is analyzed from the synthesis result reported by Synopsys Design Compiler with a TSMC $45nm$ CMOS library. From DSENT [21], the XY router with the configuration in Table 4 with $45nm$ CMOS technology consumes 16.6 mW power and has an area of 57530 μm^2. The power consumption and area of the proposed router is 16.7 mW and 57664 μm^2. Therefore, the power consumption and area overhead of the proposed router are fairly modest, only 0.60% and 0.23% higher than the original router, respectively.

6 Conclusion

In this paper, we detailed a planned obsolescence attack that targets the hotspot routers, the most vulnerable part of NoC-based many-core chips. In particular, we added the product warranty into the aging model to reveal how a manufacturer can maximize its profit. In specific, the planned aging can be achieved with the two proposed routing algorithms: one for accelerated aging when the warranty expires, and one for decelerated aging when the warranty is still in effect. Experiments have shown that the former algorithm reduces the MTTF of the chip by about 47.54% and the latter algorithm improves the MTTF by about 18.46%. The profit from the proposed planned obsolescence is 15.54%, 25.69%, and 53.36% higher than that from the normal condition, acceleration only, and deceleration only schemes, respectively. This study clearly shows that the proposed planned obsolescence attack secretly causes more economic losses to customers, which needs to be balanced out with appropriate countermeasure yet to be developed.

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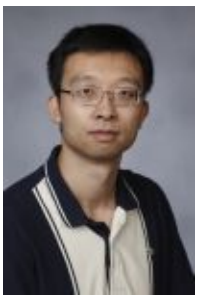

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