Power Semiconductor Devices - Silicon vs. New Materials

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IEEE Compel Conference
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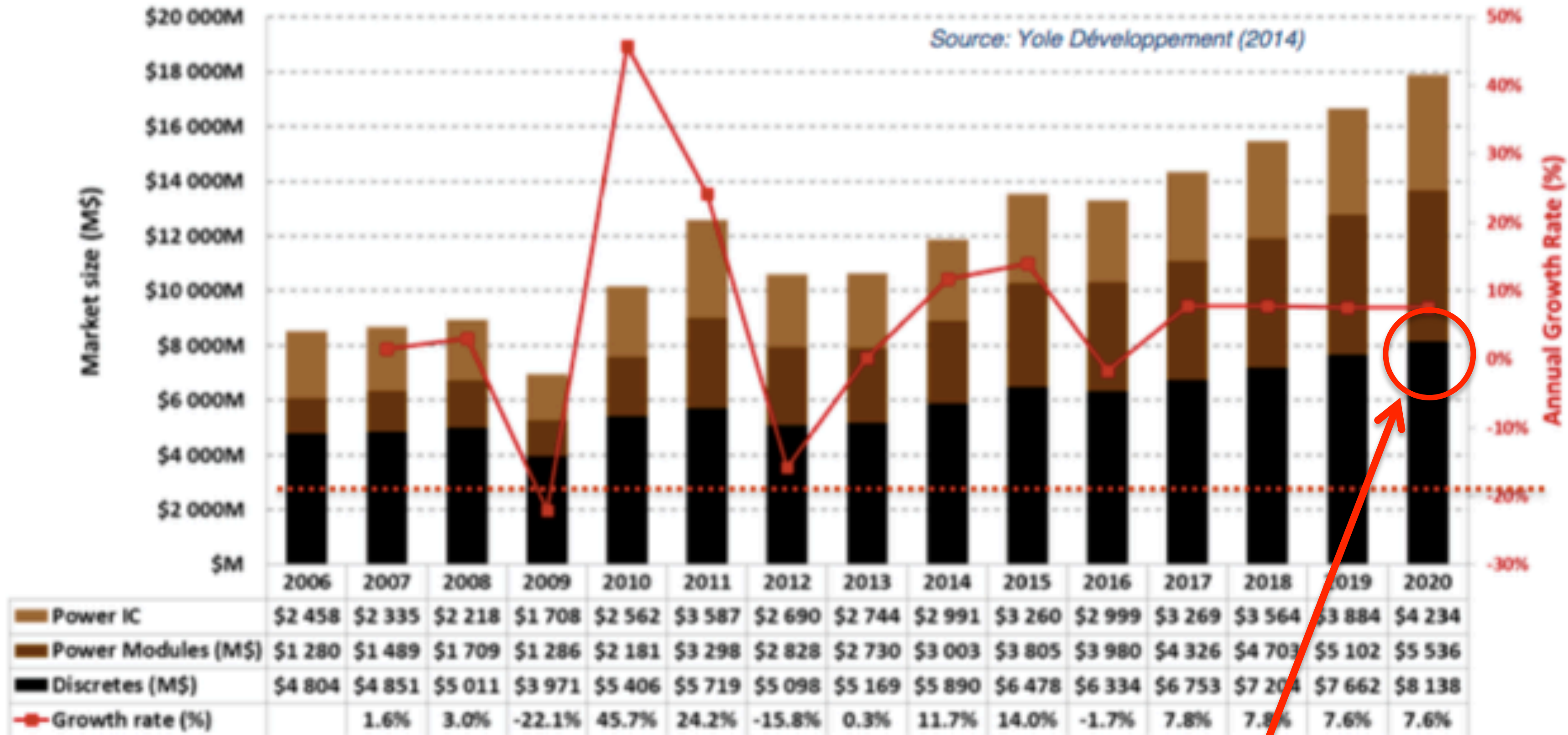
- Market Opportunities for Power Devices
- Materials Advantages of SiC and GaN vs. Si
- Si Power Devices – The Dominant Solution Today
- Current Status of GaN and SiC Power Switches
- Will GaN and SiC really capture a large part of the power switch market?
- What Are the Big Challenges/Opportunities Going Forward?
- Conclusions.

Estimated Overall Power Device Market



	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
Power IC	$2 458	$2 335	$2 218	$1 708	$2 562	$3 587	$2 690	$2 744	$2 991	$3 260	$2 999	$3 269	$3 564	$3 884	$4 234
Power Modules (M$)	$1 280	$1 489	$1 709	$1 286	$2 181	$3 298	$2 828	$2 730	$3 003	$3 805	$3 980	$4 326	$4 703	$5 102	$5 536
Discretes (M$)	$4 804	$4 851	$5 011	$3 971	$5 406	$5 719	$5 098	$5 169	$5 890	$6 478	$6 334	$6 753	$7 204	$7 662	$8 138
Growth rate (%)		1.6%	3.0%	-22.1%	45.7%	24.2%	-15.8%	0.3%	11.7%	14.0%	-1.7%	7.8%	7.8%	7.6%	7.6%

Overall discrete device market estimated at $8B in 2020.

Estimated Overall WBG Power Device Market

	2014	2015	2016	2017	2018	2019	2020
GaN	$ 5 M	$ 10 M	$ 22 M	$ 49 M	$ 102 M	$ 177 M	$ 303 M
SiC	$ 133 M	$ 197 M	$ 231 M	$ 274 M	$ 316 M	$ 357 M	$ 437 M

These projections suggest WBG devices will have < 10% of the discrete market in 2020. If they have much higher performance, WHY?

Power Devices - Silicon vs. New Materials

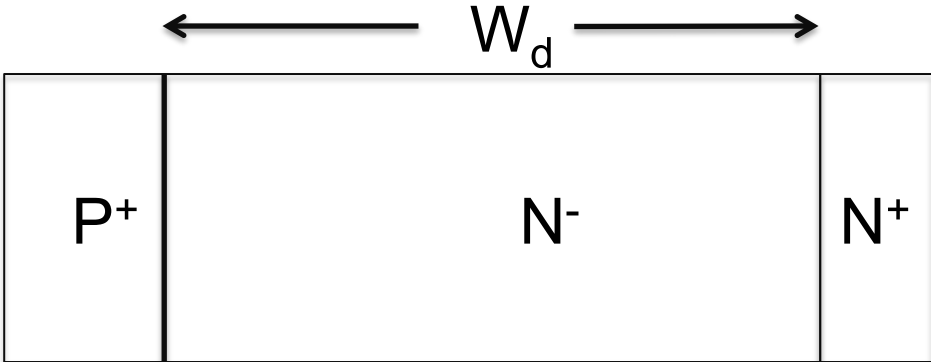
	Si	GaAs	GaN	4H-SiC
Bandgap energy (eV)	1.12	1.4	3.49	3.26
Breakdown field (MV/cm)	0.3	0.4	3.5	3
Electron mobility at 300 K ($cm^2/V{\cdot}s$)	1400	8500 *10,000	900 *2000	700
Saturated (peak) electron velocity (10^7 cm/s)	1.0 (1.0)	1.3 (2.1)	1.3 (2.7)	2.0 (2.0)
Relative dielectric constant	11.8	12.8	9	10
Thermal conductivity (W/cm-K)	1.5	0.5	1.7	3.5
Thermal expansion (10^{-6}/K)	2.6	5.7	5.6	5.1
Lattice constant (Å)	5.43	5.65	3.19	3.07

* Values of corresponding heterostructures.

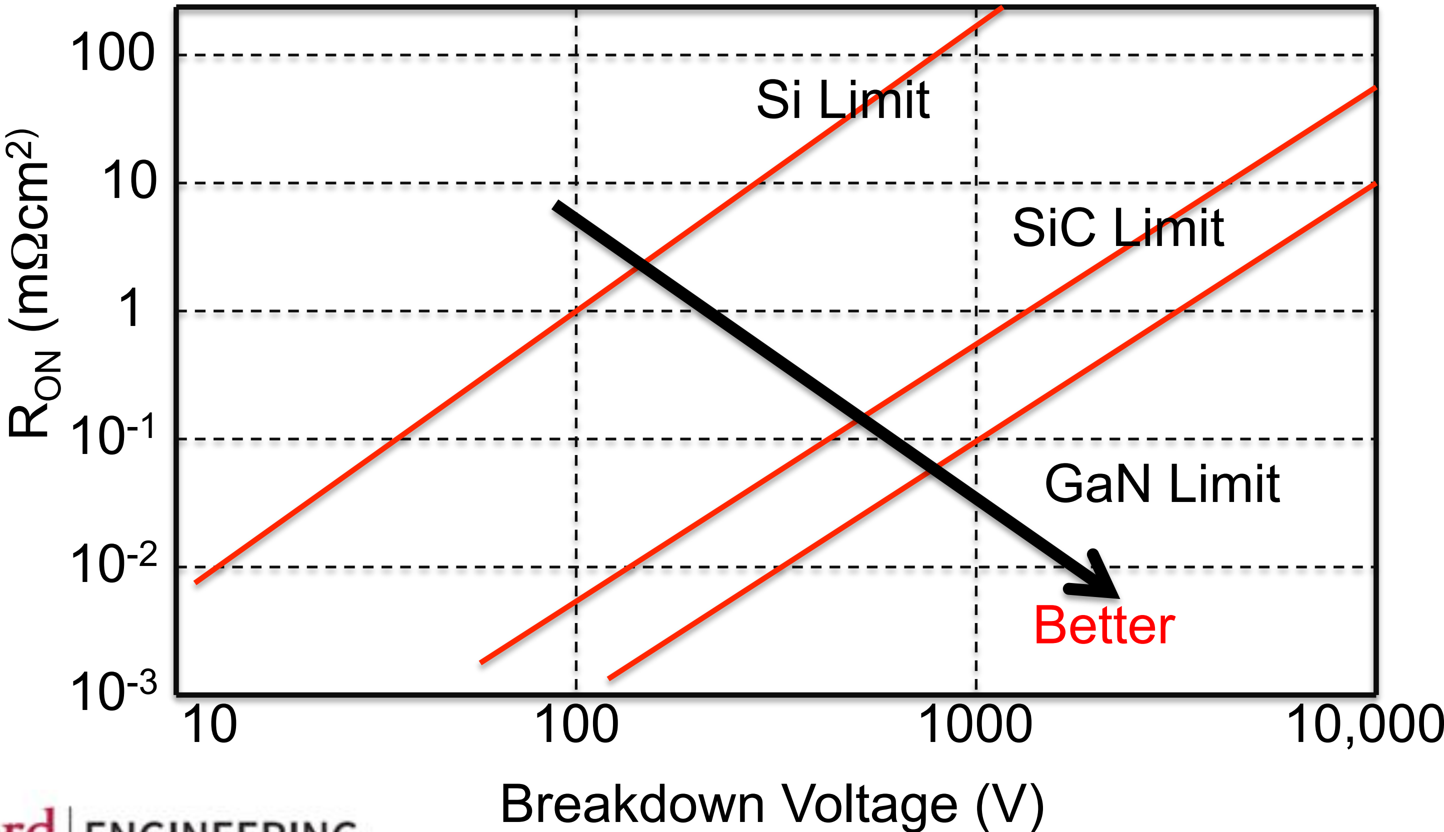
(F. Iacopi et al., MRS Bulletin, May 2015, pg. 390)

The opportunity for major advances occurs primarily because of the higher bandgap and breakdown fields in GaN and SiC.

Basic Materials Comparison – Unipolar Limit



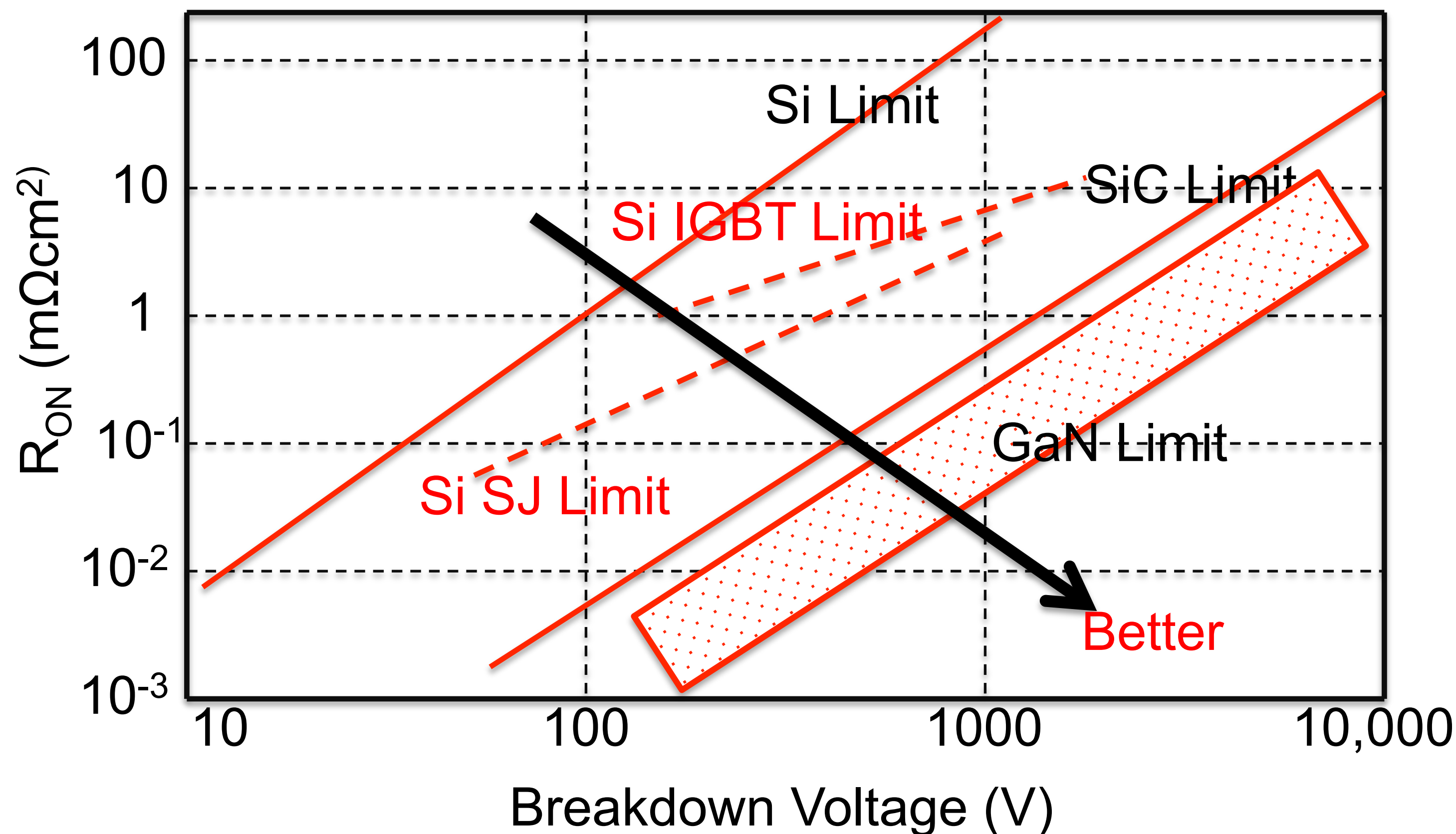
$$R_{on} = \frac{W_d}{q\mu N_D} = \frac{E_{cr}\kappa\varepsilon_o}{\mu q^2 N_D^2} = \frac{4V_{bv}^2}{\mu\kappa\varepsilon_o E_{cr}^3}$$



Basic Materials Comparison

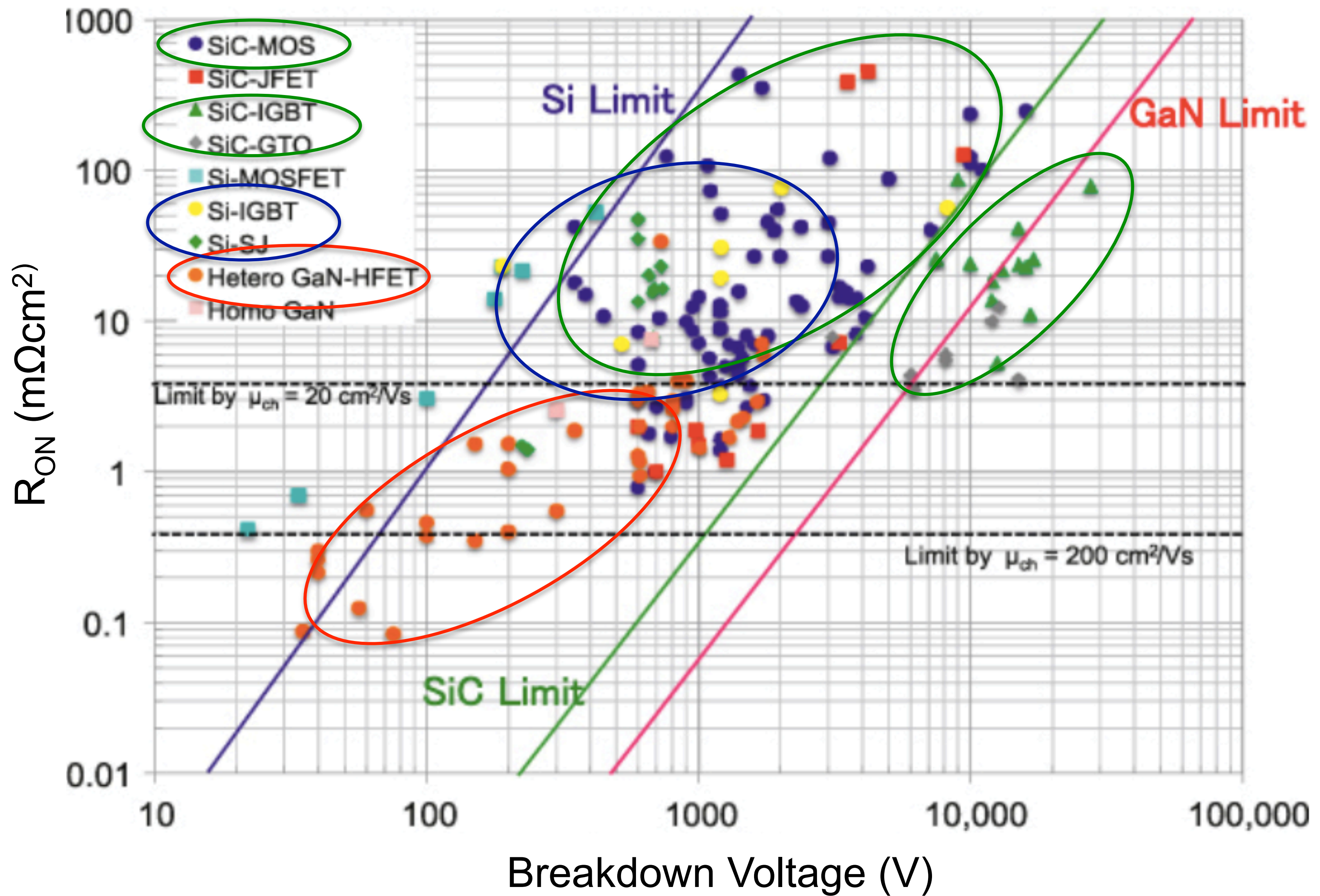
But in reality, the situation is more complicated.

- More sophisticated Si devices than simple unipolar MOSFETs.
- GaN limit depends on μ: > 2000 cm^2/Vsec HEMT,
  ≈ 1600 Bulk, < 200 MIS



(IGBT limit – A Nakagawa (Toshiba), ISPSD 2006)

Experimental Data



(H. Okumra, MRS Bulletin, Vol. 40, pg. 439,May 2015)

Observations

1. Silicon devices (IGBTs, superjunction devices) are significantly better than the unipolar Si "material limit".

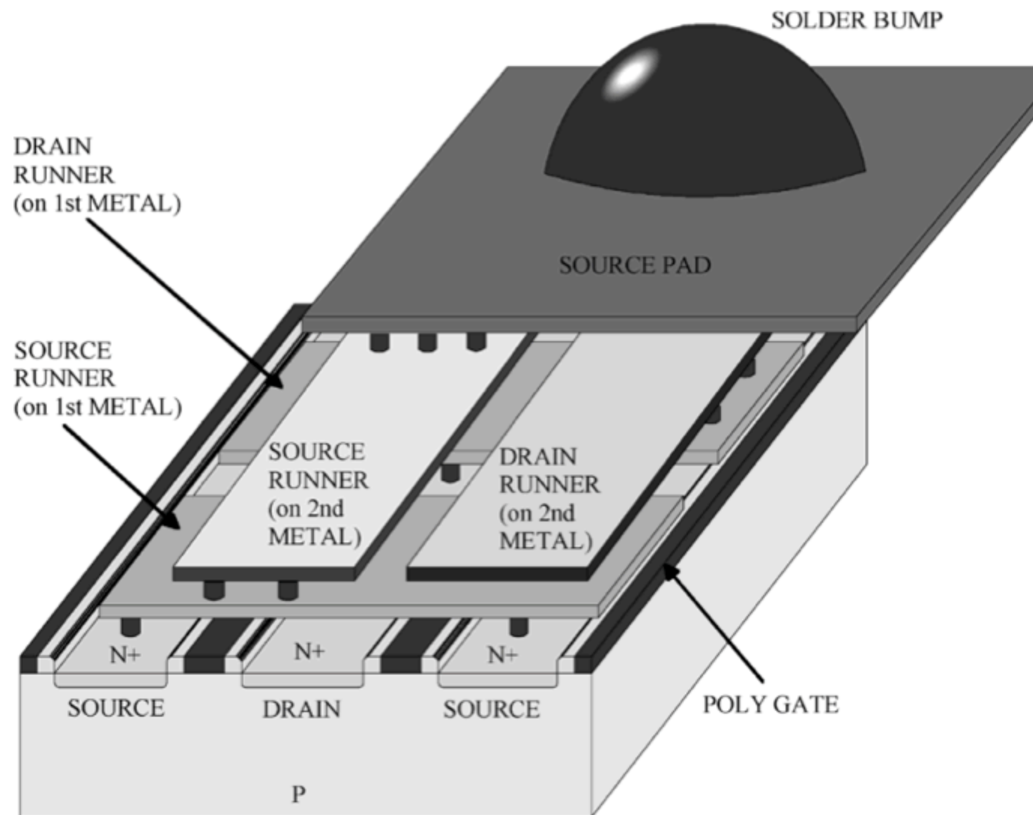
2. Low voltage SiC MOSFETs are ≈ same as Si MOSFETs. High voltage SiC MOSFETs are much better than Si. SiC IGBTs break the SiC unipolar "material limit" just as Si IGBTs break the Si limit.

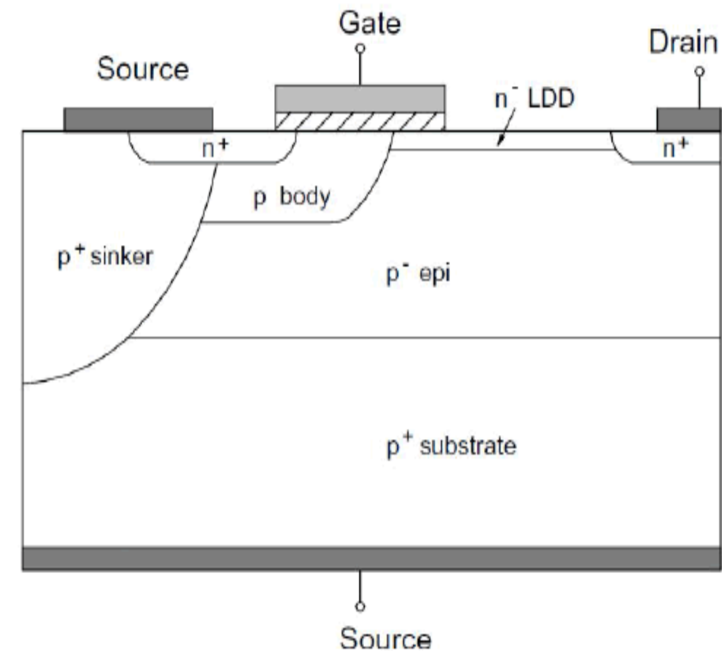
3. GaN experimental results are all < 600V and are well below the material limits expected for GaN but they do achieve the lowest R_{ON}.

4. And then, of course, there are cost, reliability, plug in replacement . . . . issues to deal with.

First let's look at the silicon competition

Low Voltage Si Power Devices: NMOS or LDMOS ≤ 20 Volts



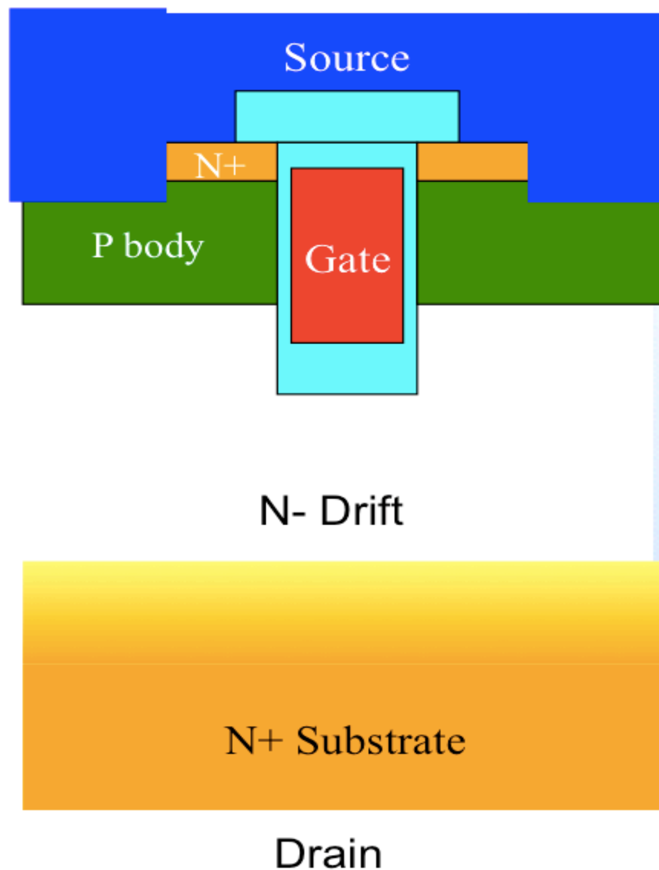


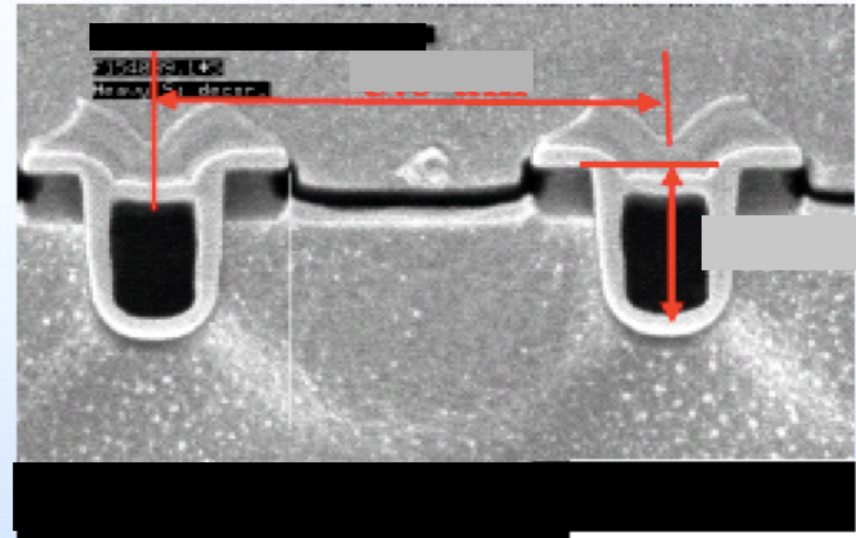
Figures : Z.John Chen et.al. IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 21, NO. 1, JANUARY 2006 p. 11-17

DMOS – Double diffused MOSFET

Conventional planar, lateral Si MOS devices. Cost reductions through manufacturing efficiencies. Mostly older nodes. CHEAP!

Moderate Voltage Si Power Devices: Vertical UMOS
15 - 200 Volts

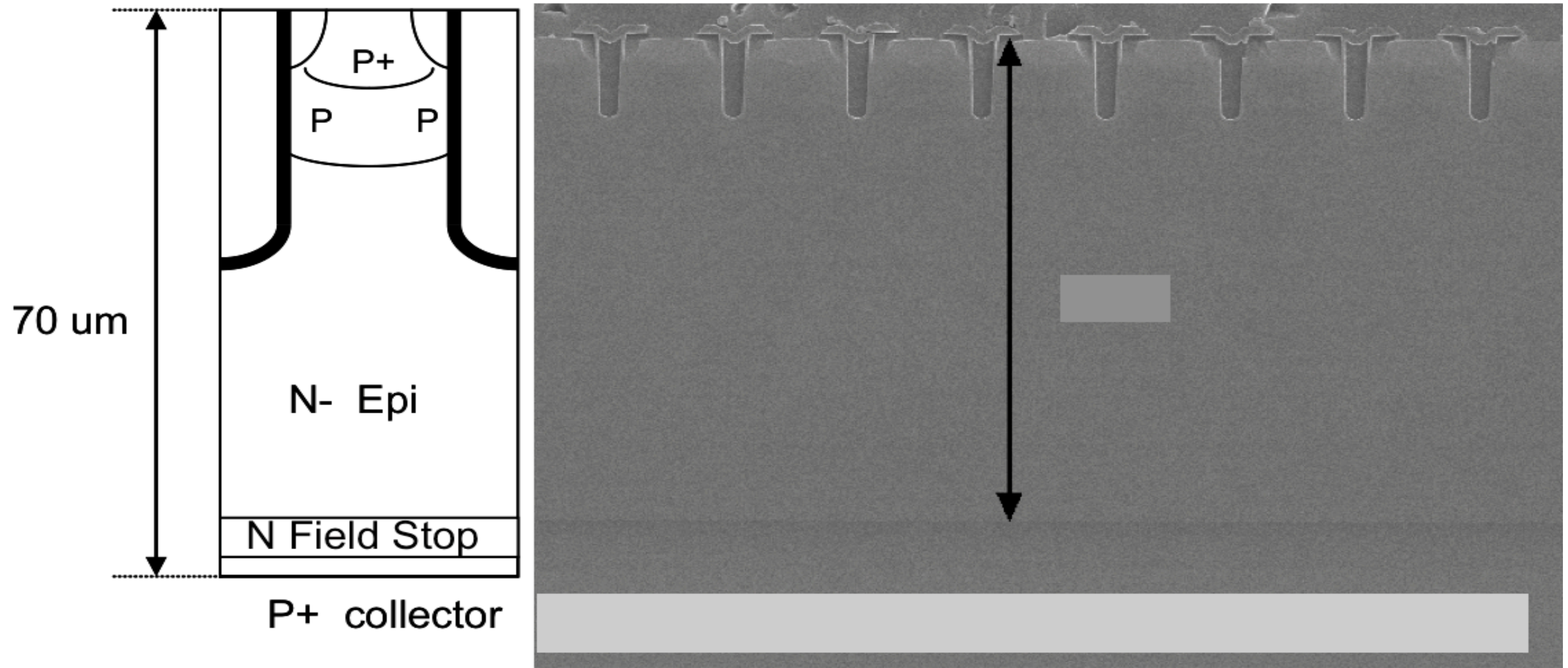




(Mike Briere – IRF)

Basic structure unchanged in many years. Cost reductions through manufacturing efficiencies. Mostly older nodes. CHEAP!

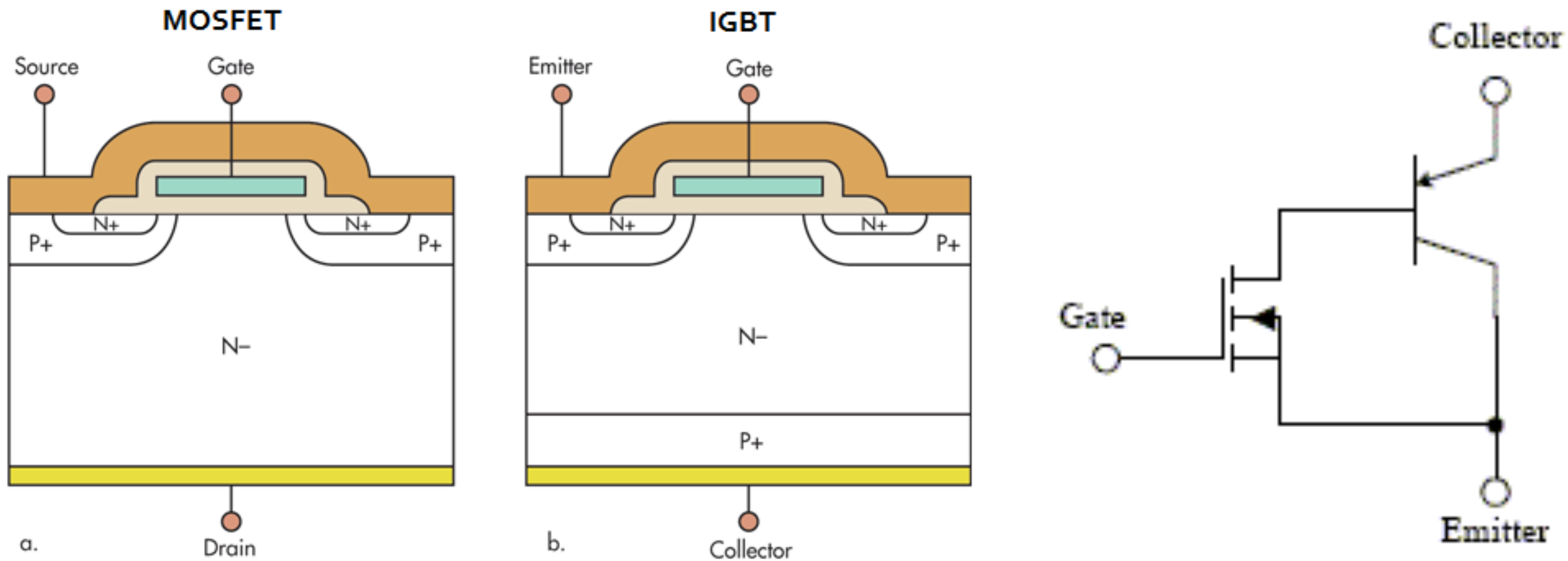
Silicon Trench Power IGBT
200 – 1200 Volts



(Mike Briere – IRF)

Basic structure unchanged in many years. Cost reductions through manufacturing efficiencies. Mostly older nodes. CHEAP!

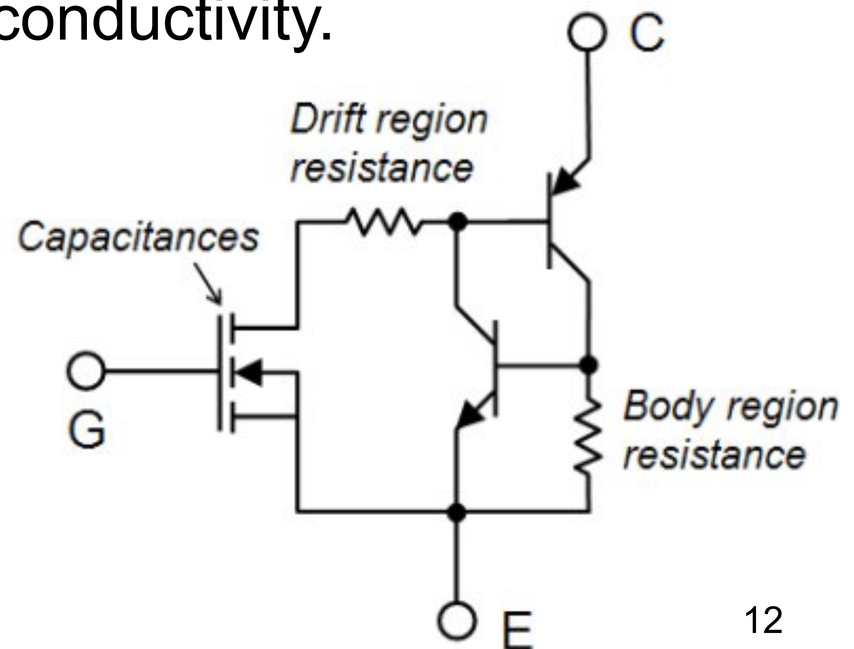
IGBT – Insulated Gate Bipolar Transistor



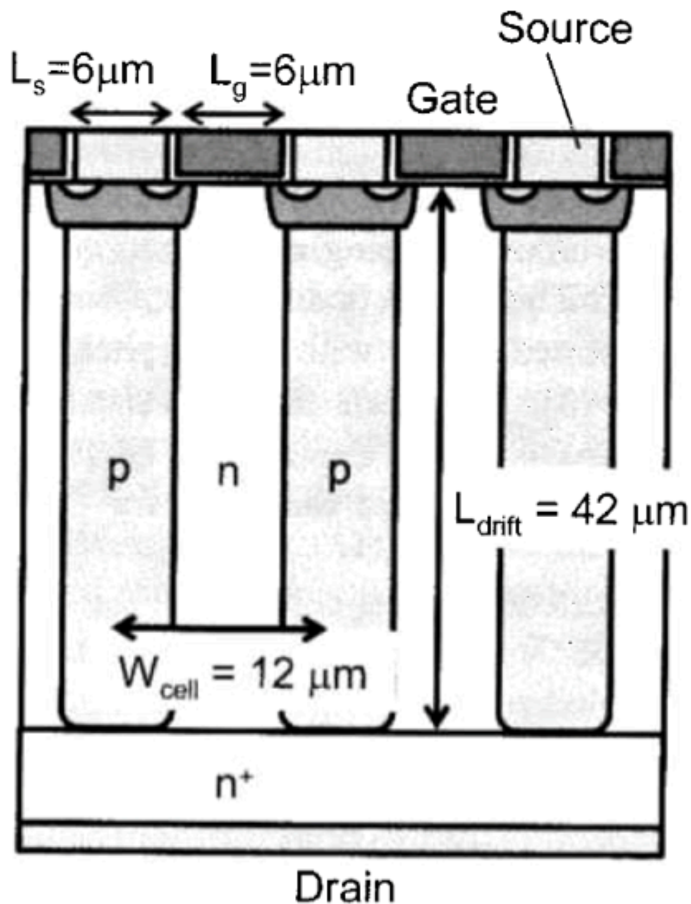
P^+ collector injects holes, increasing conductivity.

Parasitic thyristor exists in the structure. Optimization involves

1. Minimizing R so no latchup
2. Adjusting lifetime to balance switching speed and R_{ON}, (only in indirect BG materials).



Superjunction Vertical MOSFET
100 – 1000 Volts



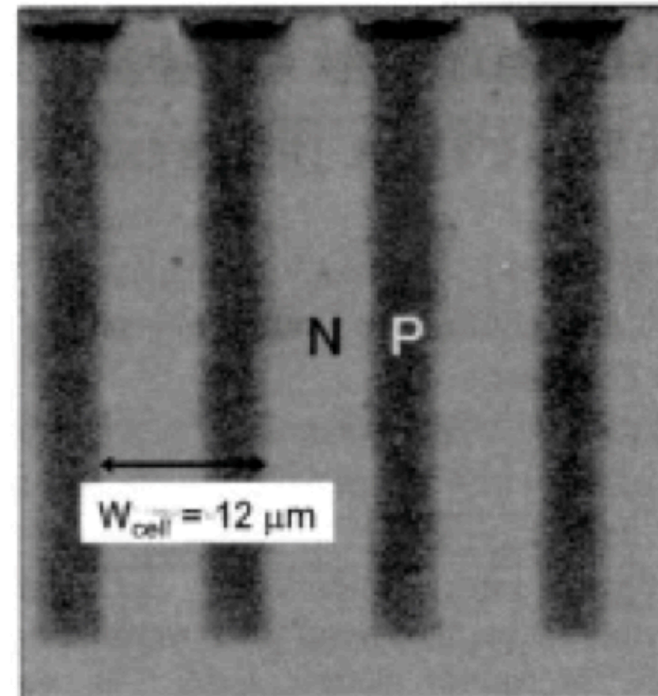


Fig. 2 SCM image of the fabricated SJ-MOSFET with the lateral pitch of 12 μm.

W. Saito et.al. (Toshiba) ISPSD 2004 p. 293

ISPSD 2004 p 293

Superjunction MOSFET

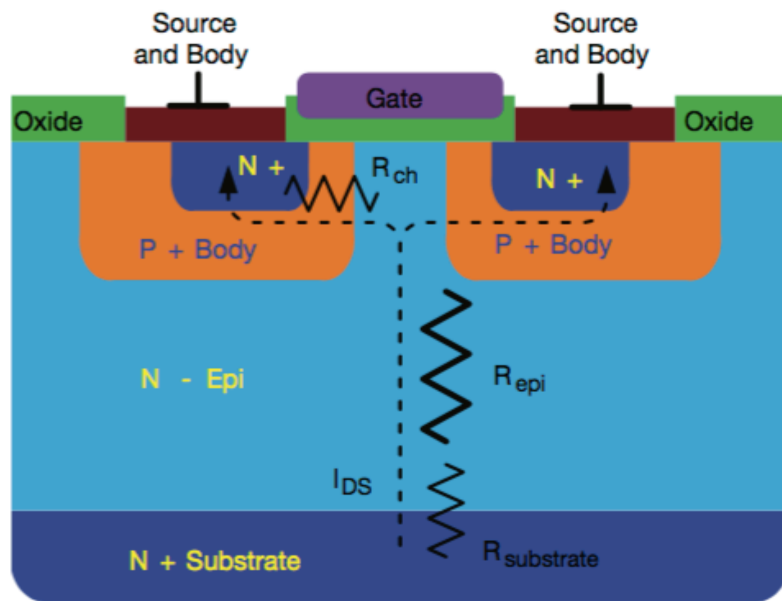


Fig. 1a - Conventional Planar MOSFET Structure

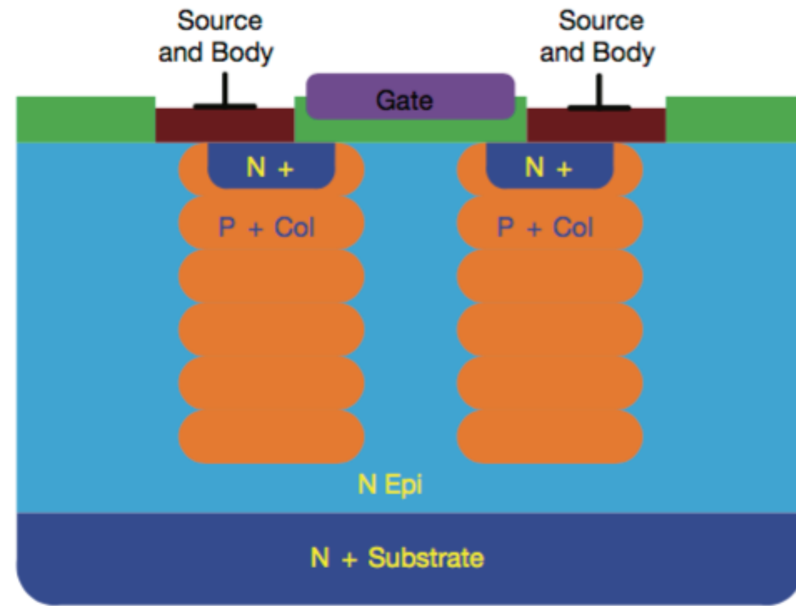


Fig. 2 - Superjunction MOSFET Structure

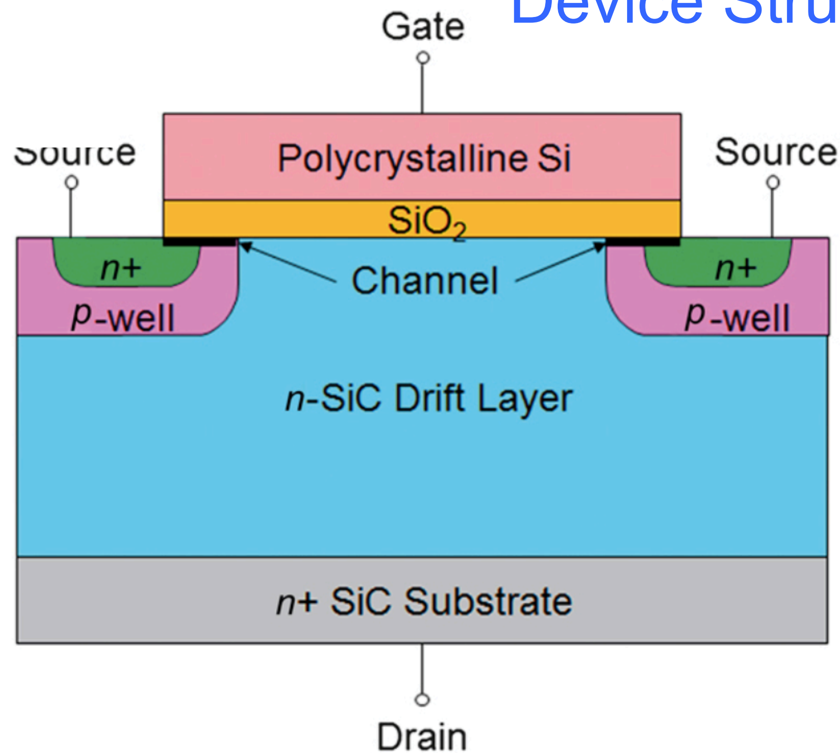
(Vishay Siliconix App. Note AN849)

- In a conventional power MOSFET, V_{dd} depletes N^- epi vertically. Increasing BV ⇒ thicker epi and lighter epi doping.
- In a superjunction power MOSFET, the N epi is fully depleted and charge balance occurs with P^+ columns. BV is proportional to epi thickness and N epi can be more heavily doped decreasing R_{epi}.

Will Silicon Power Devices Continue to Improve?

- The basic observation is often that Si power devices are "mature" and thus won't get much better.
- But because Si is the basis of the electronics industry, many $B in R&D continue to be spent each year. Some of this investment will likely result in Si power device improvements.
- Si will likely always be much better at integrating control with power devices. So major parts of the power market are simply not addressable by SiC and GaN at least in monolithic form.
- Cost will always be lower for Si power devices so cost sensitive applications will continue to use Si whenever possible.
- Bottom line – Si isn't going away. So what are the opportunities for SiC and GaN?

Device Structures in SiC



(F. Iacopi et al., MRS Bulletin, May 2015, pg. 390)

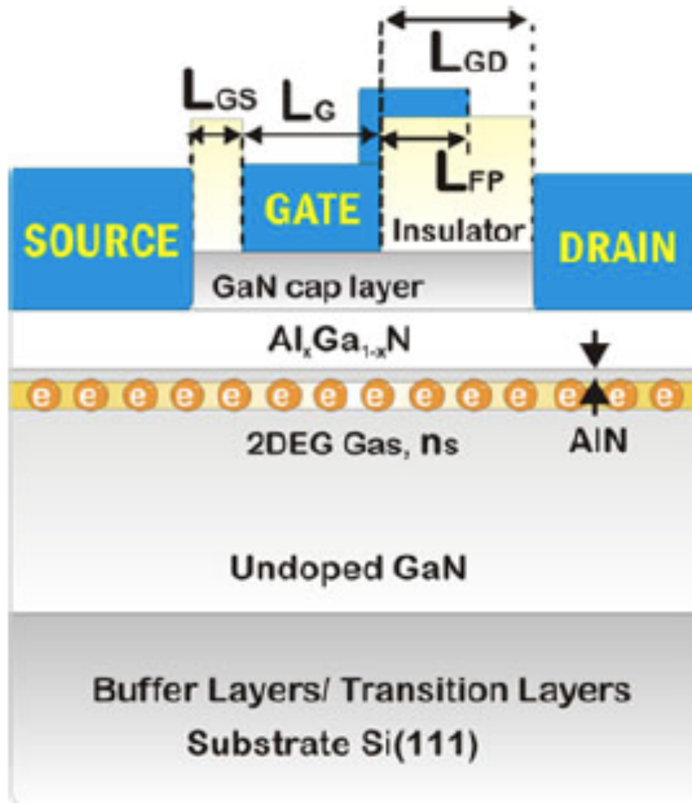
Bulk electron μ ≈ 1000 cm^2/Vsec
Bulk hole μ ≈ 150 cm^2/Vsec
Critical Field ≈ 3 MV/cm

Only E_{cr} is better than Si.

BUT – experimentally,
Inversion layer μ ≈ 20 cm^2/Vsec!!

- Primarily vertical MOSFET structures – similar to Si.
- Low V SiC MOSFETs ≈ same as Si (because of low channel μ). High V devices much better than Si.
- Vertical IGBT devices similar to Si structures, but beat Si in performance at high voltages.
- 6” SiC wafers are available, but expensive.

Device Structures in GaN



Bulk electron μ ≈ 1600 cm^2/Vsec
2DEG electron μ ≈ 2000 cm^2/Vsec
Bulk hole μ ≈ 175 cm^2/Vsec
Critical Field ≈ 3.5 MV/cm

E_{cr} is much better than Si.
2DEG μ is better than Si.

BUT – normally OFF devices have lower performance.

- Heteroepitaxy on Si, SiC limits GaN to lateral devices, < 1000 V.
- Basic device is depletion mode (normally ON).
- No large diameter GaN wafers available.

What Limits Adoption Rate of New Power Devices?

- First, quality, reliability and robustness must be demonstrated or there is no product, only a science project!
- Governing metric for market adoption = Performance/cost = P/C.
- For power semiconductors,

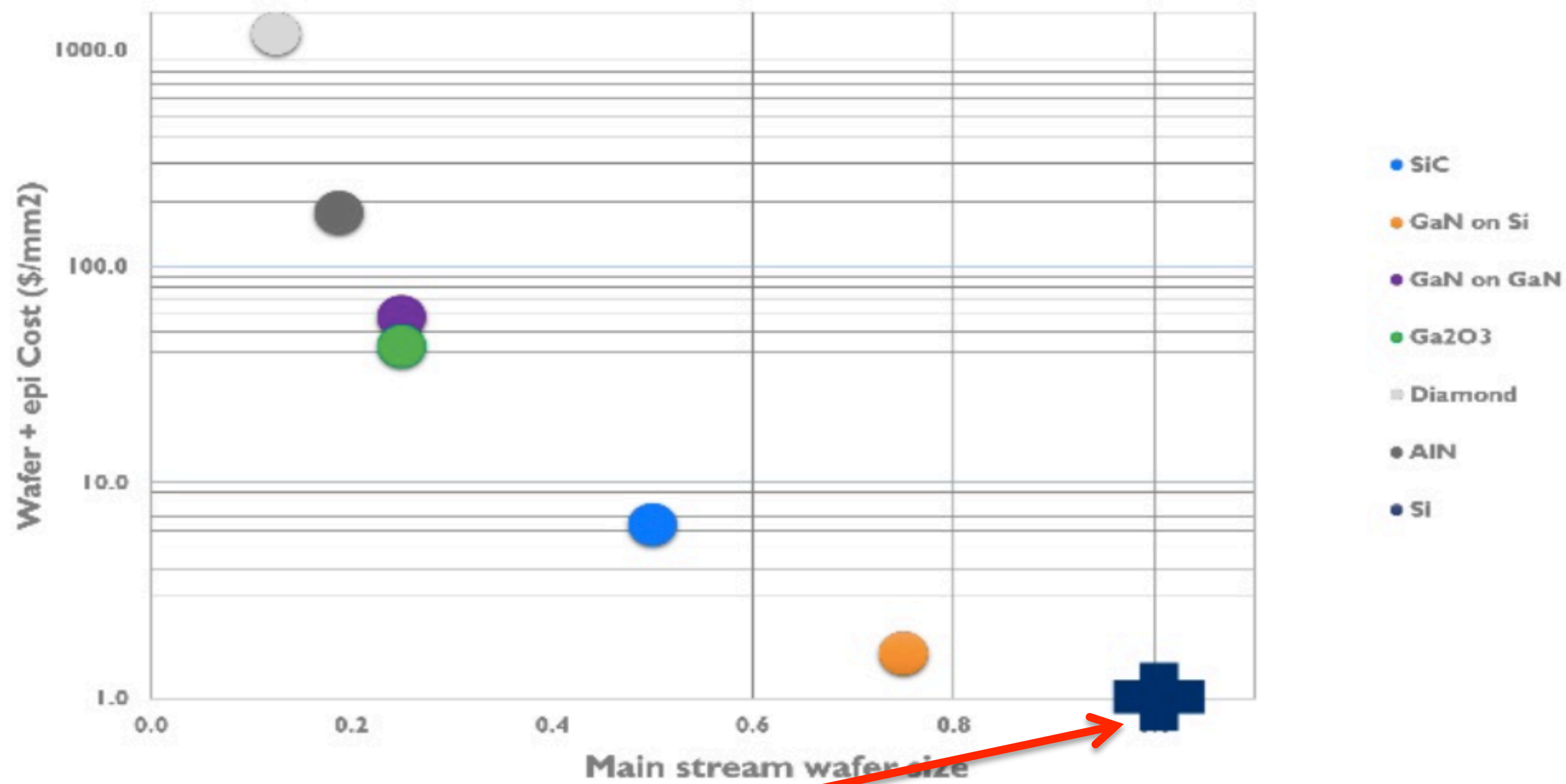
$$P/C = (\text{conduction loss})^{-1}(\text{switching loss})^{-1}/\text{Cost}$$

- For new switching materials/technologies, to displace Si in an existing application
  - If $P/C \leq 1$, niche market
  - If $P/C > 2\text{-}3X$, widespread adoption

Opportunities:

- Replace Si in existing applications – either P needs to be higher or C needs to be lower to achieve $P/C > 2\text{-}3X$.
- Enable new applications currently not achievable with Si.

Cost of Wafer Substrates

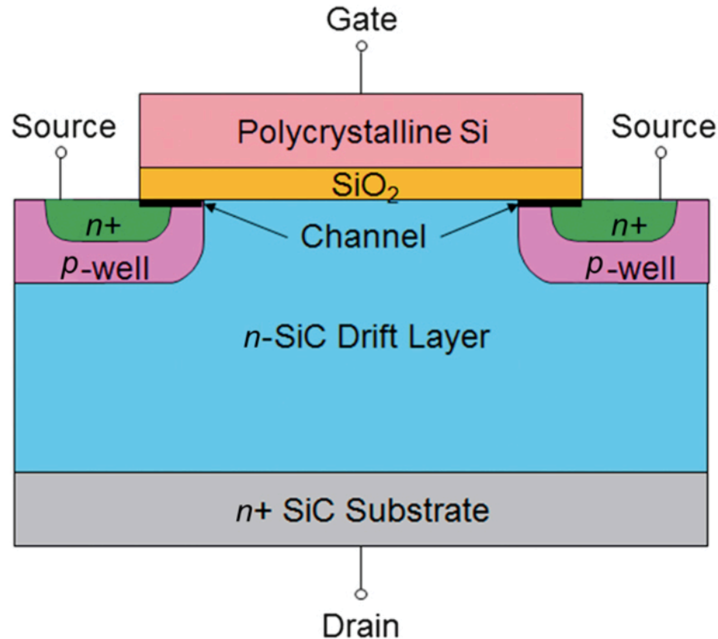


Nominalized with respect to 8-inch silicon wafer

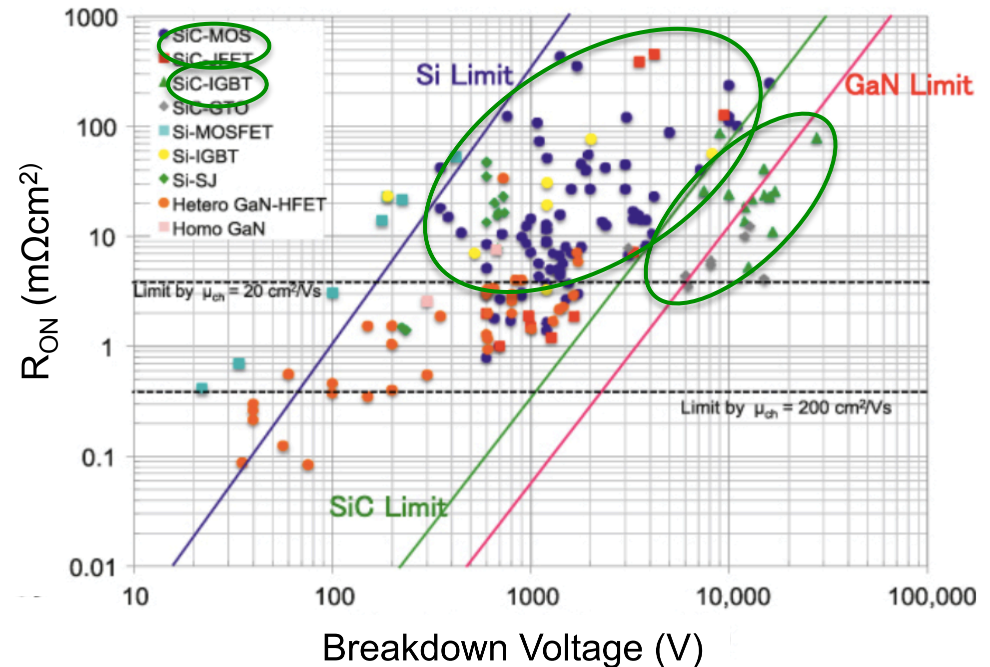
Semicon West 2017, Pierric Gueguen, Yole Développement

- Neither SiC nor GaN have a cost advantage with respect to silicon today, largely because of wafer costs.
- GaN may reach ≈ parity soon (because it’s on a Si wafer!)
- But these numbers don’t give GaN or SiC a P/C advantage.

What’s Needed To Increase Market Penetration by SiC Devices?



(F. Iacopi et al., MRS Bulletin, May 2015, pg. 390)



(H. Okumra, MRS Bulletin, Vol. 40, pg. 439,May 2015)

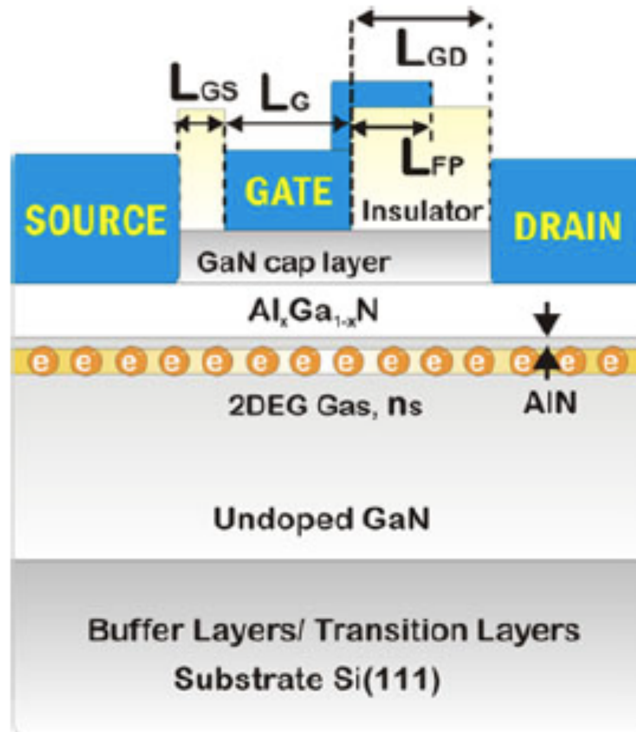
- SiC devices are often derated for reliability or material defect reasons, but still offer large performance advantages over Si.
- Material defect issues include micropipes and dislocations.
- Cost remains an issue – 6” SiC substrates are available but $$.
- SiC/SiO_2 interface not as good as Si/SiO_2 interface. ∴ lower μ than might be possible. ∴ Only high V SiC MOSFETs > Si.

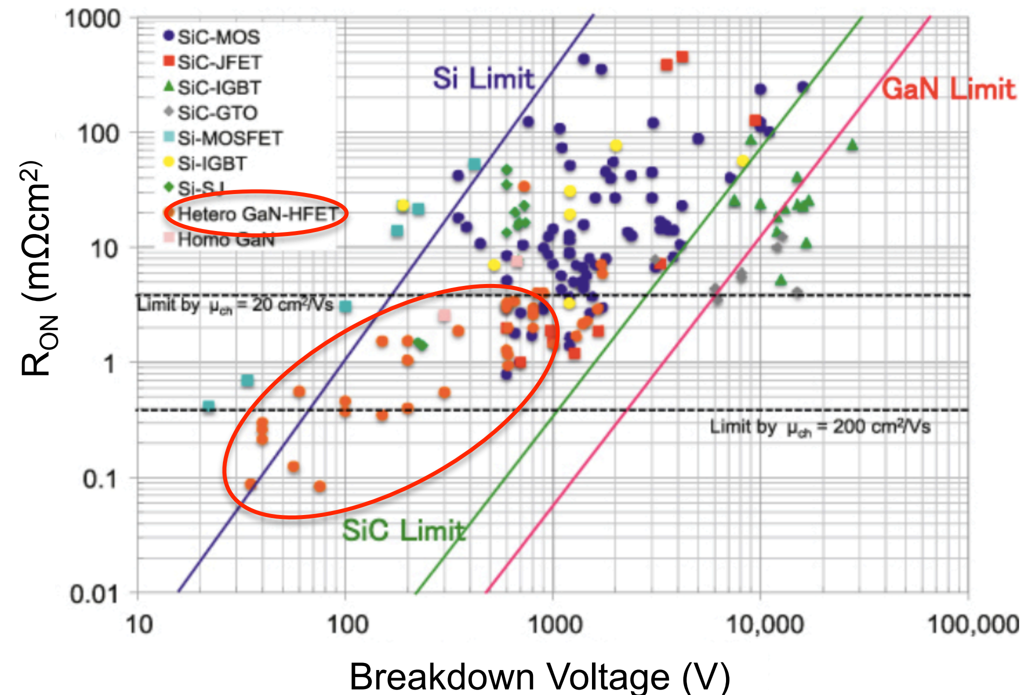
What's Needed To Increase Market Penetration by SiC Devices?

- Much progress has been made in reducing SiC crystal defects in substrates and in epi layers. But the quality is not nearly as good as Si wafers.
- The SiC/insulator interface still needs to be significantly improved to reduce interface states. Current low μ limits SiC MOSFETs to high voltage applications. In low V devices, the 10X smaller SiC channel μ mitigates SiC's ε_{CR} 10X advantage.
- Manufacturing costs are much higher than Si. A significant component of this cost is the starting wafer cost.

So currently P/C is not > 2-3X silicon and SiC is largely addressing markets where Si cannot compete or which are not cost sensitive and these markets are not huge!

What's Needed To Increase Market Penetration by GaN Devices?

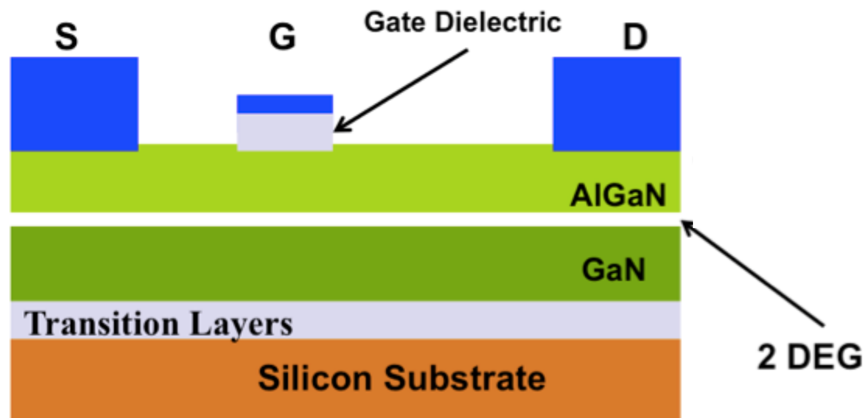




(H. Okumra, MRS Bulletin, Vol. 40, pg. 439,May 2015)

- GaN devices are primarily lateral HEMTs. This limits GaN applications to < 1000V. Most devices are far below GaN limit.
- Intrinsic device is normally ON. ∴ need Si MOSFET in a cascode configuration, or modified GaN gate structure which can degrade performance.
- Reliability issues remain with ON current collapse.

Enhancement Mode GaN Devices



What's Needed?

- V_T > 2 volts
- V_G > 10 volts
- Cascode circuit with Si MOSFET + GaN HEMT can achieve this.

Eliminate 2DEG under gate:

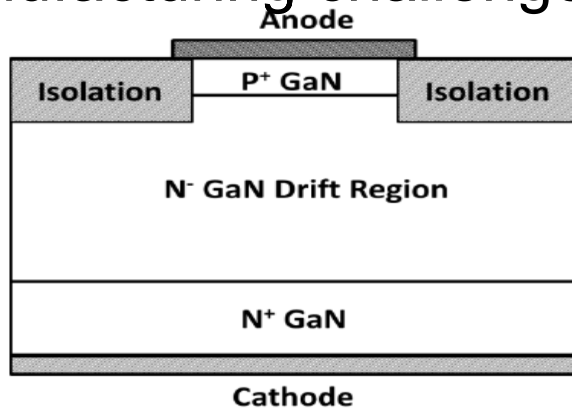
- Sub-critical barrier, e.g. recessed gate
- MOS-hybrid device
- Piezoelectric gate
- N-polar HEMT
- Lattice matched barrier (InAlN)

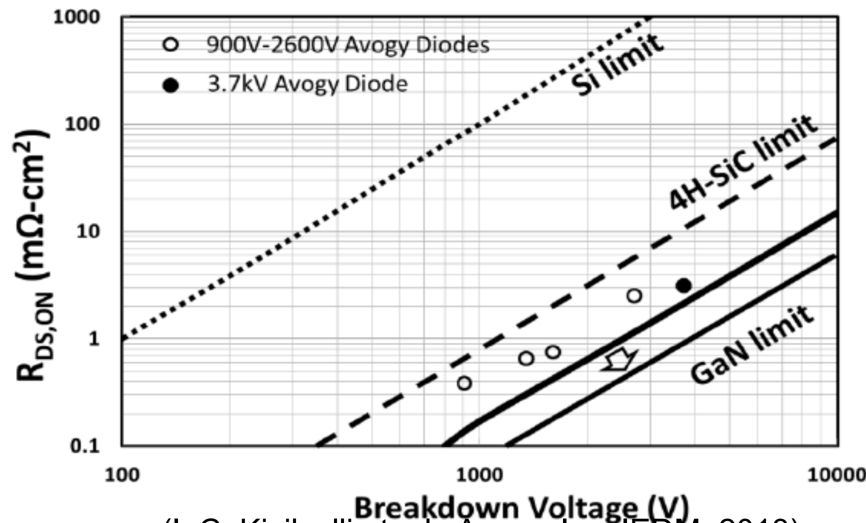
Negative charge between external gate electrode and 2DEG:

- PN junction (p GaN, p AlGaN under gate)
- Negative ions in insulator or barrier (e.g. F^-)
- Trapped electrons in gate insulator (floating gate or SiN-SiO_2)

Vertical GaN Devices
Homoepitaxy Examples

- The biggest challenge here is bulk GaN wafers. Only very small (2”) wafers currently available and the wafer manufacturing challenges are formidable.





(I. C. Kizilyalli et. al., Avogy, Inc. IEDM, 2013)

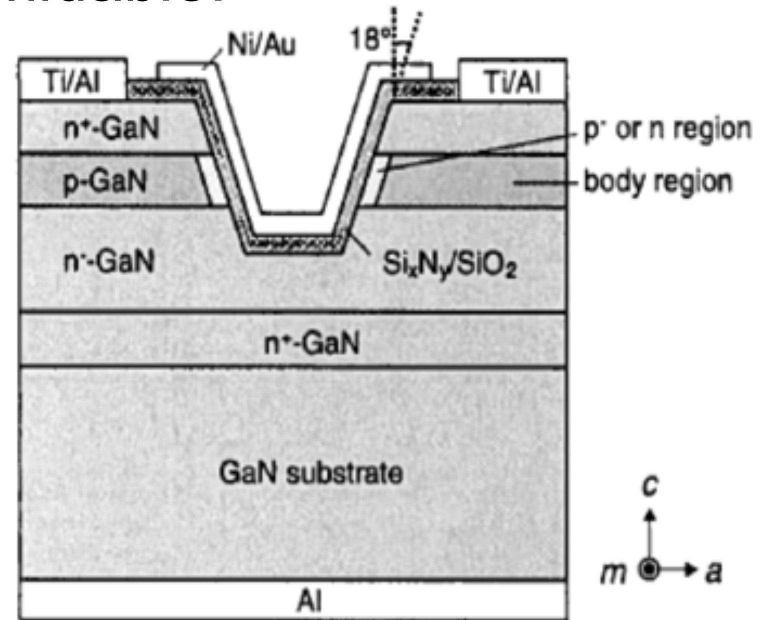


Fig. 2. Device structure of our trench gate MOSFET.

H. Otake et.al. APEX vol 1 (2008) p. 011105-1

What's Needed To Increase Market Penetration by GaN Devices?

- Much progress has been made in reducing crystal defects in GaN epi layers grown on Si. But the quality is not nearly as good as Si wafers. Si substrates are likely the best route to reduce lateral GaN HEMT manufacturing costs.

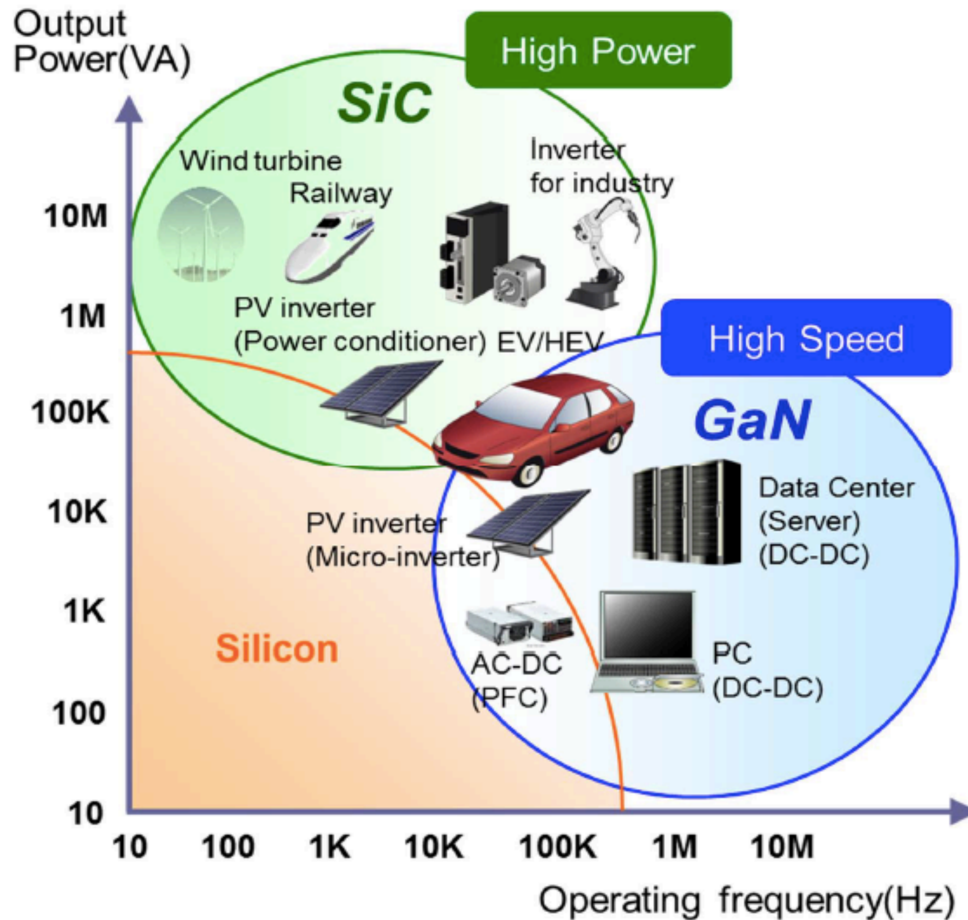
- Enhancement mode device structures need further development.

- Reliability, ON current collapse after high reverse bias, need further investigation.

- A breakthrough is needed in producing GaN bulk substrates.

So currently P/C is not > 2-3X silicon and GaN is largely addressing markets where Si cannot compete or which are not cost sensitive and these markets are not huge!

Current Market Opportunities for Gan and SiC



SiC for high power voltages (>1kV) with high current

GaN on Si for high frequency at mid-range voltages (<1kV)

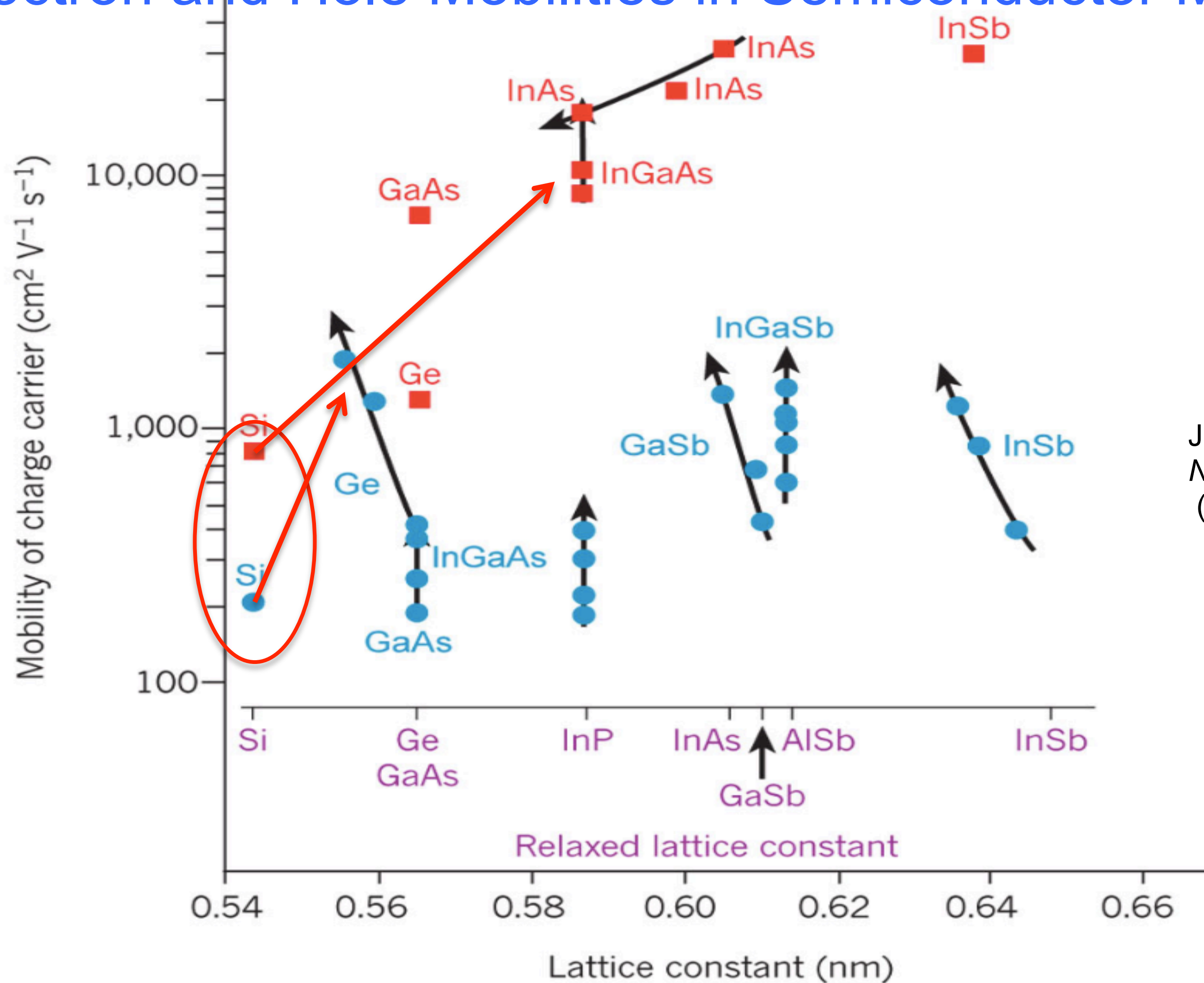
(Panasonic)

Given the current limitations of Gan and SiC in P/C, most applications are in regions where Si cannot compete.

The Situation Today

- GaN and SiC have very clear materials advantages over Si.
- In principle they allow power electronic components to be faster, smaller, more efficient and more reliable than Si parts.
- In principle they allow devices to operate at higher voltages, higher temperatures and higher frequencies than Si devices.
- Yet their market penetration is very small today. Some market projections (Lux) suggest Si will still have 87% of the power device market in 2024.
- What needs to happen to change this? Will it change?
- Perhaps there are some lessons we can learn from Si CMOS.

Electron and Hole Mobilities in Semiconductor Materials



Jesús A. del Alamo
Nature 479, 317–323
(17 November 2011)

Clearly there are higher performance materials than Si for logic applications. > 10X improvement in μ is possible.
NMOS ⟶ InGaAs, PMOS ⟶ Ge.

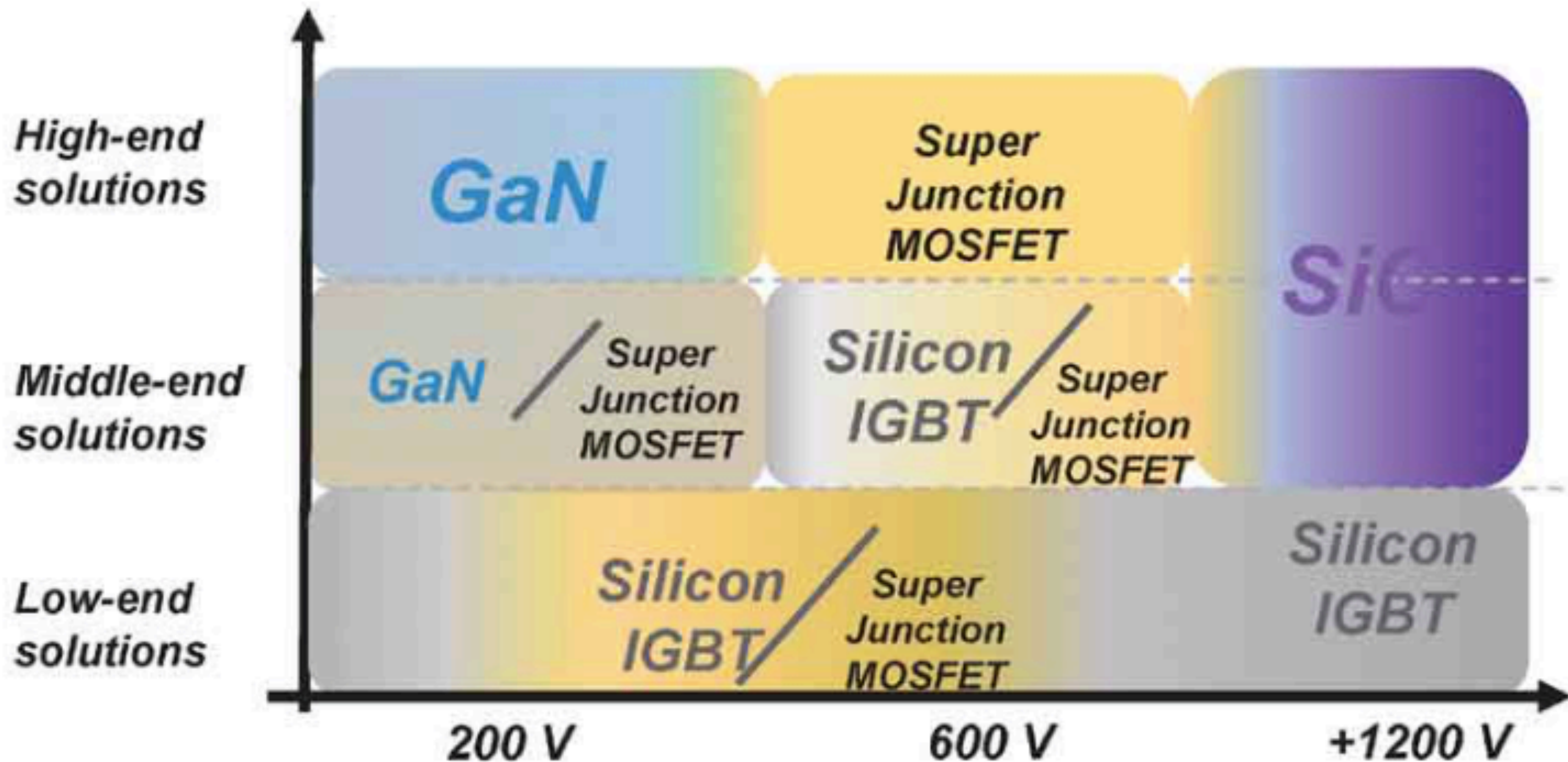
Higher Performance Materials for CMOS Logic

- Many demonstrations of higher performance III-V logic devices over the past 20 years. Also many demonstrations integrating these devices in a Si CMOS process flow.
- Yet it is unlikely that this transition will ever take place. Performance/Cost ratio not sufficient to justify manufacturing.
- Si CMOS has many advantages that offset lower mobilities:
  - “Ideal” semiconductor/insulator interfaces
  - Decades of manufacturing experience, ∴ low cost
  - Constant scaling, improving performance
  - Well understood reliability issues
  - III-V inversion layer μ not as high as bulk μ.
  - etc., etc.
- Many of these same arguments apply to Si vs. GaN or SiC power devices, except for the item in red above.

Where Have Other Materials "Competed" With Si CMOS?

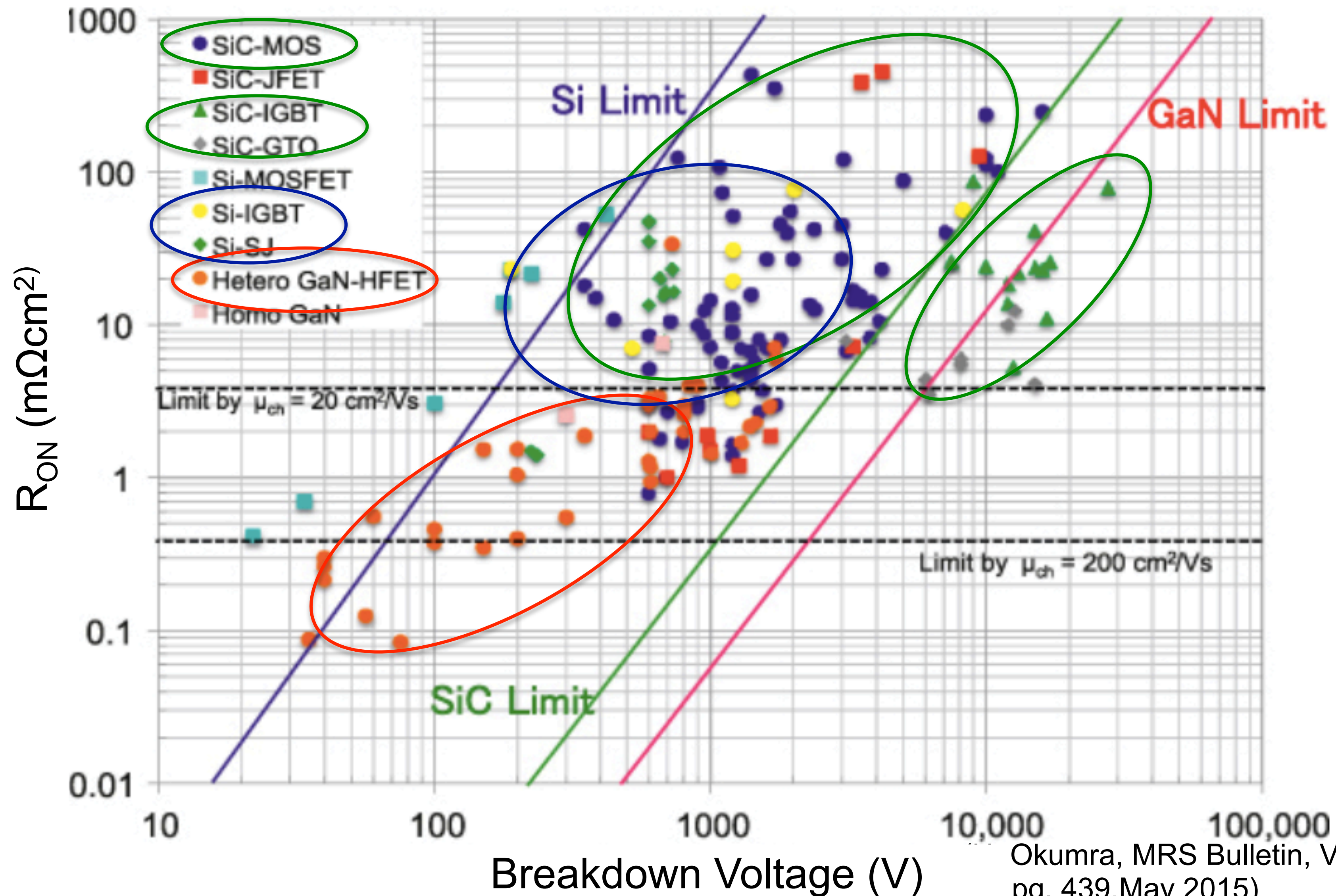
- III-V materials have other advantages besides μ.
  - Direct bandgaps.
  - Higher frequency operation possible.
- So even though III-V materials have not (and likely will not) displace Si in digital logic, they have
  - Dominated photonics markets where Si cannot compete.
  - Dominated high frequency communications markets where CMOS is too slow. (This is a moving target!)
- What's the lesson for GaN and SiC?
  - Look for markets Si power devices simply can't reach or which are not cost sensitive.
  - Grow scale, establish reliability, gain acceptance in these markets.
  - Drive manufacturing costs down through volume.

Yole Développement Technology Forecast



- Similar to the Panasonic market projection slide shown earlier.
- Given the current limitations of Gan and SiC in P/C, most applications are in regions where Si cannot compete.

Conclusions



Okumra, MRS Bulletin, Vol. pg. 439,May 2015)

- The potential for major disruption of the power semiconductor market clearly exists.

Conclusions

- As long as costs are significantly higher for SiC and GaN, market share will be difficult to win in existing applications. P/C is critical. Cost parity with Si will likely only be achieved with significant market penetration (scale).
- New technologies usually create new markets before they displace existing technologies in established markets.
- Some existing applications are less cost sensitive (usually very high performance markets). These are likely targets for early adopters.
- R&D on new circuits/packages/systems and new applications may be as important as R&D on devices and technology.

Thank you.

Questions?