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Supplementary information

A phased array based on large-area electronics that operates at gigahertz frequency

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Supplementary Information

A Phased Array based on Large-Area Electronics that Operates at Gigahertz Frequency

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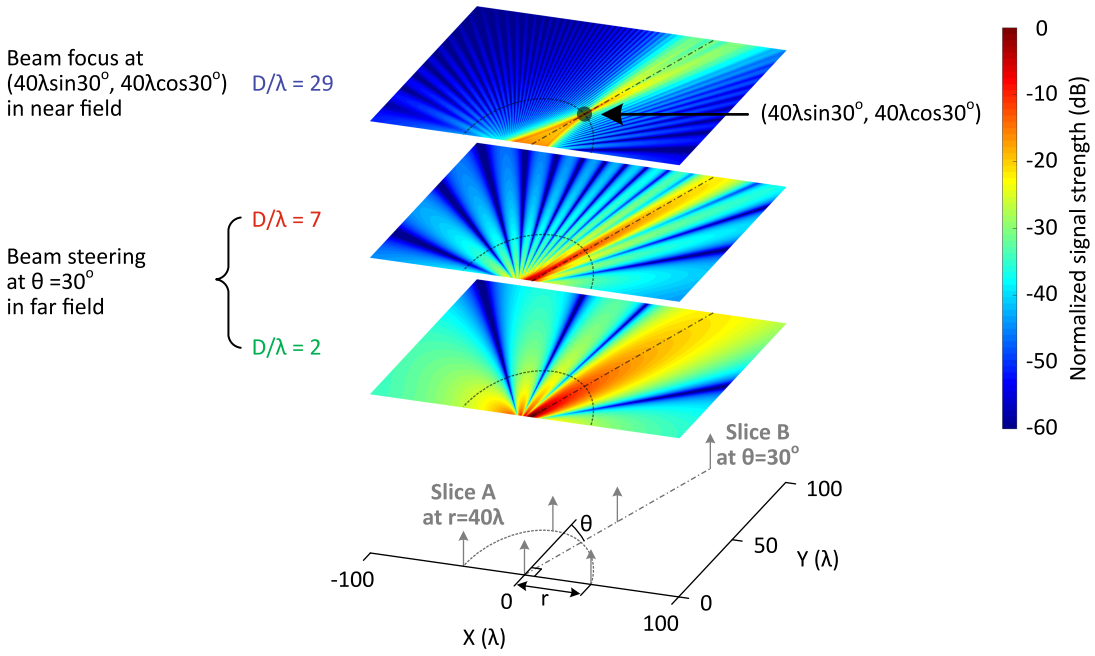
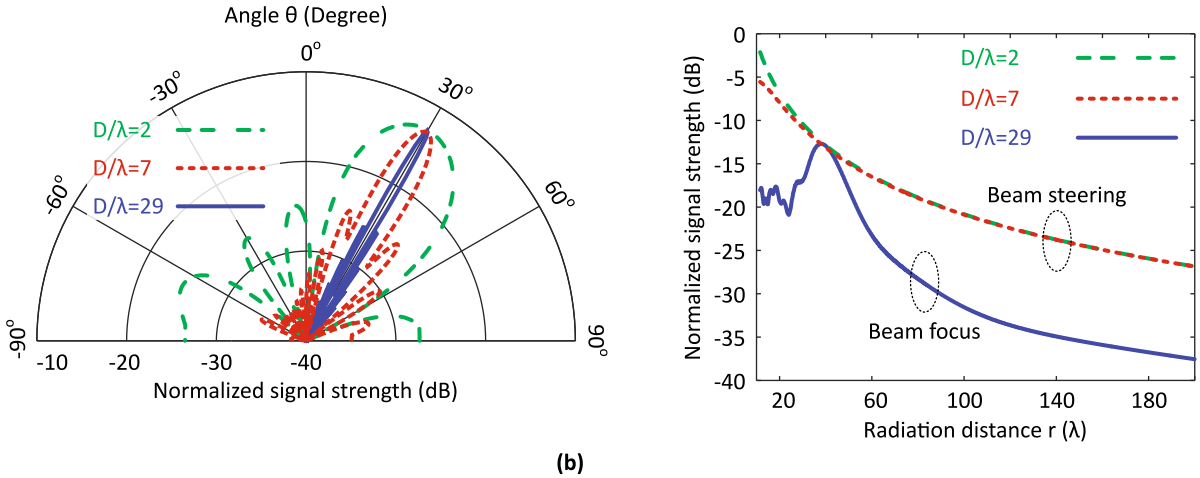
Supplementary Fig. 1
Radiation patterns of near-field beam focus and far-field beam steering.



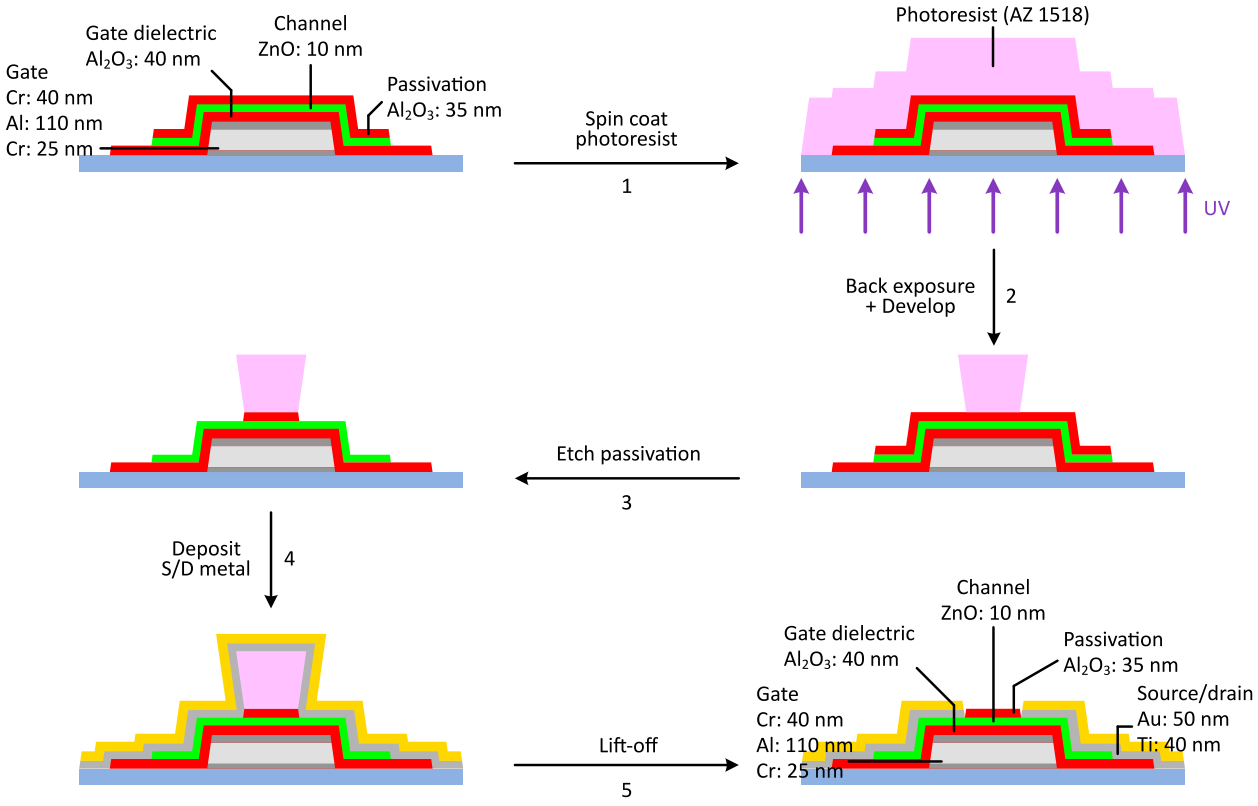
(a) 2D heat map of the modeled radiation patterns of a phased array with λ/2 spacing between antennas and different D/λ's. The signal strength is normalized by the number of antennas. In the two far-field cases (two plots at the bottom), the beam is steered to $\theta = 30°$, by setting the phase of each antenna i to satisfy $\Delta\phi_i - \Delta\phi_{i-1} = \pi sin\theta$ (where $\Delta\phi_i$ is the phase of the ith antenna). In the near-field case (plot at the top), the beam is focused at $(x = 40\lambda\, sin30°, y = 40\lambda\, cos30°)$, by setting the phase of the ith antenna to satisfy $-\frac{\Delta\phi_i}{2\pi}\lambda + d_i = n\lambda$, where d_i is the distance between the focus point and the ith antenna, and n is an integer.



(b)

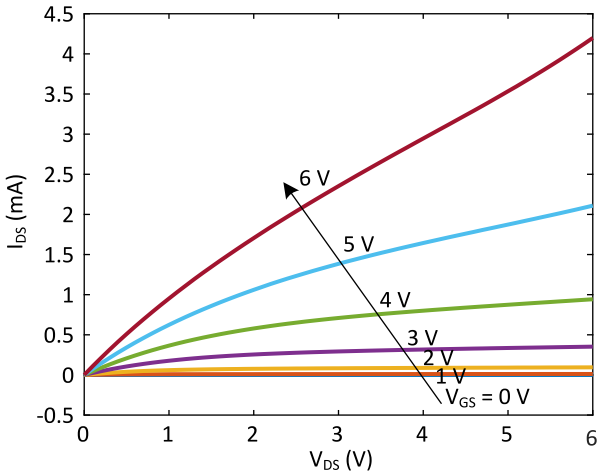
(b) 1D slices of the 2D radiation patterns in (a). Left: the slice A along θ when $r = 40\lambda$. **Right:** the slice B along r when $\theta = 30°$.

Supplementary Fig. 2
Self-aligned patterning of TFT source/drain.

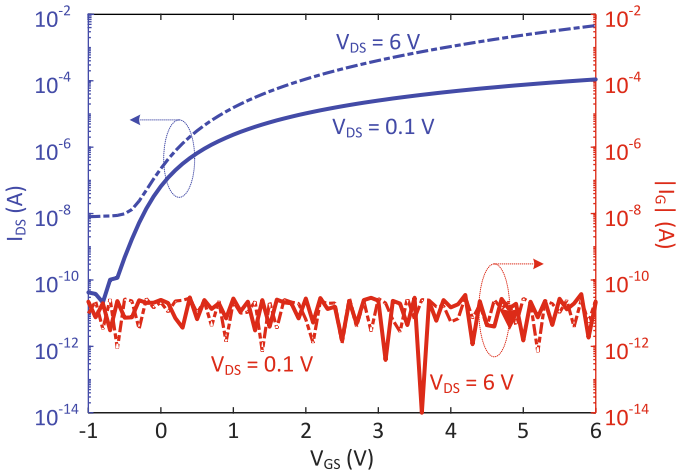


Start by patterning Cr/Al/Cr bottom gate electrode on a glass substrate. Cover the gate electrode with a stack of Al_2O_3/ZnO/Al_2O_3 layers by plasma-enhanced atomic layer deposition (PEALD), which is then patterned as islands. Next, spin coat positive photoresist (AZ 1518) and illuminate with UV light at the wavelength of 365 nm from the backside. Because ZnO and Al_2O_3 are transparent, all regions except above the gate electrode are exposed. Developing leaves photoresist only above the gate electrode. Etch away the passivating Al_2O_3 from everywhere else and thermally evaporate Ti/Au (40 nm/50 nm) for source/drain contacts. Lift off the remaining photoresist and metal above the channel. The diffraction of the UV light leaves the channel slightly narrower than the gate electrode, leading to minimal overlap between gate and source/drain.

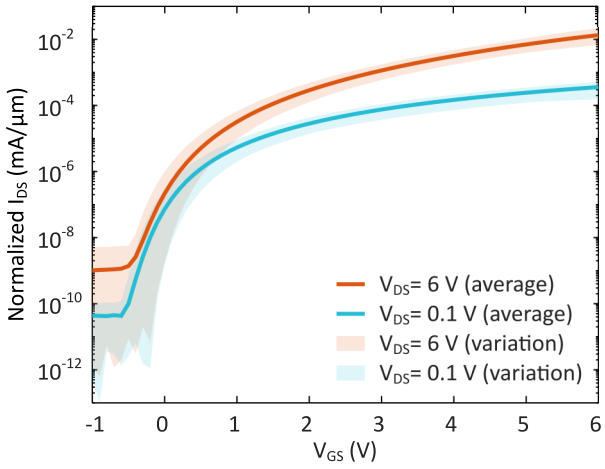
Supplementary Fig. 3
DC performance of ZnO TFTs and X-ray diffraction characterization of ZnO thin film.



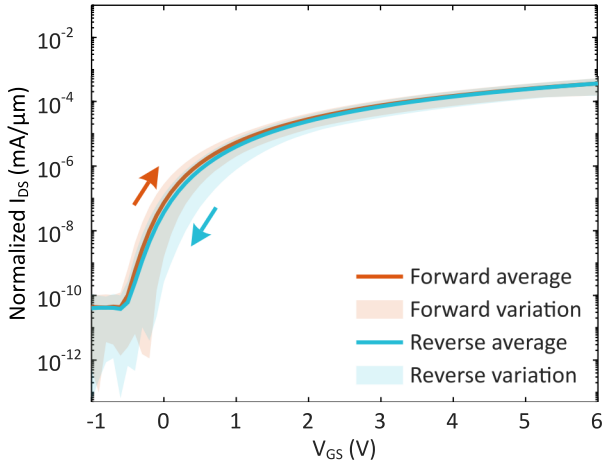
(a) $I_{DS} - V_{DS}$ output curve of ZnO TFT with $W_{TFT}/L_{TFT} = 150\ \mu m/0.7\ \mu m$.



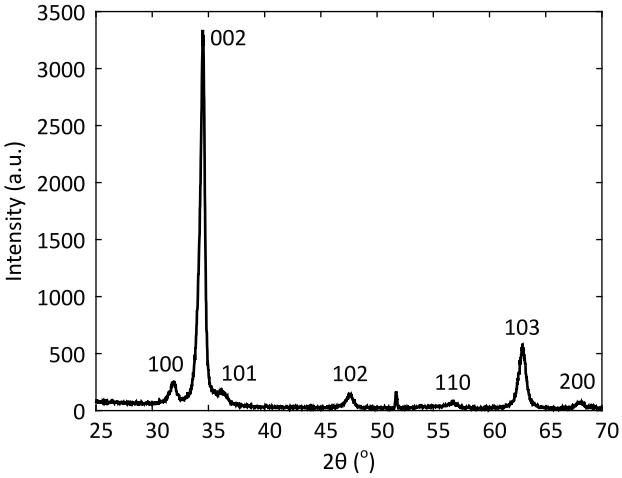
(b) $I_{DS} - V_{GS}$ transfer curve and gate leakage of ZnO TFT with $W_{TFT}/L_{TFT} = 150\ \mu m/0.7\ \mu m$.



(c) $I_{DS} - V_{GS}$ transfer curve across 50 ZnO TFTs with $L_{TFT} \approx 1\ \mu m$. The solid line shows average while shaded region shows the maximum/minimum boundary. The field-effect mobility and threshold voltage are extracted to be 11 $cm^2/V{\cdot}s$ and 2.3 V on average with standard deviations of 3.8 $cm^2/V{\cdot}s$ and 0.2 V, respectively. They are extracted by extrapolation and from the slope of the $\sqrt{I_{DS}} - V_{GS}$ curve in the saturation regime.

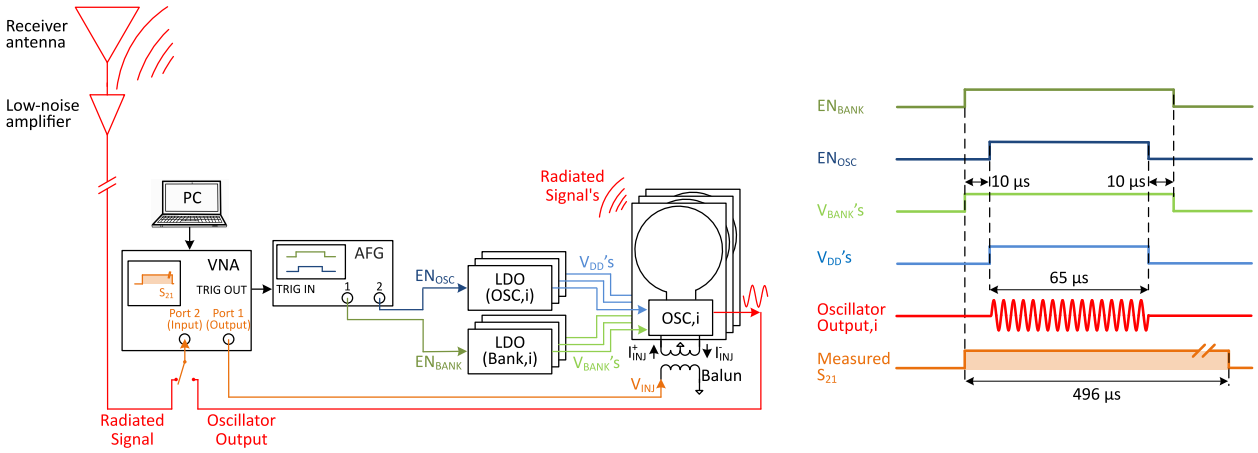


(d) Forward- and reverse-sweep of $I_{DS} - V_{GS}$ across 50 ZnO TFTs with $L_{TFT} \approx 1$ μm at $V_{DS} = 0.1\ V$. The solid line shows average while shaded region shows the minimum/maximum boundary.



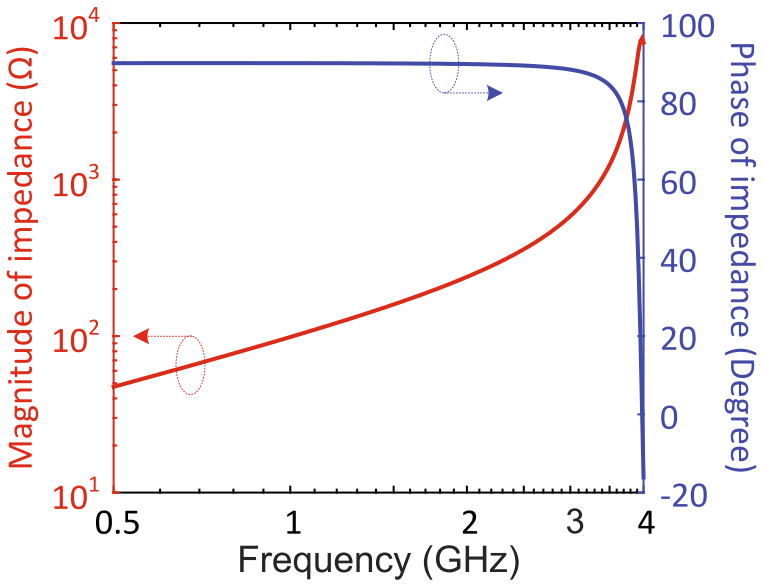
(e) Measured X-Ray Diffraction (XRD) results for 100 nm-thick ZnO deposited by PEALD. The grain size was estimated by Scherrer equation, to be $d = \frac{K\lambda}{\beta cos\theta} = 15\ nm$, where $K \approx 0.9$ is the shape factor, $\beta = 0.57^o$ is the full width of half maximum at the 002 peak, $\theta = 17.25^o$ is the Bragg angle at the 002 peak, and $\lambda = 1.5406$ Å is the wavelength of X-ray used. Because the grain size is much less than TFT channel dimensions, TFT variations are unlikely due to the polycrystalline nature of ZnO, and instead likely due to the variations in film thickness, electron mobility, and contact resistance.

Supplementary Fig. 4
Test setup for measuring radiation pattern.

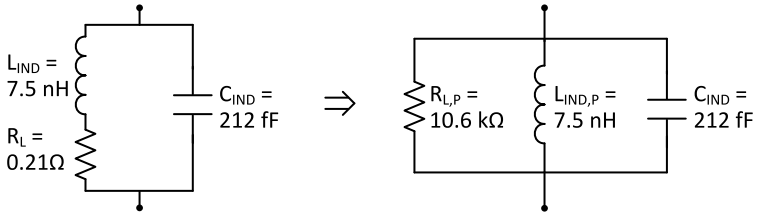


The system test setup consists of the phase-tunable oscillators (OSC,i's) that form the phased array, an arbitrary function generator (AFG), a vector-network analyzer (VNA), low-dropout voltage regulators (LDO's), and a receiver antenna followed by a low-noise amplifier. The tests are controlled by a PC. First, the PC starts the two-port scattering measurement in the VNA, which immediately triggers the AFG. Then the AFG generates an 85 µs-wide pulse, which enables the voltage regulators that provide the bias voltage V_{BANK} to the capacitor banks; 10 µs later, the AFG enables the voltage regulators that power up the oscillators (V_{DD}'s) for 65 µs. The oscillations generate EM radiation. Simultaneously the VNA sends the injection-locking signal to the oscillators from Port 1 via a balun (to generate the differential signals $V_{INJ}^{\pm}$), such that the oscillators are frequency-synchronized and phase-tuned referring to the injection-locking signal via their 4-bit digital codes. The output of the amplifier following the receiver antenna is connected back to Port 2 of the VNA and hence the amplitude of the radiated signal is measured as the S_{21} parameter.

Supplementary Fig. 5
Analysis of loop inductor.

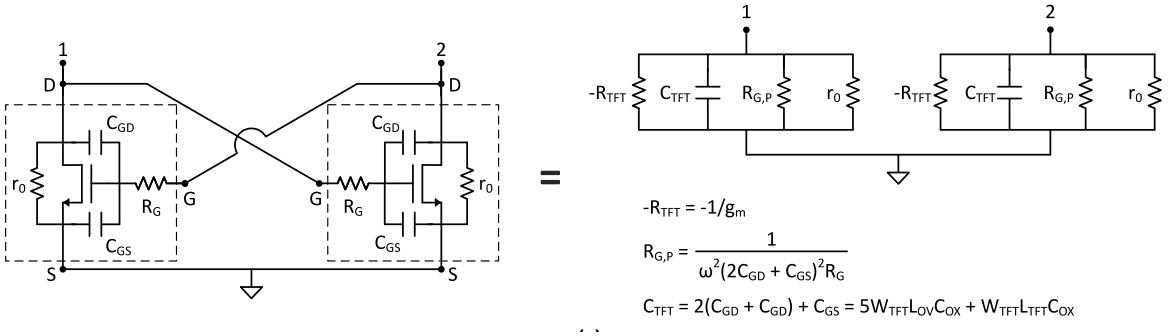


(a) Simulated impedance of the loop inductor. The 3D electromagnetic simulation was performed using Ansys HFSS. The inductor was made of 35-μm-thick, 0.9-mm-wide, 4-mm-radius copper trace on PCB. The inductance is extracted at low frequencies to be 15 nH; the self-capacitance, calculated from the self-resonance frequency $C_{SELF} = \frac{1}{\omega^2 L}$, is 106 fF. These values correspond to an inductance of 7.5 nH and a capacitance of 212 fF for each branch of the differential oscillator.

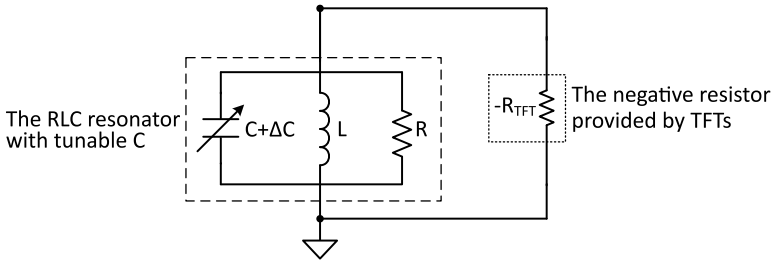


(b) Circuit model of the loop inductor. The parallel-to-series transformation is performed at 1 GHz.

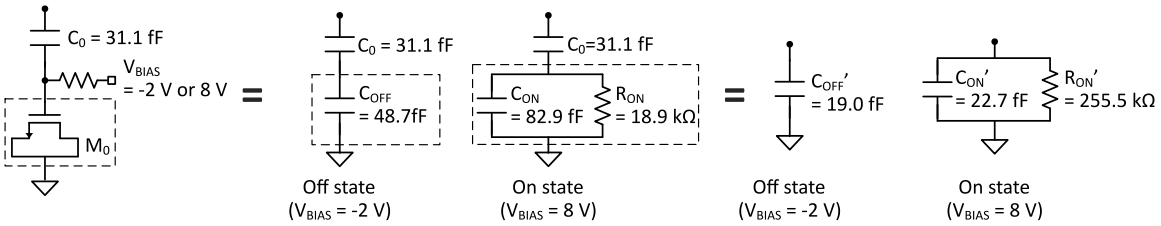
Supplementary Fig. 6
Analysis of LC cross-coupled oscillator with phase tunability.



(a) Analysis of cross-coupled TFTs. Left: circuit diagram of cross-coupled TFT pair with parasitics. R_G is the resistance of the gate electrode. C_{GS} is a combination of gate-source overlap capacitance and gate-channel capacitance, $C_{GS} = W_{TFT}L_{OV}C_{OX} + W_{TFT}L_{TFT}C_{OX} + C_{METAL}$, where W_{TFT} is channel width, L_{TFT} is the channel length, L_{OV} is the overlap length, C_{OX} is the capacitance per unit area, and C_{METAL} is the capacitance due to the overlaps between different metal layers in the layout. C_{GD} is the gate-drain overlap capacitance, $C_{GD} = W_{TFT}L_{OV}C_{OX}$. r_0 is the output resistance of the TFT in the saturation region. **Right: equivalent circuit of cross-coupled TFT pair.** By series-to-parallel transformation and vice versa, the circuit is translated into a parallel network at a fixed frequency of 1 GHz, which consists of: (1) a negative resistor $-R_{TFT}$; (2) a capacitor C_{TFT} (the factor 2 for C_{GD} is due to the Miller effect); (3) a resistor $R_{G,P}$, representing gate resistance in the parallel network; and (4) a resistor r_0.



(b) Conceptual diagram of LC cross-coupled oscillator.

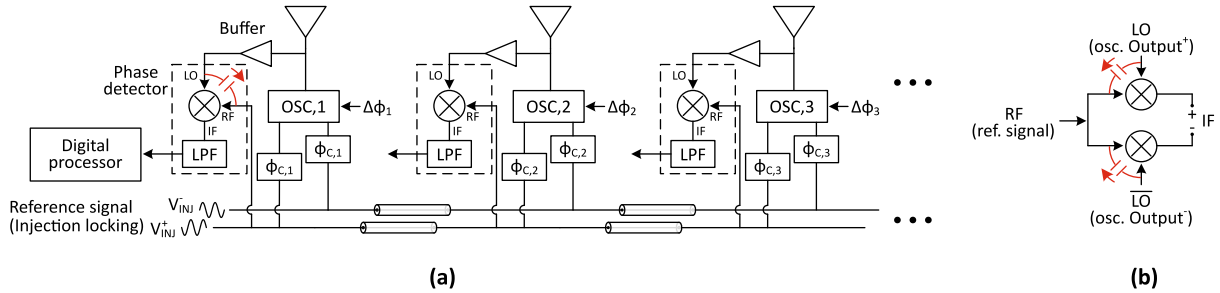


(c)

(c) Model of capacitor bank. The capacitor bank is binary-weighted; namely, the *i*th bit consists of 2^i duplicates of the basic capacitance-tuning unit. As shown above, the unit is a tunable MOS-capacitor M_0 in series with a fixed capacitor C_0. The fixed parallel-plate capacitor C_0 is made with a 40 nm-thick Al_2O_3 dielectric sandwiched between two metal pads with 3 μm × 3 μm overlap. C_0 decouples the DC bias voltage from the oscillator. The MOS-capacitor M_0 is a TFT whose W_{BANK}/L_{BANK} is 30 μm/1 μm, with its source and drain shorted. Its capacitance is controlled by a digitalized DC bias voltage V_{BIAS} (Fig. 4d). At $V_{BIAS} = -2$ V, the TFT is turned off; then the impedance of the MOS-capacitor M_0 is purely capacitive due to gate-source/drain overlap, represented by a capacitor C_{OFF}. At $V_{BIAS} = 8$ V, the TFT is turned on with its channel becoming conductive, thus an additional gate capacitance is introduced. Because of the finite conductance of the channel, the overall impedance is a mix of capacitance and resistance, represented by a parallel network of R_{ON} and C_{ON}. Therefore, at a fixed frequency of 1 GHz, by parallel-to-series transformation and vice versa, the impedance of the bank can be modeled as: (1) $C_{OFF}{}'$ at $V_{BIAS} = -2$ V; (2) a parallel network of $R_{ON}{}'$ and $C_{ON}{}'$ at $V_{BIAS} = 8$ V. The values listed in the circuits above were extracted from the measured data in Fig. 4d.

Supplementary Fig. 7
Proposed integrated calibration architecture.

As mentioned, an integrated calibration mechanism will ultimately be needed to compensate for non-idealities such as device drift, temperature changes, manufacturing variations, etc. Calibration essentially involves two steps: phase detection and phase tuning. While demonstration of an integrated calibration mechanism is left as future work (namely exploring appropriate circuit topologies for phase detectors and shifters that are suited to the limited f_T of TFTs), an approach that can be adapted for future integrated systems is presented.



(a) Proposed architecture for integrated calibration. (b) Differential implementation of the mixer to cancel LO-to-RF feedthrough.

The proposed architecture is shown above. The phase error is measured by a detector, which converts the phase difference between a reference signal and each oscillator to a DC voltage, and then fed to a digital processor. Phase tuning is performed by inserting a fine-phase-tuning circuit between the reference signal and the oscillator, i.e., $\phi_{C,i}$ ($i = 1, 2, 3, ...$), controlled by the digital processor, in response to the phase error detected.

The phase detector can be realized by a mixer with a low-pass filter. Mixers are feasible using transistors or diodes, as previously demonstrated[1,2]. Particularly in LAE technology, high device parasitic capacitances are a concern, which create an unwanted local oscillator (LO) to RF feedthrough path (indicated by the coupling capacitor in red in **(a)**) and lead to self-mixing of the LO signal and offset of the DC output. To address this, as shown in **(b)**, a fully-differential implementation can be employed to cancel the parasitic

capacitive conduction paths[3,4,5], taking advantage of the differential output available in the LC oscillator.

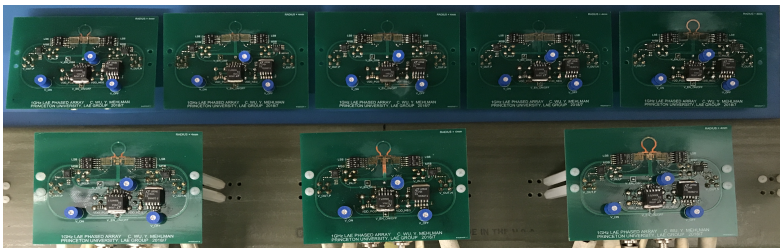
The phase shifter can be realized as switched transmission lines via RF switches. While a typical drawback of this approach is its large area, this is of reduced concern in LAE (compared to conventional technologies such as Si-CMOS). A key challenge, however, is the implementation of gigahertz RF switches. As shown in Fig. 1d, the f_T of TFTs is limited to well below 1 GHz[†]. One way to address this is through a resonant switch, employing an inductor in parallel with the TFT, to negate parasitic capacitances by taking advantage of high-quality-factor inductors possible in LAE thanks to large geometries as well as low-loss metal traces and substrates. While this trades off bandwidth, such a trade-off is often acceptable in phased arrays, employing a specific narrow frequency range for proper geometric construction of radiation patterns.

[†]The small-signal analysis of a TFT shows $f_T = \frac{g_m}{2\pi(C_{GS}+C_{GD})}$, where g_m is transconductance, and C_{GS}/C_{GD} is gate-to-source/drain capacitance. When a TFT is used as a switch, the cut-off frequency is $\frac{1}{2\pi R_{ON} C_{GD}} \approx \frac{g_m}{2\pi C_{GD}}$, where R_{ON} is its channel resistance while the TFT is turned on. As a result, the cut-off frequency of a TFT as switch is not exactly f_T but higher by a factor of $(C_{GS} + C_{GD})/\, C_{GD} \approx 3$ (assuming channel length is 0.7 μm and gate-to-source/drain overlap is 0.7 μm, as in this work).

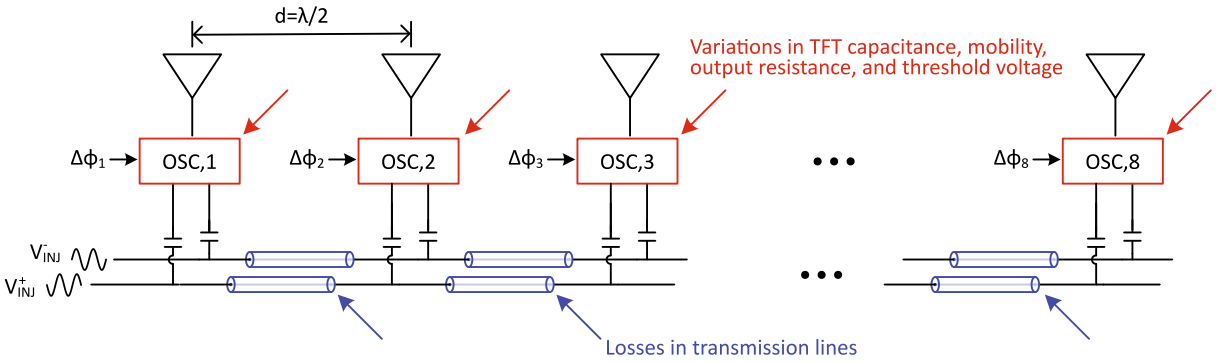
Supplementary Fig. 8

Simulation of an 8-element phased array (with ideal omnidirectional antennas).

A simulation of an 8-element phased array is performed to assess feasibility of scaling up the system. The non-idealities, such as device variations (extracted from the measurements of 8 individual elements) and losses in transmission lines are modeled in the simulation. Scaling-up from Fig. 2a, the 8-element architecture is shown in **(b)**, pointing out the non-ideal factors considered. The capacitance, mobility, and threshold voltage variation with standard deviations of $\sigma_C = 39\ fF$ (measured from eight oscillators built as shown in **(a)**), $\sigma_\mu = 3.8\ cm^2/V \cdot s$ (from Supplementary Fig. 3c), and $\sigma_{V_T} = 0.20\ V$ (from Supplementary Fig. 3c), and a loss of 1.8 dB/m at 1 GHz in the transmission lines (from EM simulation of a microstrip with 50 Ω characteristics impedance) are included.



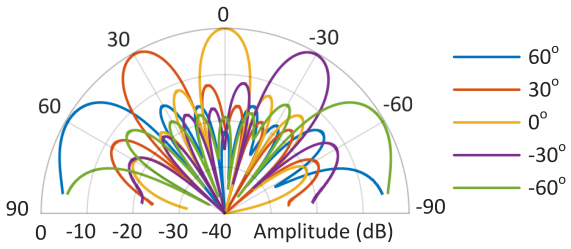
(a) Photograph of 8 phase-tunable oscillators built and measured.



(b) Simulated 8-element system architecture with non-ideal factors noted.

Capacitor banks with 4-bit precision are used (Fig. 4b). To address the offset in phase due to the capacitance variation, two redundant bits (of equal MSB weight) are used to counter variation in the free-running frequency of the oscillators. To steer the beam to a

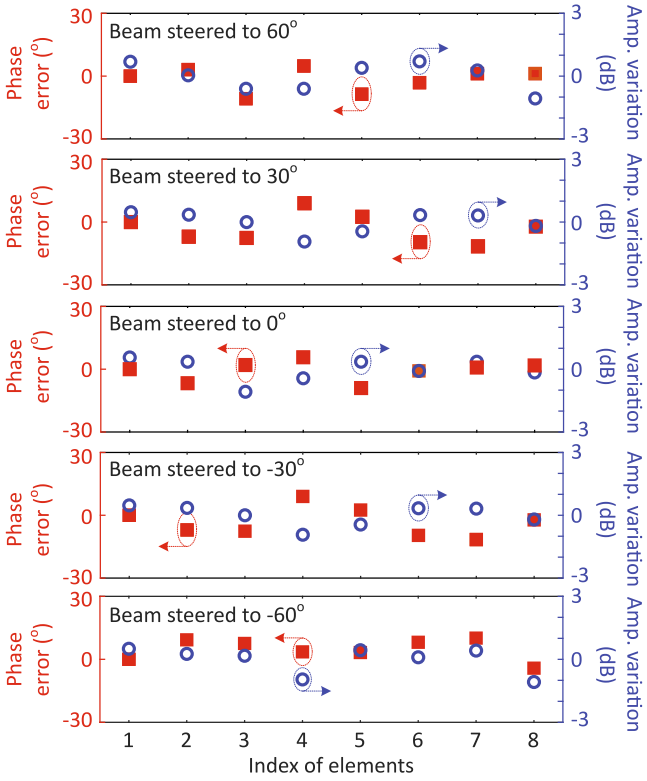
target angle θ, the phase of each oscillator is tuned to satisfy $\Delta\phi_i - \Delta\phi_{i-1} = \pi sin\theta, i = 1, 2, 3, ...$, within the precision provided by the 4-bit bank. The following figures show, for $\theta = -60^o, -30^o, 0^o, 30^o, 60^o$, the amplitude variations and phase errors for the 8 elements achieved in the simulation, and the resulting radiation patterns. These results demonstrate feasibility in the presence of the dominant static variation sources. Transient variation sources (noise, drift), though not considered here, can be addressed as needed via integrated calibration mechanisms as described in Supplementary Fig. 7.



(c)

Beam-steering angle (°)	Half power Beam width (°)	Sidelobe level (dB)
60	29.0	-13.1
30	14.6	-12.3
0	12.6	-11.6
-30	14.7	-11.4
-60	29.1	-13.0

(d)



(e)

(c) Simulated radiation patterns when the beam is steered to -60º, -30º, 0º, 30º, 60º, respectively. (d) Summarized half power beam width and sidelobe level when the beam is steered to different angles. (e) The phase errors and amplitude variations in (c) when the beam is steered to different angles.

Supplementary Fig. 9
Beam quality analysis.

The performance of the demonstrated LAE phased array, i.e., the beam error, is analyzed using Steinberg's tolerance theory[6] in "Principles of Aperture and Array System Design" Chapter 13. How the performance scales with the number of elements is also studied.

Phase quantization error and amplitude variation produce two first-order errors in the radiated beam: (A) main-beam gain error; and (B) beam pointing error.

(A) Main-beam gain error

The main-beam gain error $(G - G_0)/G_0$ is taken from equation 13.8 on p. 306 of Steinberg:

$$\frac{G-G_0}{G_0} = \left|E\left[e^{j\delta\phi}\right]\right|^2 + \frac{1-\left|E\left[e^{j\delta\phi}\right]\right|^2+{\sigma_a}^2/a^2}{N} - 1$$

G_0 is the error-free main-beam gain, G is the gain with phase quantization error and amplitude variation, E stands for the expected value, $\delta\phi$ is the phase quantization error (with rectangular distribution between $[-\frac{\Delta\phi}{2}, \frac{\Delta\phi}{2}]$, where $\Delta\phi$ is the phase-tuning resolution), ${\sigma_a}^2$ is the variance of the amplitude variation, a is the amplitude, and N is the number of elements. The two causes of gain error are (1) the phase quantization error, which arises from finite tuning resolution $\Delta\phi$; and (2) the normalized amplitude variation σ_a/a. In Fig. 9a below, the expected value ($E[(G - G_0)/G_0]$) of the gain error and its standard deviation ($\sigma_{(G-G_0)/G_0}$) are plotted as a function of the two error sources ($\Delta\phi$ and σ_a/a) and the number of elements (N).

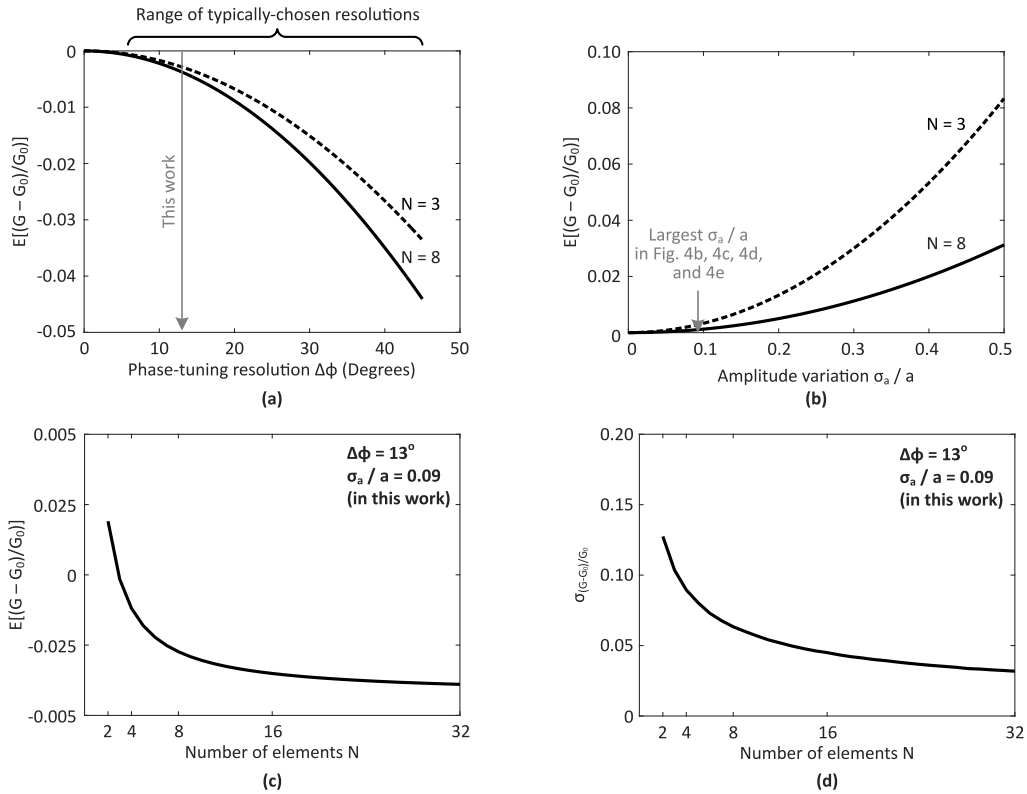


Fig. 9(a): Main-beam gain error $(G - G_0)/G_0$ vs. phase-tuning resolution $\Delta\phi$, amplitude variation σ_a/a, and the number of elements N. (a) Expected value of gain error vs. phase-tuning resolution, for 3 and 8 elements. The grey arrow shows the resolution (13^o) of our phased array. The bracket comprises the phase resolutions of published arrays[7,8,9,10,11,12,13] and commercial products[14,15,16]. **(b)** Expected value of gain error vs. amplitude variation, for 3 and 8 elements. The grey arrow shows the largest standard deviation of amplitude variation (0.09) in our antenna demonstration (manuscript Fig. 5b, 5c, 5d, and 5e). **(c)** Expected value of gain error vs. the number of elements, for the phase-tuning resolution (13^o) and the largest standard deviation of amplitude variation (0.09) of our array. **(d)** Standard deviation of gain error vs. the number of elements, for the phase-tuning resolution (13^o) and the largest standard deviation of amplitude variation (0.09) of our array.

(B) Beam pointing error

The beam pointing error u originates only in the phase quantization error; it is not affected by amplitude variation. The phase quantization error $\delta\phi$ translates to the beam

pointing error through a non-linear relationship that depends on the beam-steering angle θ. Steinberg showed that for a linear phased array the expected value of u is zero, i.e., $E[u] = 0^o$, because the quantization error $\delta\phi$ has a rectangular distribution between $[-\frac{\Delta\phi}{2}, \frac{\Delta\phi}{2}]$, with a mean value of zero; $\Delta\phi$ is the phase-tuning resolution. The standard deviation of the pointing error (i.e., RMS pointing error) σ_u is given by:

$$\sigma_u \approx \frac{\sqrt{3}}{\pi}\frac{\sigma_\phi}{\sqrt{N}} \cdot \Delta u \text{ (equation 13.32 on p. 312 of Steinberg).}$$

σ_ϕ is the standard deviation of the phase error ($\sigma_\phi = \Delta\phi/\sqrt{12}$) and N is the number of elements. Δu is the beamwidth, estimated as $\Delta u \approx \frac{\lambda}{Ndcos\theta}$, where θ is the beam-steering angle and $d = \lambda/2$ is the spacing of antenna elements.

In Fig. 9b below, the RMS beam pointing error σ_u is plotted in function of the beam-steering angle (θ), the phase-tuning resolution ($\Delta\phi$), and the number of elements (N).

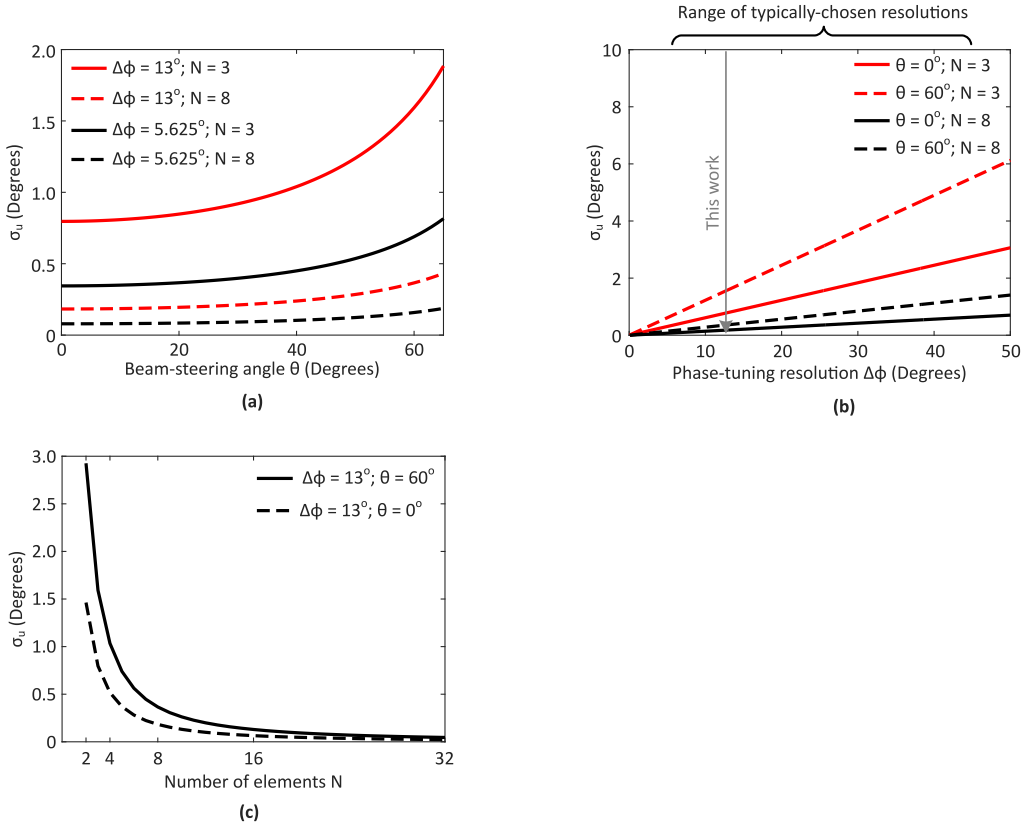


Fig. 9(b): Beam RMS pointing error σ_u vs. beam-steering angle θ, phase-tuning resolution $\Delta\phi$, and the number of elements N. (a) Beam RMS pointing error vs. steering

angle, for two phase-tuning resolutions ($\Delta\phi = 5.625^{\mathrm{o}}$ and 13^{o}) and two numbers of elements ($N = 3$ and 8). **(b)** Beam RMS pointing error vs. phase-tuning resolution, for two beam-steering angles ($\theta = 0^{\mathrm{o}}$ and 60^{o}) and two numbers of elements ($N = 3$ and 8). The grey arrow points to the resolution (13^{o}) of our phased array. The bracket comprises the typical phase resolutions of published arrays[7,8,9,10,11,12,13] and commercial products[14,15,16]. **(c)** Beam RMS pointing error vs. the number of elements, for different beam-steering angles ($\theta = 0^{o}$ and 60^{o}) and the phase-tuning resolution (13^{o}) of our array.

Supplementary Table

	ref[14]	ref[16]	ref[17]	ref[18]	ref[19]	ref[20]	ref[21]	ref[22]	This work
Demonstrated number of elements	16	16	2 and 4	32	16	64 and 256	4	2	3
Technology	discrete chips + antennas on PCB	CMOS chip + LAE antennas	CMOS chip + antennas on PCB	BiCMOS chips + antennas-in-package	BiCMOS chip + antennas-in-package	BiCMOS + sub-reticle stiching	Bi-CMOS	CMOS	LAE
Flexible compatibility	No	Yes	No	No	No	No	No	No	Yes
Monolithic-integrable	No	No	No	No	No	No	Yes	Yes	Yes
Frequency (GHz)	7.5	10	24	28	60	60	77	105.5	1
Loss of EM signal in air at the frequency (dB/km)	<0.01	0.01	0.06	0.06	20	20	0.2	0.2	<0.01
D/λ achievable	-	-	-	-	-	-	7.3	10.0	11.2
Near-field range (D^2/λ) achievable (m)	-	-	-	-	-	-	0.2	0.3	37.9

Table I – Comparison of relevant metrics of the demonstrated system and previous demonstrations in other technologies.

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