V_{TH} subthreshold hysteresis technology and temperature dependence in commercial 4H-SiC MOSFETs

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Abstract

V_{TH} subthreshold hysteresis measured in commercially available 4H-SiC MOSFET is more pronounced in *trench* than in *planar* ones. All *planar* devices from different manufacturers exhibit an inverse temperature dependence, with the hysteresis amplitude reducing as the temperature increases, whereas all *trench* devices from different manufacturers exhibit the opposite behaviour. A physical interpretation is proposed, based on experimental evidence, which demonstrates that temperature dependence of the V_{TH} subthreshold hysteresis is related to the technology. The findings are relevant to the ongoing discussion on SiC bespoke validation standards development and contribute important new insight.

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1. Introduction

Discrete SiC MOSFETs ranging from 600 V to 1700 V have been commercialised for several years and soon 3.3 kV counterparts will be available. Before marketing, manufacturers have tested their devices in order to comply with the existing reliability standards. Nevertheless, some concerns persist since standard tests have been designed for Si technology and may not explore all of the reliability issues that exist in SiC devices. In particular, recent research has gained interest on threshold voltage instability [1-7]. It is important to clarify the different types of instability, their origin and of course their impact on long term reliability.

V_{TH} instabilities can be categorised into two main groups:

- Permanent drift (NBTI, PBTI)
- Recoverable shift (V_{TH} Hysteresis)

This paper focuses in the fully recoverable V_{TH} subthreshold hysteresis. Comparison amongst commercially available *planar* and *trench* 4H-SiC MOSFETs has been carried out in order to discover any influence of the structure and technology of the device on this phenomenon.

2. Theoretical Background

The V_{TH} subthreshold Hysteresis is defined as a recoverable increase of the subthreshold leakage current, caused by a reduction of the threshold voltage when a negative gate bias is applied at the OFF-state. Above the threshold, the hysteresis is considered to be erased and the drain current to be recovered to its characteristic value. In physical terms, it is defined as the difference between the V_{GS}^{UP}, voltage of the up-sweep trace, and V_{GS}^{DOWN}, voltage of the down-sweep trace, both obtained at 100nA (eq. 1).

$$\Delta V_{TH}^{HYST} = V_{GS}^{UP} - V_{GS}^{DOWN} \quad (1)$$

It has been noticed through static characterisation that ΔV_{TH}^{HYST} decreases for higher level of drain current until it is completely erased when the threshold level is reached [7]. Another property of ΔV_{TH}^{HYST} is the dependence on the negative bias V_{GS}^{Start}. Depending

on the V_{GS}^{Start}, three noticeable domains can be defined as follows:

- No hysteresis
- Linear growth
- Saturation

These domains are related to the position of the Fermi Level during device operation, since by modifying its position, not only the concentration of electron and holes is changed at the semiconductor side, but also the quantity of charge (electrons and holes) captured/released from the oxide and interface traps. According to the classical theory of semiconductors [8], the simplified behaviour of a *trench* MOSFET having an oxide containing both donor and acceptor traps is shown in figure 1. The band diagram is represented for four possible states and traps are considered as charged or neutral depending on the Fermi level:

- Depletion (no bias)
- Flat band ($V_G < 0$ V)
- Accumulation ($V_G << 0$ V)
- Inversion ($V_G >> 0$ V)

To satisfy the flat band condition, the Fermi level has to be shifted down by applying a negative voltage equal to V_{FB}, which is given by equation 2.

$$V_{FB} = \phi_{MS} - (Q_F + Q_M + Q_{ID} / C_{OX}) \quad (2)$$

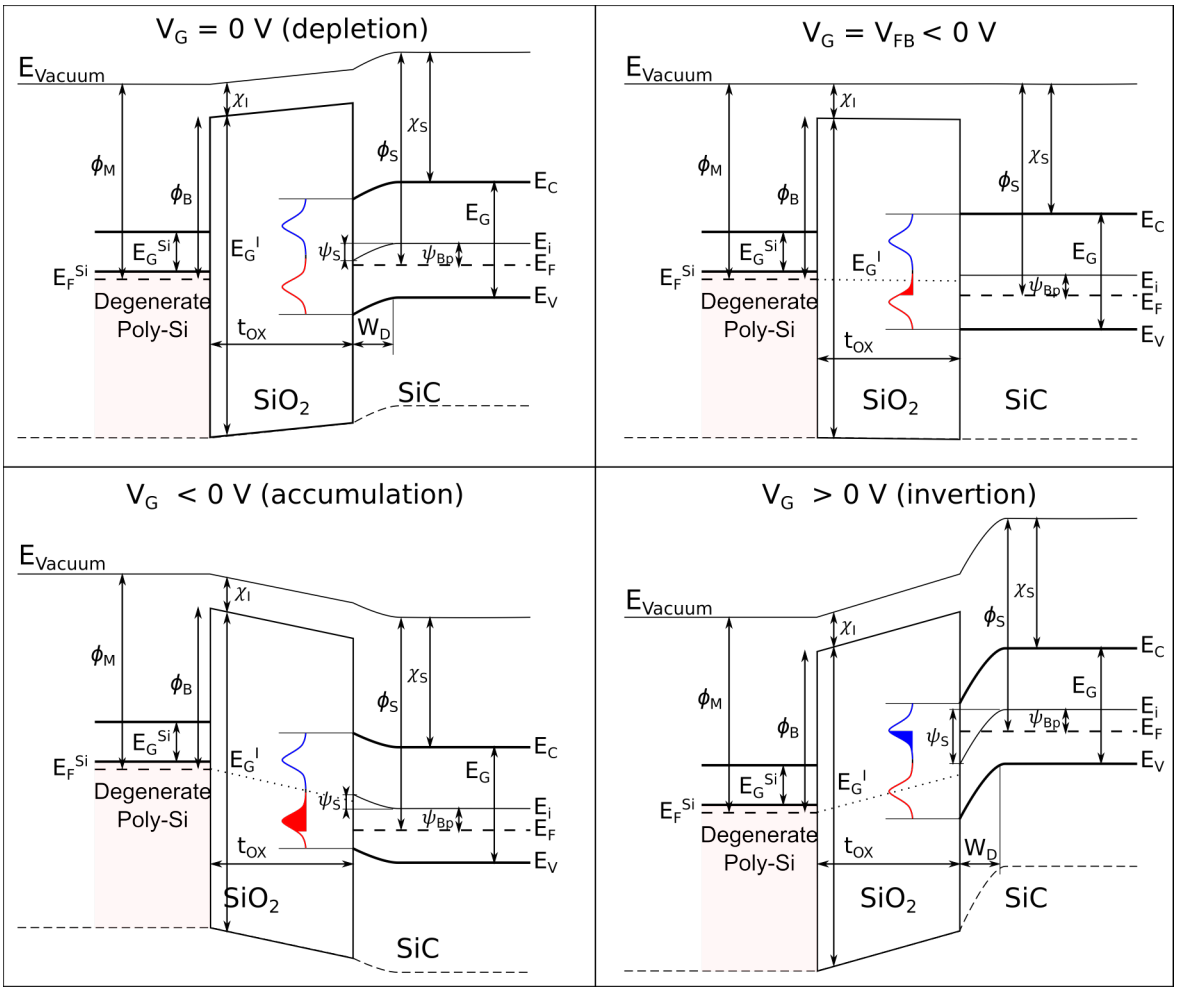

Fig. 1. The representation of the band diagram of *trench* MOSFET taking into account the workfunction difference between degenerate poly-Si gate and SiC and containing Gaussian distributions of both donor (red, lower part of the gap) and acceptor (blue, upper part of the gap) traps in the oxide near the interface. Mobile ions and fixed charge hasn't been taken into account. The same diagram applies to *planar* MOSFET but instead of degenerate poly-Si metal gate is used.

In this equation, ϕ_{MS} is the difference in workfunction between the degenerate poly-Si or metal gate and the semiconductor, Q_F is the fixed charge in the oxide, which has a great impact on the flat band voltage, Q_M is the charge of the mobile ions in the oxide, which are neglected since clean rooms standards allow very low concentration of (sodium, potassium, lithium, etc.) contaminants [7,9], Q_{ID} is the charge trapped at the interface and C_{OX} is the capacitance of the oxide. The interface states are created in different ways:

- the semiconductor discontinuity [10,11]
- semiconductor traps [12]
- oxide traps near the interface [13,14]

By putting the device in the accumulation regime, the donor traps in the oxide are filled at a rate defined by their energy level and capture time constant. When the bias is applied for a long period or at a very energetic level, all of the hole traps at the interface border are filled and the ΔV_{TH}^{HYST} saturation level is reached. In the up-sweep, the device goes from accumulation to depletion and then to inversion. During this process, small increments of gate bias are applied and the trapped holes are slowly released, meaning that the V_{TH} of the device is slightly lower than expected since electrons in the bulk are attracted by the remaining trapped holes. The dependence of V_{TH} on V_{FB} and thus on the related traps is defined in (3),

$$V_{TH} = V_{FB} + 2\psi_B + (\sqrt{(4\varepsilon_S qN_A \psi_B)}/ C_{OX}) \qquad (3)$$

The maximum value of hysteresis that can be experienced in SiC MOSFETs has been calculated [6] with equation (4).

$$\Delta V_{TH}^{HYST} = Q_{ID}/C_{OX} = q D_{IT} \Delta E_{IT} t_{OX}/\varepsilon_r \varepsilon_0 \qquad (4)$$

It can range between 1.07 V and 10.7 V, depending on the Density of interface and oxide traps (D_{IT}) and the distribution of their energy levels (ΔE_{IT}) for a 70 nm thick oxide (t_{OX}). These values are high enough to raise reliability concerns, since undesired switching can happen and as a result power electronics standards are not met.

3. Tested devices and experimental setup

Devices from four different manufacturers were tested. Besides manufacturer 4, which has a proprietary packaging, all the other manufacturers used TO-247 packaging. Table 1 shows the devices measured by manufacturer, rating and structure.

Table 1 - Tested devices

M.	Rating	V_{FB}	V_{TH}	Struc.	Qt.
1	1.2 kV - 19A	- 7 V	3 V	*planar*	4
2	1.2 kV - 20A	- 8 V	3 V	*planar*	4
3	1.2 kV - 17A	- 13 V	4 V	*trench*	4
4*	1.2 kV - 25A	- 14 V	8 V	*trench*	4

* Proprietary packaging

I(V) and C(V) tests have been carried out using a B1505A Power Device Analyser and an E4990A impedance analyser respectively. The temperature of the DUT has been controlled by a conventional hot plate with degree precision. For I(V) measurements, V_{DS} has been kept constant at 1V, while V_{GS} is swept up and down from a starting voltage of V_{GS}^{Start} up to 4V with a 100mV step. V_{GS}^{Start} ranges from – 20V to 0V with a 1V step. All I(V) measurements were carried out after a fast V_{GS} up-sweep preconditioning from 0V to 10V in order to erase the effects coming from previous bias [6]. The schematic view of the I(V) test setup is illustrated in figure 2.

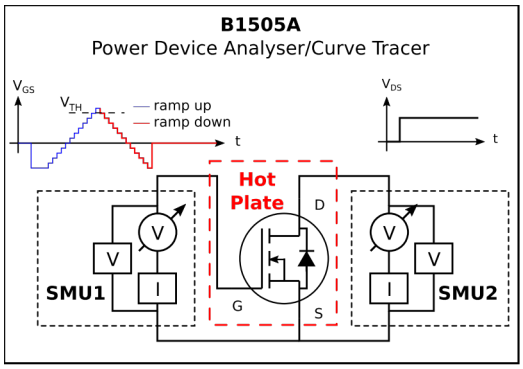

Fig. 2. Temperature dependent V_{TH} Subthresold hysteresis measurement setup.

C(V) tests were carried out in order to determine the flat band voltage V_{FB}, the threshold voltage V_{TH} and the operating (accumulation, depletion or inversion) regime of the MOSFET. The schematic C(V) setup is shown in figure 3. Drain and Source electrodes have been shorted during the measurement and the gate voltage V_G was swept from – 20V to 10V, for devices 1 and 2, from – 30 V to 15 V for device 3 and from – 30 V to 30 V for device 4, with a 100mV step. An AC signal of 25mV – 1MHz was superposed to the DC sweep voltage in order to measure the device capacitance. Measurement have been made for several operating temperatures controlled with a

regulated hot plate.

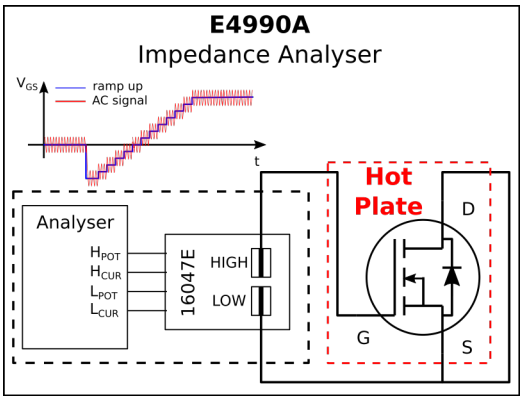

Fig. 3. Temperature dependent C(V) measurement setup for commercial 4H-SiC MOSFETs.

4. Results and discussion

The measurements carried out on MOSFETs form manufacturer 1 are shown in figure 4. The transfer characteristic differs much as V_{GS}^{Start} goes from – 20V to 0V in the up-sweep direction (dashed oval). In the down-sweep direction all the traces almost overlap (small oval), showing that independently of the previous state of the V_{GS}^{Start}, all traces are identical and that its effect has been recovered/erased. This effect has been encountered in literature as well, but details have not been given on the device's structure [6,7].

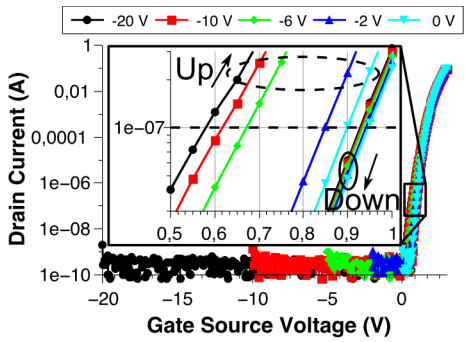

Fig. 4. V_{TH} Subthresold hysteresis effect in a commercial 1200 V 4H-SiC MOSFET transistor from Manufacturer 1.

The value of the ΔV_{TH}^{HYST} subthreshold hysteresis has been extracted on all the devices of the 4 manufacturers. As shown in figure 5, hysteresis is measurable in each of them, but it is more pronounced in *trench* than in *planar*. The manufacturing process are different for each device since they are fabricated by different competing manufacturers. Thus, the difference between values of hysteresis measured on *planar* and *trench* devices can be considered inherent to the technology itself.

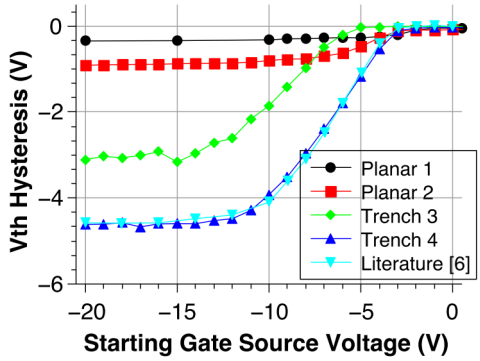

Fig. 5. V_{TH} Subthresold hysteresis of all measured devices at room temperature compared to literature.

Referring to figure 1, when a negative bias is applied on the gate, the donor traps are filled with holes. These traps, are distributed around several energy levels in the gap and have very different relaxation time constants [15]. As a consequence, different device processing may induce different types of oxide traps, which will produce different values of hysteresis. One way to prevent a high amount of holes from being trapped in oxide near the interface is to operate the device in deep depletion mode when in off state, since fewer holes will be available near the oxide traps and the built-in voltage will create a repelling electrical field. This requires a low V_{FB} though gate engineering (poly-Si doping, metal choice, channel doping and oxide fixed charge. This will also provide a low V_{TH}. Adjusting the design parameters (oxide thickness, channel doping, and bulk doping) can bring the V_{TH} voltage to an acceptable value. As shown from the C(V) characteristics in figure 6 and table 1, it is the case of the 4 devices, since their V_{FB} is very low and the V_{TH} is just a few volts above 0 (except for device 4 which shows a particular C(V) characteristic).

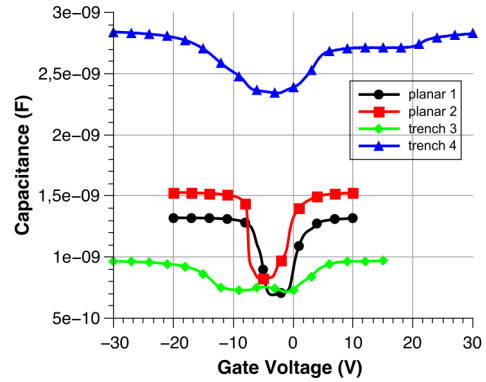

Fig. 6. Capacitance of each device measured at room temperature with a 25 mV – 1MHz oscillation.

In order to pinpoint the position of the Fermi level at the interface, the computation of the surface potential has been carried out from the C(V) characteristics at room temperature and is shown in figure 7.

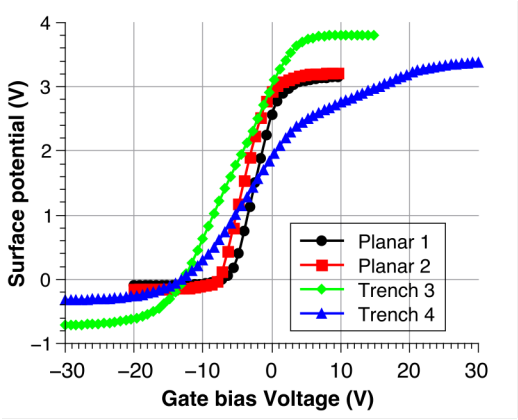

Fig. 7. Surface potential vs. gate bias extracted from C(V) measurements.

Devices 1 and 2 show a very steep variation of the surface potential and the excursion is close to the width of the band gap of the 4H-SiC, which is in conformity with the theoretical predictions. Devices 3 and 4 have a slower capacitance variation, which requires a higher gate bias to fully explore the C(V) characteristics (from accumulation to full inversion). The measurement is thus flawed because of higher gate leakage currents mostly due to hole trapping since this phenomenon occurs only when a negative bias is applied. Figure 8 shows the measured leakage current for the 4 measured devices. For positive bias, the leakage current is below the detection range of the equipment and considered very low, whereas, for negative bias, the leakage current is one magnitude higher in trench devices in the low electric field domain (dashed square). In the high electric field domain, all the devices exhibit Fowler-Nordheim tunnelling leakage current, which is often considered to be completed by trap assisted tunnelling [16]. The electrical field in the oxide can be estimated between 3 and 6 MVcm^{-1} for a 50 nm thick oxide.

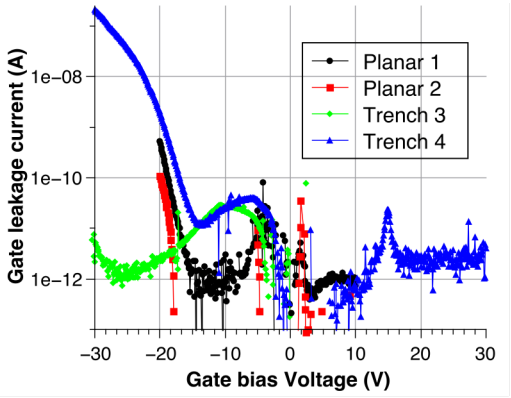

Fig. 8. Gate leakage current of the 4 measured devices.

A comparison of *planar* and *trench* technologies ΔV_{TH}^{SUB} subthreshold hysteresis for different temperatures is shown in figure 9. There is an interesting dependence on temperature and structure at the same time. *Planar* devices from both manufacturers exhibit a negative dependence of the hysteresis (for higher temperature hysteresis is reduced), whereas *trench* devices from both remaining manufacturers exhibit the opposite behaviour. These results are to be taken into account when operating trench devices, since depending on the V_{GS}^{Start} and temperature, the V_{TH}^{UP} can be only be a few tens of millivolts above 0 V and can considerably enhance leakage currents in the subthreshold regime. The origin of this behaviour is related to the different capture/emission time constants of the hole traps in the oxide [15]. Both these processes are accelerated when temperature is increased thus no change should be expected, but instead opposite behaviour is present for the two technologies. Since both *planar* devices undergo hysteresis saturation around - 7 V of V_{GS}^{Start}, the high temperature reduces the measured hysteresis because the V_{TH} of the device is lowered. The trapped charge in saturation is almost not affected by temperature, which means that the up-sweep trace stays the same

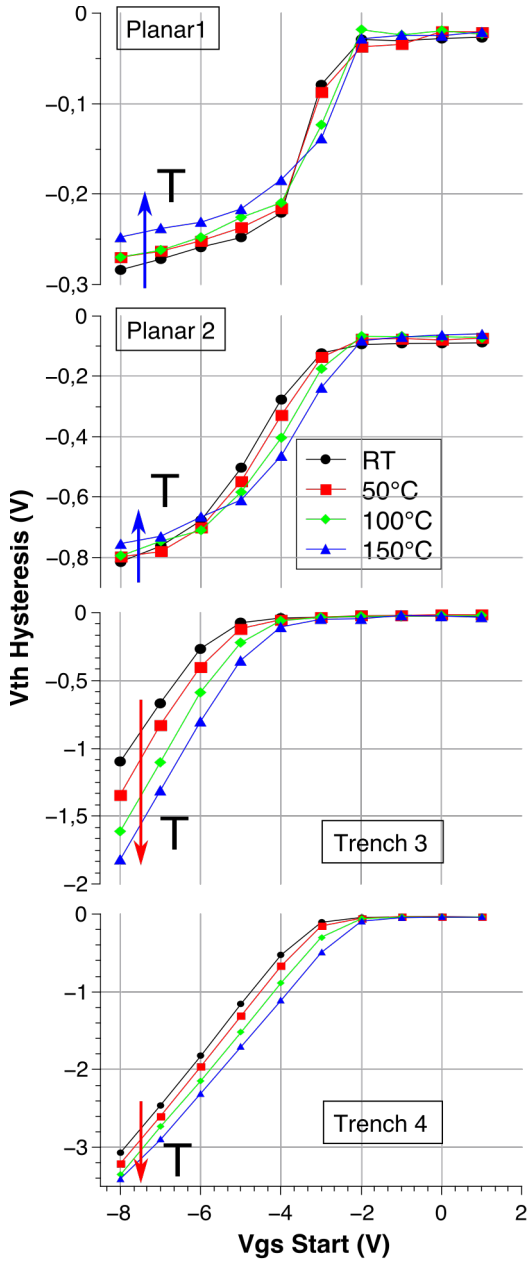

Fig. 9. V_{TH} Subthresold hysteresis of all measured devices.

in saturation domain whereas the down-sweep is shifted due to the V_{TH} lowering. In the case of *trench* devices, hysteresis saturation occurs for lower negative voltage V_{GS}^{Start}. Increasing the temperature causes an acceleration of the capture of holes, which leads to a bigger trapped charge for V_{GS}^{Start} = - 8 V. The up-sweep trace is strongly affected, whereas the down-sweep is only affected by the V_{TH} lowering. Since the emission time constants are generally longer compared to the capture time constants [15], the measured hysteresis is enhanced. This behaviour has been normalised in figure 9 in order to show which device is more affected by temperature. Devices 1 and 2 behave very similarly, since at these conditions they operate in hysteresis saturation domain. They exhibit a very small decrease of the hysteresis. Devices 3 and 4 exhibit an increase of the hysteresis, but are very different. Device 3 hysteresis saturates for V_{GS}^{Start} = - 15 V at - 3 V minimum value. As a consequence, the temperature highly enhances the quantity of charge trapped in the oxide during the test at V_{GS}^{Start} = - 8 V for different temperatures. Device 4 instead shows a higher hysteresis and its saturation appears for V_{GS}^{Start} = - 11 V, which means that the left charge to be trapped is much smaller for V_{GS}^{Start} = - 8 V, leading to a smaller increase of the hysteresis with the effect of temperature.

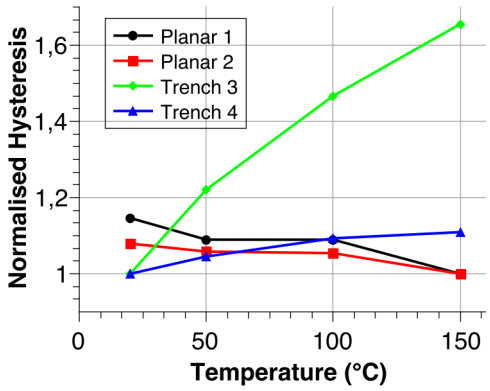

Fig. 9. Normalised V_{TH} Subthresold hysteresis of all measured devices. Exctractions are carried out for I_D 100 nA and V_{GS}^{Start} of - 8 V.

This finding shows that *planar* devices must have lower density of traps(D_{IT}) and the distribution of their energy levels near the valence band.

From figure 4, 7, 8 and 9, it can be stated that *trench* devices are affected by a higher density of oxide traps near the interface and that the distribution of their energy levels is closer to the midgap, thus more prone to hysteresis. Their energy level can be assumed closer to the midgap since the hysteresis saturation is observed for V_{GS}^{Start} higher than the V_{FB}. A schematic view of oxide border hole traps distributions in *planar* and *trench* MOSFET is shown in figure 10.

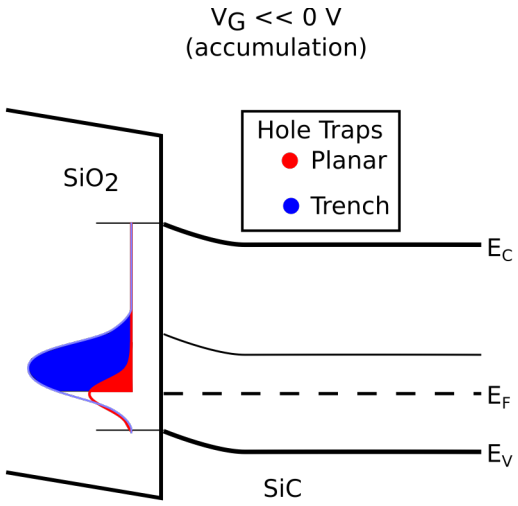

Fig. 10. Schematic illustration of the distributions of oxide border hole traps in commercially available *planar* and *trench* MOSFETs that are responsible for the V_{TH} subthreshold hysteresis.

4. Conclusions

It has been reported that V_{TH} subthreshold hysteresis is fully reversible and doesn't affect the device reliability [6], but there are not any studies that evaluate its evolution when devices are stressed in real application conditions. This paper shows that there is enough difference between commercial *planar* and *trench* MOSFETs to raise concerns when it comes to V_{TH} subthreshold hysteresis. Further tests are needed in order to learn more on the evolution of this phenomenon in long term. A specific standard could be issued for the evaluation of this phenomenon in commercial devices.

It has been shown in this paper that *trench* technology is more affected by the V_{TH} subthreshold hysteresis and that the phenomenon is enhanced with increasing temperature due to higher density of traps, shallower and broader distributions energy level (around midgap) compared to *planar* counterparts.

Dynamic characterisation of this phenomenon has been reported [17] and shows presence of hysteresis beyond the threshold voltage. No double pulse measurements with different negative OFF-state V_{GS} has yet been reported. These measurements might shed some light on the enhancement of power losses due to higher leakage current caused by the V_{TH} subthreshold hysteresis.

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