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Limitations of Switch Level Analysis for Bridging Faults

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Abstract—**Switch level models are widely used for fault analysis of MOS digital circuits. Switch level analysis (SLA) provides significantly more accurate results compared to the gate level models and also avoids the complexities of circuit level analysis. The accuracy of SLA is critically examined, and conditions under which switch level analysis may generate incorrect results are specified. Such conditions may occur when the bulk of a transistor is connected to its source. These conditions are especially applicable under certain types of bridging faults. A simple technique is suggested for accurate switch level modeling under such conditions.**

I. Introduction

In the past, test generation and simulation were conducted exclusively at the gate level. Recently, however, it has been pointed out that the classical stuck-at-fault model does not represent some important failure modes, especially in the case of MOS devices. In a complex gate, the physical nodes do not directly correspond to nodes in an equivalent gate level network [1], [2]. Hence, many physical opens and shorts cannot be satisfactorily represented at the gate level. Gate level fault models, even for simple gates, can become quite complex [2]-[4]. Consideration of failure modes at the switch level or circuit level are alternatives to gate level modeling. Circuit level simulators, such as SPICE, can be used for the study of failure modes but due to the high CPU time requirement, they become impractical even for moderate sized devices. As a consequence, switch level modeling is gaining wide acceptance for fault modeling and test pattern generation of MOS circuits [2]-[7]. The following assumptions are generally used for a simple switch level analysis (SLA).

1) A transistor is an ideal switch. For an n-channel transistor an *H* (definitely recognized high voltage level) at the gate causes it to represent low resistance and an *L* (definitely recognized low voltage level) causes it to represent very high resistance. When the input is not *H* or *L* (i.e., indeterminate), the transistor presents an indeterminate resistance.
2) The resistance of the depletion load transistor in an nMOS gate is much larger than the ON resistance of an enhancement mode transistor, but much less than the OFF resistance of an enhancement mode transistor.
3) A node, when connected to both V_{dd} and ground only through high resistance paths, will retain the previous voltage level (at least for a limited time). A node connected to both V_{dd} and ground through low resistance paths will have an indeterminate voltage level.

It is sometimes possible to resolve an indeterminate situation by assuming a specific resistance ratio for enhancement and depletion type transistors. However, this makes the model more complex. Also, the resistance depends not only on the transistor dimensions, but also on the position of transistor in a network.

In this paper the problem of modeling faults in a two terminal network of n-channel or p-channel transistors is considered. The results obtained are applicable to the *n*-network in nMOS as well as the *p*-network and the *n*-network in CMOS. The results can be used in both voltage testing and current testing [8] environments. We present conditions under which SLA may generate wrong results. In the presence of a bridging fault, unexpected structures may be formed, giving rise to such situations. Techniques for accurate analysis using switch level models are suggested. For simplicity, it is assumed that all the inputs and outputs are accessible and only a single bridging fault exists.

Some terms used in this paper are defined below and illustrated in Fig. 1.

Conductance State of an n-Network (p-Network): An *n*-network (*p*-network) is *on* when it presents very low resistance between the output and the ground (V_{dd}) nodes. It is in the *off* state when it presents a very high resistance between the two nodes.

Internal Node of a Gate: A node in a gate which is neither a transistor input (gate connection) nor the power supply is an internal node. In Fig. 1, internal nodes are marked with lower case letters (*a* to *l*).

Column: A column consists of a set of serially connected MOSFET's. In a column there are no transistors (or sets of transistors) in parallel. In Fig. 1, nine columns are shown, marked 1 to 9.

Parallel Connected Columns (PCC): A structure with more than one column in parallel. Fig. 1 has four PCC's, marked I to IV.

Internal Node of a PCC: Any node in a PCC which is not common to another PCC is defined as an internal node of the PCC. In Fig. 1, nodes *a*, *b*, and *d* are internal nodes of PCC I, *f* is an internal node of PCC II, *g* and *h* are internal nodes of PCC III, and *i*, *j*, and *k* are internal nodes of PCC IV.

Conduction Path: Any path which connects the ground and the output node will be called a conduction path. Fig. 1 has the following conduction paths—*ABCFGH*, *ABCFI*, *DEFI*, *DEFGH*, *JKNOP*, *JKQ*, *LMNOP*, and *LMQ*.

Logical Node: A logical node is a logical input or an output node of a gate. In general all logical nodes are outputs of gates or complex gates.

Deterministically Testable Fault: A fault is deterministically testable if there is at least one vector which will definitely (under the switch level modeling assumptions) cause the logical output to be the complement of the output of fault free circuit.

Equivalence of Switch Level and Circuit Level Analyses: In a MOS network, if SLA generates the same conductance state as that provided by the circuit level analysis, or if the result of the SLA is indeterminate, the results are said to be equivalent. When SLA predicts an indeterminate result, the circuit level analysis often produces a definite result. In this case, SLA cannot be faulted because it does not use specific information about the parameter values. In fact circuit level analysis could sometimes be misleading because

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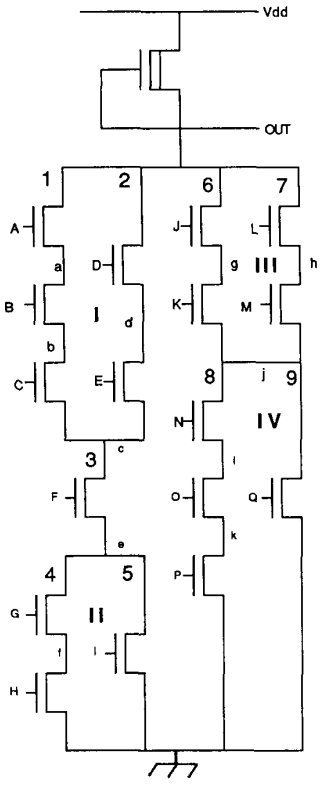

Fig. 1. Illustration of definitions.

the results are sensitive to the parameters. If SLA predicts a definite conductance state, but circuit level analysis does not, then the two analyses are not considered equivalent. In this case the results obtained via SLA may be misleading.

II. Effect of Substrate Connection

In the majority of digital IC's made on silicon, the substrate of a nMOS transistor is connected to the ground or the maximum negative voltage on the chip. Similarly the substrate of a pMOS transistor is connected to V_{dd} or the maximum positive voltage. This ensures that the substrate—drain and the substrate—source junctions never become forward biased. Thus the substrate (or well) becomes completely isolated and the possibility of a current through the substrate is eliminated. In this case, the drain and the source regions are interchangeable (except in cases like lightly doped drain (LDD) type structures). Hence, the device acts as a simple switch controlled by the gate voltage.

In some IC designs the substrate (well) of a transistor is connected to its source node (rather than the maximum positive or negative voltages). This is generally true in silicon on insulator (SOI) technology [9]-[11] in which a floating substrate lowers the effective threshold voltage and thus causes a "kink" in the transfer characteristics [10]-[12]. The main reasons for this kink include impact ionization, weak avalanche, and charge pumping in the substrate. To avoid the effects of this "kink," the transistor substrate is electrically connected to its source node [9]-[11]. Since under normal operation of a device, the source voltage of an nMOS (pMOS) transistor is lower (higher) than the drain voltage, there is no possibility of the substrate-drain junction becoming forward biased. In general the source-substrate connection results in lower body-effect, equal potential distribution, and may even result in less area. However, when the substrate of a transistor is connected to its source, its behavior cannot always be characterized as a simple switch. Consider the following cases.

i) When drain voltage V_d of an nMOS transistor is greater than its source voltage V_s, and the gate voltage is high, the transistor conducts and provides a low impedance path between its drain and the source. When gate voltage is low, the transistor offers a high impedance between its source and drain. The switch level model is valid for this case.

ii) When $V_d < V_s$ (which can occur only in presence of a fault), the substrate-drain junction becomes forward biased. This provides a low resistance source to drain path through the substrate and the current through the transistor is no longer controlled by the gate voltage. Therefore, the MOSFET cannot be modeled as a switch controlled by the gate. In this case, the current through the device can cause significant power dissipation, which could even result in permanent failure of the device. Such conduction of a MOS transistor will be referred to as *anomalous reverse conduction* (ARC). This situation never occurs under normal operation of the device. However, as shown later, this situation could arise in the presence of bridging faults.

Bridging faults in nMOS and CMOS complex gates were examined under both the substrate connection schemes: (i) when the substrate is connected to the maximum negative or positive potential and (ii) when the substrate is connected to the source. It is assumed that all the inputs are independently accessible. Only irredundant gates are considered in this paper. In the case where the bulk of an nMOS or pMOS transistor is connected to the most negative (positive) voltage, the results from SLA are in complete agreement with the circuit level analysis. Hence, the results for this case are not discussed.

Consider the structure of Fig. 2, assuming that the substrate of each transistor is connected to its source. Each bridging fault was examined under all possible test vectors at switch level as well as at circuit level (using SPICE). The results are shown in Table I. Some faults provide only redundant information, hence, they are not included in the table. When the value predicted by SPICE is outside of the noise margins, it is termed probably H or probably L, depending on whether it is higher or lower than the switching threshold. It can be seen that all the faults are deterministically testable. For most of the faults, results obtained using switch level analysis are found to be in agreement with those from the circuit level analysis. However, there are some cases in which the results of switch level analysis do not match with those from the circuit level analysis. In these cases a more detailed analysis at a lower level is essential. This is best illustrated by an example.

Example 1: Consider the nMOS complex gate of Fig. 2 in the presence of fault no. 10 (a short between nodes 5 and 8) with the test vector $\overline{ABCD} = 0011$. The complex gate implements the function $\overline{AB + CD}$. A simple switch level analysis suggests that the transistors NA and NB are OFF, and transistors NC and ND are ON. One end of the short, node 5, is between two OFF transistors. According to the assumptions of the switch level analysis, the presence of the short should be of no consequence. The output, being connected to the ground through NC and ND both of which are ON, should be at logic 0.

However, SPICE analysis gives an output voltage of 2 V, which is neither logic "0" nor logic "1" (see Fig. 3). The analysis also gives a current of about 20 μA flowing from node 5 to node 2. In this case node 5 effectively becomes the drain of NA. However, according to the switch level model, there should be no current through NA except for a small leakage current.

The circuit level analysis suggests that the resistance of the OFF transistor NA is not as close to the ideal (infinite) as the switch level analysis assumes. The significantly low OFF resistance and thus the abnormally large leakage current through transistor NA, can be explained by the ARC phenomenon. □

Example 1 is restricted to one PCC. In this case SLA may give misleading results for some input vectors. However, the faults are

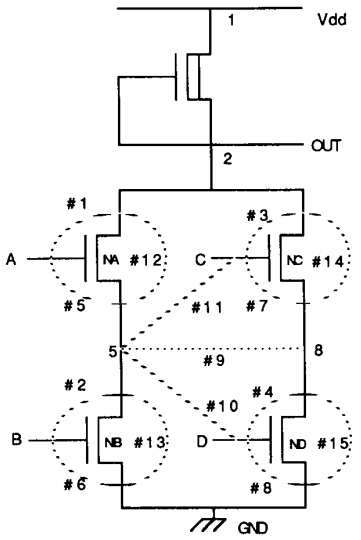

Fig. 2. nMOS complex gate for Example 1.

TABLE I
ANALYSIS OF nMOS COMPLEX GATE OF FIG. 2 FOR DIFFERENT BRIDGING FAULTS.

INPUTS				OUTPUT									
A	B	C	D	NORMAL	#1	#2	#5	#6	#9	#10	#11	#12	#13
0	0	0	0	1	0,0	1,1	1,1	1,1	1,1	1,1	1,1	1,1	1,1
1	0	0	0	1	1,1	0,0	1,1	1,1	1,1	0,0	1,1	1,1	0,0
0	0	0	1	1	0,0	1,1	1,1	1,1	1,1	1,1	1,1	1,1	1,1
1	0	0	1	1	1,1	0,0	1,1	1,1	1,1	0,0	1,1	1,1	0,0
0	1	0	0	1	0,0	1,1	1,1	1,1	1,1	1,1	1,1	0,0	1,1
1	1	0	0	0	1,1*	1,1*	1,1	1,1	0,0	0,0	0,0	0,0	0,0
0	1	0	1	1	0,0	1,1	1,1	1,1	0,0	1,1	1,1	0,0	1,1
1	1	0	1	0	1,1*	1,1*	1,1	1,1	0,0	0,0	0,0	0,0	0,0
0	0	1	0	1	0,0	1,1	1,1	1,1	1,1	1,1	1,1	1,1	1,1
1	0	1	0	1	1,1	0,0	1,1	1,1	0,0	1,1	0,0	1,1	0,0
0	0	1	1	0	0,0	0,0	0,0	0,0	0,0	0,1*	0,1*	0,0	0,0
1	0	1	1	0	0,0*	0,0	0,0	0,0	0,0	0,0*	1,1*	0,0	0,0
0	1	1	0	1	0,0	1,1	1,1	1,1	1,1	1,1	1,1	0,0	1,1
1	1	1	0	0	1,1*	1,1*	1,1	1,1	0,0	0,0	0,0	0,0	0,0
0	1	1	1	0	0,0	0,0	0,0	0,0	0,0	1,1	1,1	0,0	0,0
1	1	1	1	0	0,0	0,0	0,0	0,0	0,0	0,0	0,0	0,0	0,0

1* : Probable H (2.7-2.2 volts)
0* : Probable L (2.2-1.25 volts)
x,y : Results of switch level and circuit level analysis respectively.

testable. When a bridging fault occurs between two nodes of two different PCC's, the analysis becomes more complicated. In such a case, it is possible that the fault may become untestable at switch level as illustrated in Example II.

Example 2: Consider the *n*-network of the complex gate shown in Fig. 4, which implements the function $\overline{(CD + E)(AB + F)}$. The gate may be an nMOS gate with a depletion mode load transistor or a CMOS gate with a *p*-network as the pull-up part. A possible layout of the gate is shown in Fig. 5. Consider a bridging fault between nodes 1 and 3. Such a fault is quite possible in the given layout because the two nodes are close to each other. Consider the test vector *ABCDEF* = 100010. According to the switch level analysis, the transistors *ND*, *NC*, *NB*, and *NF* are OFF, and the transistors *NA* and *NE* are ON. The *n*-network is thus off. The output should be logic "1." Also in case of CMOS, the supply current should consist only of the leakage current which is typically very small.

A CMOS version of the above gate was simulated using SPICE. Under the applied vector, the output voltage was found to be 3.08

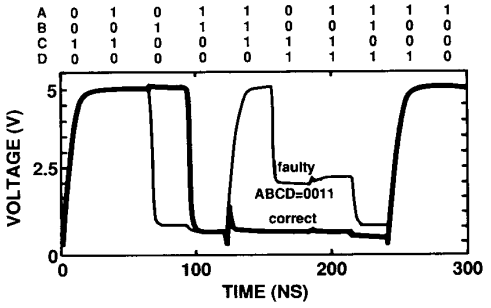

Fig. 3. SPICE output for fault no. 10, in nMOS complex gate of Fig. 2.

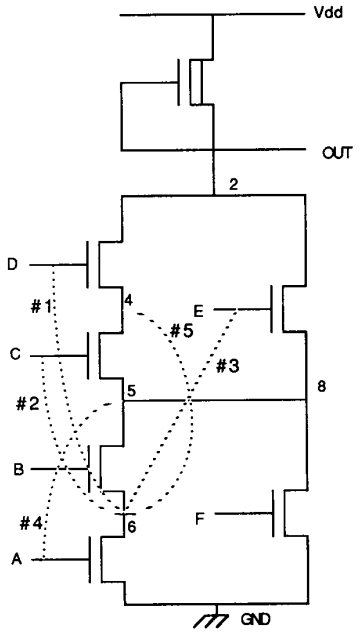

Fig. 4. nMOS complex gate for Example 2.

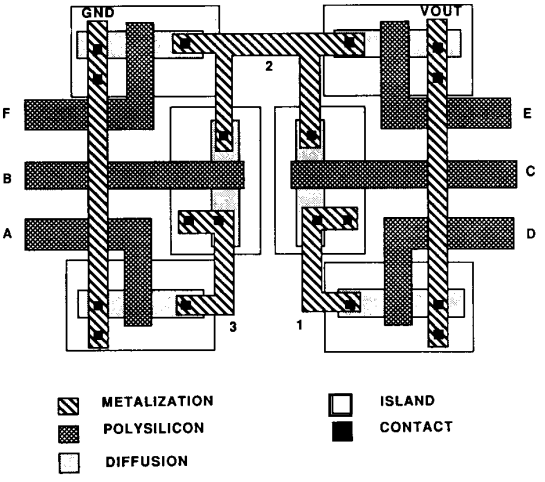

Fig. 5. A possible layout of the *n*-network of Example 2.

V. As it is outside of the noise margin, it may or may not be recognized as logic "1." The fault has a more dramatic effect on the supply current. It changes from a normal value of 26 pA–116 μA. This indicates that in the presence of this fault, both n and p parts are on. Practically all the current flows through the transistor *NC*. This contradiction between the switch level analysis and the circuit level analysis again suggests that the switch level analysis cannot adequately represent the circuit behavior. As node 1 is connected to ground through a low resistance path, and node 2 is connected to V_{dd} through a low resistance path, voltage at node 2 is higher than that at node 1. There will be a current flow from node 2 to 1 through *NC*, as a consequence of ARC phenomenon.

An nMOS version of the gate was also simulated under the same conditions. It also shows that in presence of the bridging fault the n-network is on. This causes the output voltage to drop to about 0.93 V, which is recognized as logic "0" by the subsequent stages. The analysis also gives a current of 22 nA through the transistor *NC* which contradicts the results of switch level analysis. These situations can be resolved by taking into account the ARC phenomenon. □

Both the above examples show that if the source voltage of an nMOS (pMOS) transistor becomes higher (lower) than its drain voltage, the behavior of that transistor cannot be modeled at the switch level because of the ARC phenomenon. It can be easily seen that ARC can occur in an nMOS gate only when the n-network is off. ARC can occur in the n-network (p-network) of a CMOS gate only under the vectors for which it is normally off, and the complimentary network is on. The above observations lead us to the following assertions which are applicable when the substrate and the source of a transistor are connected.

Assertion 1: In an n-network or a p-network, for any short between two internal nodes of a PCC, its behavior can be correctly modeled at the switch level.

Proof: Consider an n-network. For ARC to occur, the drain voltage of an nMOS transistor must be lower than the source voltage. In this case, the drain of a transistor must be connected to ground and the source to V_{out} which should be approximately equal to V_{dd}. For the drain to be connected to ground, there must be a low resistance path from the drain to the upper common node of the PCC, which should be connected to the ground through at least one of the parallel columns of the PCC. However, if the upper common node of the PCC is connected to ground, there cannot be any internal node in the PCC with a voltage higher than the ground. There is, therefore, no way the source of the transistor can be connected to V_{out} because of an internal short. The proof for a p-network is similar. Q.E.D.

Assertion 2: In an n-network or a p-network, if a short occurs between two internal nodes of a PCC, then there exists at least one vector for which the conductance state is different from that of the fault free network.

Proof: If both nodes belong to one conduction path, all the transistors between the faulty nodes will appear as s-ON and their inputs become don't care terms. If the short occurs between two internal nodes of two different conduction paths, then the network will perform one product of sum operation in place of sum of product. Hence, the conductance state will be different for at least one vector. Q.E.D.

Assertion 3: In an n-network or a p-network, if a short between two columns involves one nonlogical node within a column and one logical node (except ground), then there is at least one vector under which the SLA is not applicable.

Proof: Consider an n-network. Two situations are possible—(i) when both the columns belong to the same PCC and (ii) when the columns belong to different PCC's. The two cases are considered separately.

(i) When both the columns belong to the same PCC, consider the case when one end of the fault is 1, i.e., the power supply or an input which can be set to 1. The transistor(s) will show ARC under the following conditions: (a) all conduction paths are OFF except for those passing through the affected PCC, (b) all transistors of all healthy columns of the affected PCC are OFF, and (c) all transistors in the column with the faulty logic input are ON and all transistors in the column of the nonlogic faulty node have gate voltages equal to "0."

(ii) When columns belong to different PCC's, the transistor(s) will show ARC when the following conditions are met: (a) all conduction paths are OFF except for those passing through the affected PCC's, (b) all transistors of all healthy columns in the PCC of faulty logic input are OFF, while all transistors in the column of faulty logic input are ON, and (c) all transistors of the column of faulty nonlogical node are OFF, while all transistors in all healthy columns in the same PCC are ON.

In both the cases some transistor(s) will show ARC as their source voltages become higher than the drain voltages. Hence, from Assertion 1, a switch level model cannot predict the behavior of these transistor(s). Similar argument applies to the p-network. Q.E.D.

Assertion 4: In an n-network or p-network, for any short between two internal nodes of different PCC's, there exists at least one vector under which some transistor(s) show ARC, and hence, the switch level analysis is not applicable.

Proof: To prove this assertion for an n-network, we will consider all the possible situations separately.

1) When both PCC's belong to one conduction path—let PCC1 and PCC2 be the PCC's involved in the fault, PCC1 being closer to the output node and PCC2 to the ground, respectively. Some transistor(s) will show ARC when the following conditions are met:

a) all conduction paths are OFF except for one conduction path which has the affected PCC's,
b) in PCC1, all transistors in the faulty column have a "0" at their gates, while other columns are ON,
c) in PCC2 the transistors between faulty node and ground are switched ON, while all other transistors are switched OFF.

2) When the two PCC's belong to different conduction paths, some transistor(s) will show ARC when the following conditions are met:

a) all conduction paths are OFF except the paths which have affected PCC's,
b) all transistors in the faulty column of one PCC have "0" at their gates, while all other columns are ON,
c) all transistors in the other PCC have "0" at their gates except the transistors between faulty node and output node.

In both the situations, the source voltage of some transistor(s) become higher than the drain voltage. Hence, they will show ARC. Therefore, switch level modeling is not able to predict the behavior of these transistor(s). The proof for a p-network is similar. Q.E.D.

The assertions stated above identify the conditions under which switch level analysis fails to predict the behavior of an n-network or a p-network. A simple addition to the switch level model to account the ARC may be made by introducing a diode across the switch [13], [14]. The diode represents the behavior of the substrate–drain junction. Under normal operation, when the drain voltage is higher than the source voltage, the diode is reverse biased and the current through the switch is controlled by the gate voltage only. In case of a fault, if the source voltage becomes higher than the drain voltage, the diode becomes forward biased and shows the effect of ARC. This modification should be introduced in the switch level algorithms used for the simulation. Existing switch level simulation algorithms may not support the representation of diodes without appropriate modifications.

The implementation of the results presented here will require careful examination. It should be recognized that for CMOS, both the n-part and the p-part may remain ON/OFF in presence of some faults. This aspect of fault modeling in CMOS is discussed in detail in [14].

III. Conclusions

Accuracy of switch level modeling for VLSI testing has been examined. SLA generally predicts the correct logic output, although it does not predict any degradation in noise margins. In some cases, it will predict a definite value even though the actual voltage stays outside the noise margin.

When the substrate is connected to the source, there are some cases in which results from the SLA do not match with those from the circuit level analysis. For faults like gate to source, gate to drain, and drain to source shorts, the switch level model is adequate for obtaining the necessary test vectors. For shorts between a logical input and a nonlogical node of another column, the switch level model does not correctly predict the behavior under all vectors. In these cases an analysis at a level below the switch level is essential. Also, when a short occurs between two nodes of two different PCC's, the switch level model may not be accurate enough to generate the necessary test vectors. Under some specific conditions, the ARC phenomenon must be taken into account.

SLA can be used very effectively to characterize faults. However, in some specific cases, the circuit level behavior must be taken into account for accuracy.

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Improved Deterministic Test Pattern Generation with Applications to Redundancy Identification

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Abstract—**Based upon the sophisticated strategies used in the automatic test pattern generation system SOCRATES, this paper presents several new concepts and techniques aiming at a further improvement and acceleration of the deterministic test pattern generation and redundancy identification process. In particular, we will describe an improved implication procedure and an improved unique sensitization procedure. While the improved implication procedure takes advantage of the dynamic application of a learning procedure, the improved unique sensitization procedure profits from a dynamic and careful consideration of the existing situation of value assignments in the circuit. As a result of the application of the proposed techniques, SOCRATES is capable of both successfully generating a test pattern for all testable faults in a set of combinational benchmark circuits, and of identifying all redundant faults with less than 10 backtrackings.**

I. Introduction

Recent advances in VLSI technology and the increasing economic impact of testing operations on the overall chip costs have led to the meanwhile widespread use of the various scan-design techniques [1]. Since those techniques offer the important advantage of reducing the problem of testing complex sequential circuits to that of testing combinational circuits, efficient methods for fault simulation and automatic test pattern generation (ATG) in combinational circuits have gained great practical significance. Motivated by this fact, a considerable number of ATG approaches for combinational circuits, as e.g., [2]–[8], has been proposed.

Moreover, in view of the increasing quality requirements, it has frequently become a necessity to identify all redundant faults in a given circuit, in order to guarantee the completeness of the generated test set with respect to all testable faults. As is well known, redundancy identification (RI) can be performed by both methods specifically developed for this purpose, as e.g., [9], as well as deterministic ATG algorithms, which are complete in the sense that, given enough time, they will generate a test pattern for all testable, i.e., non-redundant, faults.

Among the ATG approaches cited above, the most significant progress has been achieved by the ATG system SOCRATES [7], [8], which has been presented very recently. SOCRATES' efficiency, even in a workstation environment, results from the application of a very fast fault simulation algorithm [10] and a sophisticated deterministic ATG algorithm. The latter one benefits from several distinct techniques which optimize the pruning of the search space [11], that has to be investigated during the deterministic ATG process. As a consequence, conflicting value assignments are recognized much earlier and the number of occurring backtrackings is drastically reduced. In particular, the deterministic ATG algorithm of SOCRATES incorporates an improved implication procedure, an improved unique sensitization procedure, and an improved multiple backtrack procedure, which all have been developed by extending the concepts of the FAN algorithm [4].

A specific feature of the deterministic ATG algorithm implemented in SOCRATES consists in its capability of identifying most

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