Silicon RF-Photonics Processor Reconfigurable Core

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Abstract *We demonstrate a programmable core for a microwave photonic processor integrated in silicon on insulator. Based on a hexagonal mesh of tunable couplers, it enables reconfigurability of circuit topology and design parameters for signal filtering and dispersive time delaying applications.*

Introduction

General-purpose integrated programmable photonic processors[1] are called to play a key role in the implementation of massive-scale application scenarios, such as next-generation wireless communications front ends and the Internet of Things. Their significance lies in the capability of implementing several signal processing functionalities by suitable programming of one common photonic hardware architecture. The central element of the proposed reconfigurable photonic processors[2-4] is a reconfigurable optical core system, where the main signal processing architectures can be set up in response to specific electronic control signals. For instance, it should be able to implement radiofrequency (RF)-photonic filters and dispersive delay lines by employing a scheme based on single-sideband modulation (SSM) and carrier injection, where the optical filter response is translated into the RF domain.

A pioneering configuration[2] of the processor optical core was built upon a cascade of beamsplitters or Mach Zehnder Interferometers (MZIs) with the incorporation of phase tuning elements that enable independent control of the amplitude and phase of the light. This approach allows, actually, the synthesis of both feed-forward and -backward architectures, with the demonstration of feed-backward configurations for microwave photonics (MWP) filtering based on a square-waveguide-mesh topology. Nevertheless, the Free Spectral Range (FSR) was limited to around 12.6 GHz for several combinations of two optical ring resonators (ORRs). More recently, a hexagonal-mesh-based architecture was proposed for the configuration of feed-forward and -backward photonic integrated circuits (PICs), featuring improved performance in terms of spatial tuning reconfiguration step, reconfiguration performance, switching elements per unit area and losses per spatial resolution[3]. This mesh profits from several synthesis algorithms reported for arbitrary frequency response circuit designs like cascaded MZI[4,5] and ORRs combinations[4,6].

We report a silicon photonics waveguide mesh core capable of performing different RF-Photonic operations by simple reconfiguration and demonstrate two of these: MWP filtering and dispersive delay line. The programmable photonic core is based on a hexagonal waveguide-mesh architecture integrated in Silicon on Insulator (SOI).

Concept & Architecture

The demonstrated functionalities operate following a self-homodyne coherent scheme. With the proposed hexagonal mesh, reconfigurable and flexible optical filters can be directly translated to reconfigurable software-defined RF-photonics filters. Fig. 1 illustrates the general concept underlying on-chip programmable RF-photonic processors, where the hexagonal-mesh-based reconfigurable optical core can implement several PICs, such as cascaded unbalanced MZIs (UMZIs) and ORR-loaded MZIs. This is achieved by the suitable

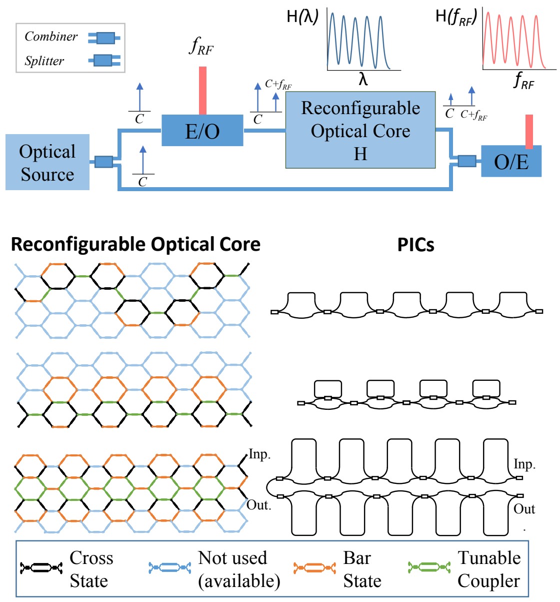

Fig. 1: Simplified scheme of self-beating RF-photonic systems employing single-side-band modulation and carrier injection (left). Examples of settings for the implementation of different cascaded PICs (right). E/O: Electro-optic converter, O/E: Opto-Electronic converter, RF: Radiofrequency.

programming of each Tunable Basic Unit (TBU) that comprises each hexagonal cell either as a tunable coupler or a discrete delay line in cross or bar state.

The TBU consists of a 2x2 balanced MZI loaded with a phase shifter (PS) on each arm. Each thermo-optic PS is implemented by means of a metal heater subject to the Joule effect. Overall, the TBU can synthetize independently the amplitude splitting ratio and the phase response. A detailed analysis of mesh topologies and the Basic Unit Length (BUL) implication shows that for hexagonal-mesh-based PICs, the FSR of the synthetized structures is given by[3]:

$$FSR = \frac{c}{n_g Interferometric\_Length} = \frac{c}{n_g N \cdot BUL}, \quad (1)$$

where c is the speed of light in vacuum, $n_g = 4.18$ is the waveguide group index, BUL = 975 μm, while N = 2, 4, 6, 8, … for the synthesis of unbalanced MZIs and N = 6, 8, 10, 12, 14, 16, ... for the synthesis of optical ring resonators.

Next, we demonstrate several selected configuration examples from the total of over 100 PICs that can be programmed on a 7-cell hexagonal mesh.

Fabrication

The device of Fig. 2 was fabricated in SOI wafers with a 220-nm thick silicon overlayer and a 3-μm thick buried oxide layer. E-beam lithography was employed to write the grating couplers. Dry etching of 70 nm into the silicon overlayer to form the grating couplers was then carried out followed by resist stripping. Another e-beam lithography and 120-nm silicon dry etching step was performed to produce the optical waveguides. Following resist stripping, 1 μm of PECVD silicon dioxide was deposited to act as the upper cladding layer of the waveguides. Photolithography was then performed to define isolation trench openings, followed by a deep dry etching process to etch through the top cladding, silicon overlayer and buried oxide layer providing thermal isolation to adjacent devices and improved the efficiency of the heaters. A 1.8-μm thick metal layer was deposited after the resist

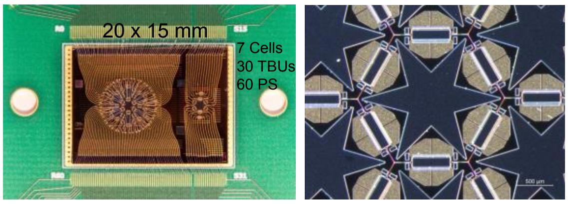

Fig. 2: Fabricated PCB-mounted photonic die (left) and fabricated hexagonal cell image (right).

had been stripped. A subsequent photolithography and dry etching step realised electrodes used to provide localised heating to tune the devices. The resist was then stripped and the wafers diced into individual dies. These dies were then mounted onto PCBs and a wire bonding process was used to provide electrical connections both within the die and between the die and the PCB.

Finite Impulse Response Circuits

UMZIs are 2-input/2-output periodic notch filters that constitute the basic building blocks for lattice and finite impulse response (FIR) transversal filters. By suitably tuning the MZI devices in the 7-cell waveguide mesh of Fig. 3 left, we implemented several UMZI devices with different FSRs limited by the number of current sources available at the moment of measurement. The periodicity in the transfer function or FSR changes according to the path unbalance (36.81 GHz for the 2-BUL UMZI, 18.4 GHz for the 4-BUL UMZI and 9.2 GHz for the 8-BUL UMZI) allowing for operation in the Ka, K and X bands, respectively. In each case, we compared the experimental results with those provided by the theoretical transfer functions, obtaining an excellent agreement. We also checked the tuning of the notch position over a complete spectral period by proper phase shifting in one of the UMZI arms, as illustrated on the inset of Fig. 3 (right) for a 2-BUL UMZI. The suppression of the carrier does not affect since the modulation scheme introduces carrier injection on the lower stage, as shown in Fig. 1.

By changing the values of k_1 to k_3, we tuned the positions of the two zeros provided by Fig. 3 structure and, therefore, reconfigured its transfer function.

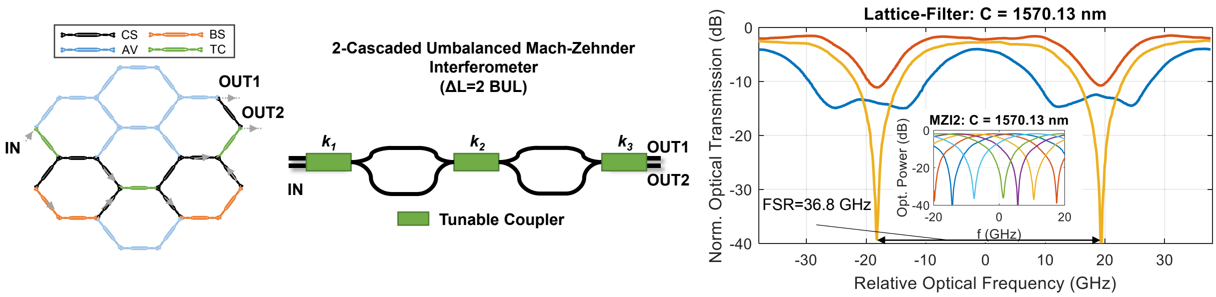

Fig. 3: Layout of the fabricated 7-cell hexagonal mesh and TBU settings (left) for the implementation of 2-cascaded UMZIs (middle). Optical Response for three different combinations of coupling coefficients (k) (right), and MZI2 tunability (inset).

Infinite Impulse Response

Ring cavities are either 1-input/1-output or 2-input/2-output periodic filters. In the first case, they implement all-pole infinite impulse response (IIR) notch filters, while in the second they can implement both IIR notch and FIR+IIR bandpass filters. They constitute the basic building blocks for more complex filter designs such as Cascaded Resonator Optical Waveguides (CROWs) and Series Coupled (SCISSORs). Figure 4(a) and 4(b) show the layout and implementation of a double-ring SCISSOR structure, respectively.

Fig. 4c shows that once a circuit topology design is programmed, its design parameters can be set as well, enabling in this case: Single ORR (dashed) and 2 cascaded ORRs with different resonance frequencies, i.e. moving its zeros and poles over the z-plane compared to a Doubled-ORR-Loaded MZI (dotted). In this case, the Insertion Losses corresponds to 3 dB for the SCISSORs and 7 dB for the DL-MZI. Again, full-FSR tunability can be achieved by exploiting the fact that the coupling constant and the phase shift in any MZI device of the mesh can be adjusted independently.

True Time Dispersive Delay lines

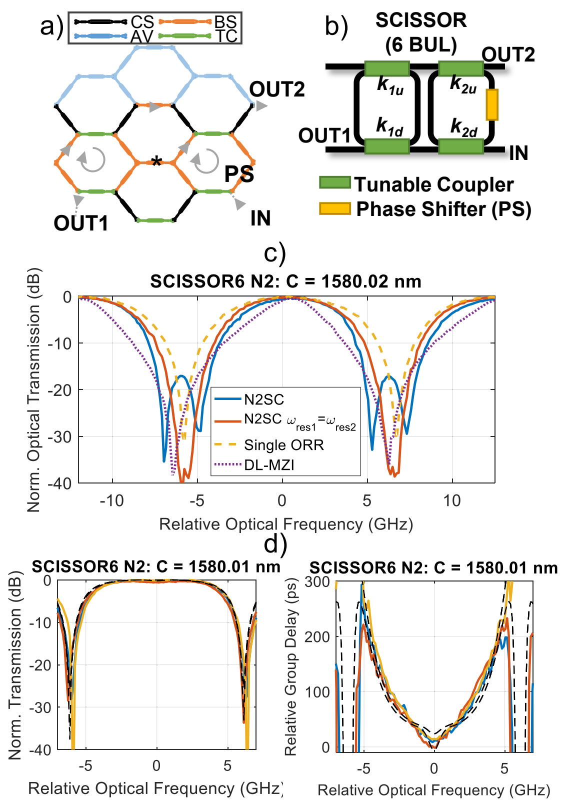

Fig. 4: (a) Layout of the fabricated 7-cell hexagonal mesh and TBU settings for the implementation of **(b)** 2-cascaded ORRs. **(c)** Optical Response for 2 critically coupled cascaded ORRs with PS variation (solid), one ORR (dashed) and Double-ORR-loaded MZI response (dotted). **(d)** Measured Optical Response and Group Delay for different sets of *k* and phases (SCISSOR).

True time dispersive delay lines are the building block of many RF-Photonic applications. The proposed core can be designed to perform arbitrary group delays for ideally flat-passband filters employing MZIs or ORRs. Fig. 4(d) shows the implementation of a parabolic dispersion compensator featuring up to 215 ps inside the 3-dB bandwidth of the filter, what translates to a dispersive delay coefficient of 4.3 ns/nm, equivalent to more than 200 km of optical fiber.

Conclusions

We have reported a silicon reconfigurable core for RF-photonics processing. The photonic circuit integrated in silicon can be programmed for different functionalities, of which we here have shown two: MWP filtering and dispersive true time delaying. The reported core enables the reconfiguration of both circuit topology and circuit parameters to provide full reconfigurability, tunability and flexibility. The BUL of our fabricated device relates the targeted FSRs to a set of discrete values that cover the S, C, X, Ku, K and Ka bands.

Acknowledgements

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