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***Abstract*—To address the semiconducting qubit biasing bottleneck, we develop a cryogenic analog demultiplexer operating 64 independent channels at 4 K and integrating a realistic 20 μm to 100 nm pitch reduction compatible with dense qubit arrays. We achieve <0.22% crosstalk while maintaining 0.44 μV/s maximum voltage drift. Our active router allows DC to >100 MHz signals to target static qubit polarization as well as fast (down to 3 ns) voltage pulses for qubit manipulation. From the extracted power consumption (3.54 μW/MHz/channel), we can extrapolate the thermal budget required to control future large-scale qubit arrays.**

***Index Terms*—qubit, biasing, sample-and-hold, signal multiplexing, crosstalk**

I. Introduction

Large-scale fault-tolerant quantum computing pushes for an ever-increasing number of quantum bits (qubits), which will quickly be compromised by the number of interconnects in any architecture directly wiring each qubit control signal to room temperature. The multitude of DC, baseband, and RF signals required to reach the dense qubit array at cryogenic temperatures is becoming a bottleneck, calling for scalable solutions. Semiconductor spin qubits already showcased key capabilities towards scalability by being seamlessly integrated with sub-Kelvin CMOS circuitry [1], or operating at temperatures of a few Kelvins [2] [3], and enabling qubit operations with baseband pulses. The unique opportunity to co-integrate a quantum chip with control circuits at similar temperatures paves the way to trading the current IO overcrowding with power, space, self-heating, and noise management issues.

In parallel with recent developments towards more scalable and complex quantum circuits [2] [4], several qubit control signals have been recently transposed from room-temperature electronics to cryogenic ICs. Pauka et al. [5] reported a multiplexed DC biasing, with a global square pulsing up to 100 MHz. Enthoven et al. [6] presented 15-bit DACs with a 157 µW power consumption for qubit biasing. Park et al. [7] implemented arbitrary 3.2 ms to 10 ns voltage pulsing using individual 11-bit DACs. Finally, Le Guevel et al. [1] and Ruffino et al. [8] focused on qubit state readout via cryogenic amplifiers and superconducting resonators, respectively. However, some key functionalities have yet not been reported, in particular the ability to independently tune several qubits in and out of resonance with a common addressing tone using 100 ns to 10 µs voltage pulses, while simultaneously maintaining multiplexed DC polarizations. Such baseband pulses are required for large-scale qubit addressing via Stark effect [4] or to implement two-qubit logic gates [9]. In addition, the minimum routing pitch reported by previous works is 225 nm [5], while spin qubits often present a 100 nm pitch or below [3] [4]. This dense metal routing affects the circuit's performances, e.g. amplifying crosstalk, and a comparable routing pitch should be used to validate the specifications and scalability of cryogenic ICs. Thus, a scalable and complete control scheme compatible with typical spin qubit pitch, limited power consumption (∼10 mW at 1K) and low footprint overhead (∼1 mm^2) has yet to be demonstrated.

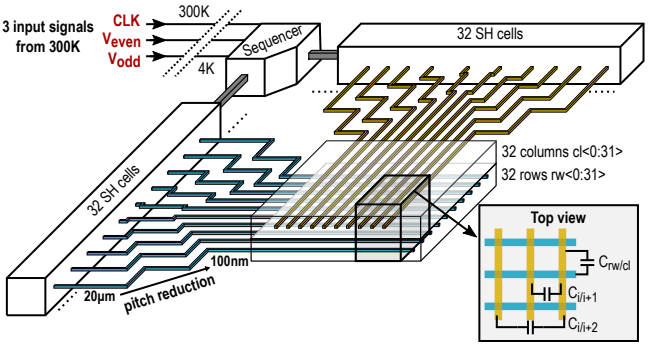

Fig. 1. Analog demultiplexer and adaptive routing.

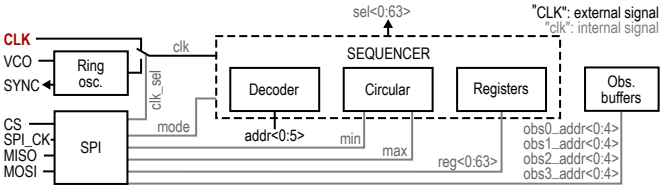

Fig. 2. Sequencer architecture.

This paper presents a 64-output programmable dynamic voltage biasing circuit operating at 4 K in 28 nm FDSOI technology co-integrated with a 100 nm-pitch dense routing matrix. This row-column addressing scheme was chosen as a worst-case scenario in terms of crosstalk among the possible

future quantum computers architectures. However, this 2-to-64 active router can accommodate qubit chips with shared or independent control voltages. It is compatible with 3D integration technologies: it can either be monolithically co-integrated with quantum circuits or be part of an active interposer stacked by flip-chip techniques [10] [11] directly on top of a qubit chip. The circuit architecture is presented in Section II, and we demonstrate the independent control of all 64 outputs in Section III. Sections IV and V study the performances (voltage crosstalk and drift, maximum operating frequency and power consumption) measured at $4\,\mathrm{K}$. From these metrics, we can estimate the power consumption for several large-scale applications, and compare with the available cooling power of standard cryogenic equipment.

II. Demultiplexer architecture

Large-scale qubit control requires increasing the density of connections from few mm-pitch inter-temperature cables, limited by cryogenic environments, to $100\,\mathrm{nm}$-pitch, typical distance between qubits. This is achieved by a combination of shared control signals and multiplexing techniques. However, some degree of individual control must remain to mitigate the large variability observed in semiconducting qubit technologies [12].

Fig. 1 presents the proposed analog demultiplexer based on 64 sample-and-hold (SH) cells, driven by a digital sequencer and 3 main inputs. Each $20\,\mu\mathrm{m} \times 20\,\mu\mathrm{m}$ SH circuit is composed by a pass gate switch and a $70\,\mathrm{fF}$ decoupling capacitor C_S, plus a $C_{par} = 22\,\mathrm{fF}$ parasitic capacitance to the substrate. This SH cell allows µs voltage refreshing cycles while reducing the crosstalk and maintaining the qubit polarization stable during the high impedance mode. A digital sequencer, configured using additional IOs or an SPI link, controls the pre-programmed activation of the 64 SH. Each qubit line is either connected to the V_{even} or V_{odd} voltage source from room temperature, with an alternating parity to minimize the first-order crosstalk between adjacent lines. We include a funnel-like smart layout routing from typical die-stacking microbump pitch ($20\,\mu\mathrm{m}$) down to a typical qubit gate pitch ($100\,\mathrm{nm}$) to include realistic crosstalk. The layout of this funnel metal routing (see also Fig. 10) has been carefully drawn to reduce parasitic capacitance down to $C_{i/i+1} = 0.3\,\mathrm{fF}$ between adjacent lines using a microstrip configuration while following technological design rules.

Fig. 2 describes the main building blocks of the analog/digital sequencer enabling the SH in a pre-programmed pattern synchronized with a clock input CLK (up-to $320\,\mathrm{MHz}$). Several alternative sequencing modes are available, including an analog 6-bit decoder, an incremental counter with adjustable min/max or a custom sequence from 1 to 64 registers. Four voltage amplifiers in a follower configuration each dynamically probe the voltage applied on a selected channel in high-impedance mode. Thus, this buffer has been designed to achieve a high input impedance not to overload the sensed line so as to allow fast sensing (MHz range).

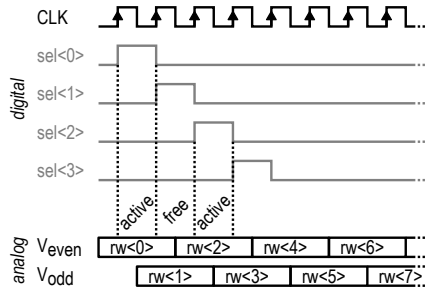

Fig. 3. Sequencer signals chronogram and alternating even/odd parity.

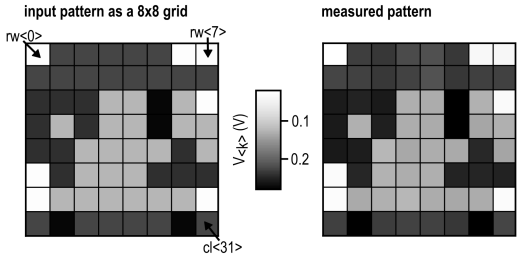

Fig. 4. Example of 64-pixels biasing.

III. Independent control of 64 signals

Fig. 3 shows typical signal waveforms for addressing all 64 outputs sequentially. The active channel is updated on every rising edge of the clock, according to the pre-programmed list of addresses from the circular counter or registers. The alternating parity allows to modify the even/odd input voltage when the opposite parity is active, making the addressing robust against input voltage rise times.

We can use the on-chip buffers to check the applied voltages on all outputs. As a first illustration, we programmed a predetermined pattern (represented in Fig. 4 as a 64-pixel picture) and measure all 64 output voltages. We observe no significant voltage mismatch between the input and measured patterns. To individually check each output, we then apply $0.8\,\mathrm{V}$ on a single channel <i>, while maintaining all other 63 channels at $0.2\,\mathrm{V}$. Using the observation buffers, we record all 64 output voltages and obtain (Fig. 5) a 1D trace exhibiting the expected

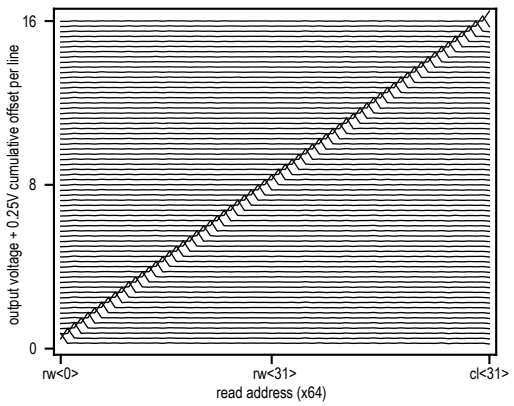

Fig. 5. Individual addressing of each output.

Dirac function. Repeating this experiment for every channel <i> (rw<0:31> and cl<0:31>), we demonstrate that each row/column is independently controllable.

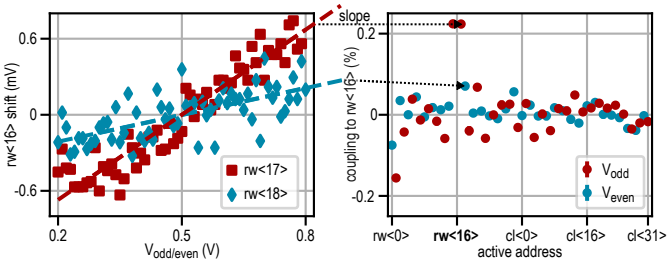

Fig. 6. Crosstalk measurement.

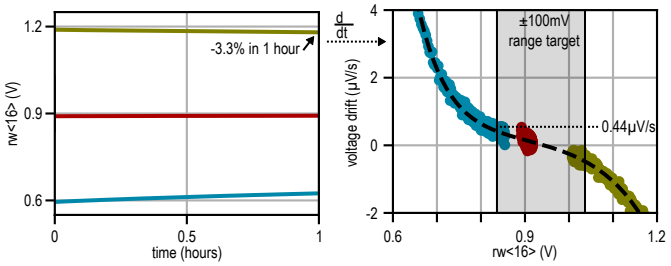

Fig. 7. Voltage drift rate at 4K.

IV. Crosstalk and Voltage Drift

As previously mentioned, the main focus driving this circuit's design was the minimization of the crosstalk while including a realistic routing down to 100 nm pitch, characteristic of finest metal levels. To achieve this objective, ground planes were included when possible between signal lines. In addition, the pass-gate switches were designed to effectively suppress parasitic coupling to the input signals $V_{even/odd}$. To control that the crosstalk is indeed dominated by the geometry of the routing, rw<16> is monitored while another channel rw/cl<i> is swept from 0.2 to 0.8 V (all other channels at 0.5 V). Repeating this measurement and extracting the slope for every i, we obtain the data presented in Fig. 6. As expected, a maximum of 0.22 % is observed for first-order neighboring channels (rw<15> and rw<17>), while the second-order crosstalk (to rw<14> and rw<18>) is limited to 0.05 % and the average crosstalk among all other 63 channels reaches 0.03 %. The measured first-neighbor crosstalk is in good agreement with the ratio of estimated parasitic capacitance between adjacent channels to the total capacitance of each SH cell ($C_{i/i+1}/(C_S + C_{par}) = 0.32\,\%$). Our 20 µm to 100 nm routing thus achieves a worst-case crosstalk that is negligible with respect to the typical cross-capacitance observed between gates defining the qubits (∼10 %) [12].

Fig. 7 presents the voltage drift estimation. rw<16> is first initialized at 0.6 , 0.9 or 1.2 V, and all other channels are kept at 0.5 V. The sequencer is then stopped and the voltage buffers outputs are recorded for several hours. A bi-exponential dependence of the derivative with the voltage is observed, indicating a slow leakage to $V_{DD}/2$. Nevertheless, for our target range of ±100 mV (typical for Silicon spin qubit manipulation), the voltage drift remains below 0.44 µV/s. The origin of the bi-exponential leakage to V_{SS} and V_{DD} are the ESD protection diodes on V_{even} and V_{odd} present in the circuit IO ring, which will be optimized in the next iterations of the circuit. Nevertheless, the voltage drift rate is greatly suppressed at cryogenic temperatures (by 4 orders of magnitude between 300 K and 4 K), validating the SH-based approach for qubit biasing. In particular, our circuit is able to maintain 64 independent output voltages with a <5 ppm accuracy using a 1 Hz refresh rate per gate (64 Hz base clock).

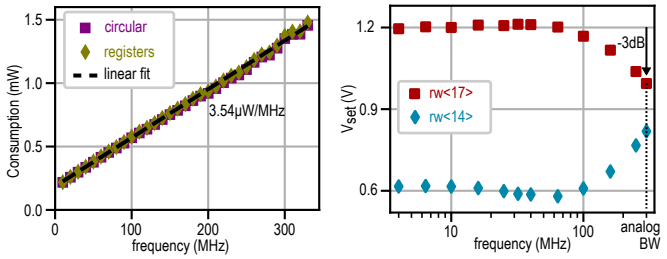

Fig. 8. Power consumption and bandwidth.

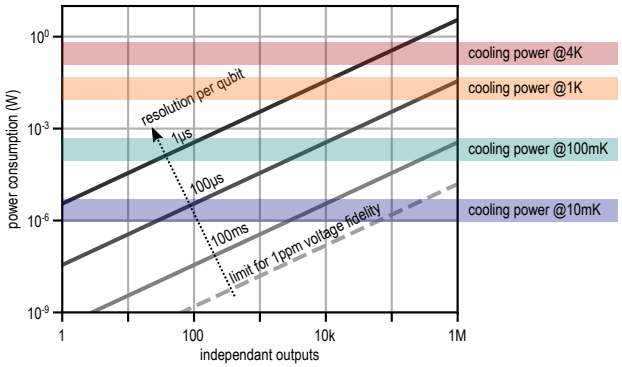

Fig. 9. Perspective for large-scale qubit control.

V. Operating Frequency and Power Consumption

On top of this individual DC biasing, semiconductor spin qubits require baseband (∼1 µs) voltage pulses to bring them in and out of resonance with each other or with an external excitation. To prove the ability of controlling DC and AC signals using our proposal active router, Fig. 8 presents the maximum operating frequency. To overcome the limited observation buffer bandwidth, we program all 64 outputs and stop the circuit with all outputs but cl<31> in high-impedance mode. In this state, the established voltages are preserved and, once the on-chip buffers are stabilized, two output voltages are sensed. Repeating this protocol while sweeping the clock period, we extracted a 320 MHz −3 dB bandwidth at 4 K. The demultiplexer is thus able to apply 64 arbitrary waveforms with a 5 MHz resolution to each controlled line, outperforming the targeted requirement for baseband qubit manipulation and

readout, especially for exploiting Stark effect. The power consumption of our active router increases linearly with the clock frequency with a slope of $3.54\,\mu W/MHz/channel$. The $180\,\mu W$ offset is mainly due to the observation buffers.

From the voltage drift extracted from Fig. 7 and the power consumption dependence on the master clock, we can estimate the power budget of larger matrices in realistic use-cases of quantum algorithms (Fig. 9). Because the available thermal budget (cooling power) scales as the square of the stage temperature, this diagram indicates the temperature range at which this circuits could operate. For example, $1\,M$ individual outputs could be controlled with a power consumption of $15.2\,\mu W$, compatible with a base temperature $<100\,mK$. However, in a realistic quantum algorithm a portion of the quantum array would need to be manipulated with µs pulsing on top of this DC-biasing, increasing the average power consumption of the circuit. Adding to our previous example a $1\,MHz$ pulsing of $1\,\%$ of the $1\,M$ outputs, the power consumption would reach $35.4\,mW$, and bring the operating temperature around $1\,K$. Thus, the power consumption of a SH-based multiplexing circuit strongly depend on the intended quantum algorithm and qubit array architecture.

VI. Conclusion

In this work, we demonstrate a stable multiplexed DC control and an individual MHz pulsing capability. The voltage decay rate is below $0.44\,\mu V/s$ for a $\pm 100\,mV$, sufficient to allow a $<5\,ppm$ voltage with a $1\,Hz$ refresh rate per gate. On the other hand, the maximum operating frequency of our circuit is $320\,MHz$, allowing us to also apply the baseband ($\sim$ µs) voltage pulses required for qubit manipulation. Our $20\,\mu m$-to-$100\,nm$ shielded routing (Fig. 10) limits the average voltage crosstalk to $0.03\,\%$, with a maximum of $0.22\,\%$ for adjacent lines, close to the value expected from capacitance simulation. This routing represent one possibility of qubit array control (row-column addressing), but our circuit would also be compatible with individual qubit addressing with a modified routing. In addition, our circuit is compatible with standard microbump pitches used for multi-chip assemblies, allowing stacking of Silicon spin qubits chips on top of our matrix [10] [11].

The requirements of large-scale qubit architectures are challenging for the cryogenic circuits used to control them. In particular, the significant qubit-to-qubit variability [12] pushes for an individual control of each qubit. Our approach of multiplexing all qubit signals from DC to MHz partially solves this challenge, trading the connection bottleneck problem for some requirements on the numbers of signals pulsed simultaneously and power and thermal management perspectives.

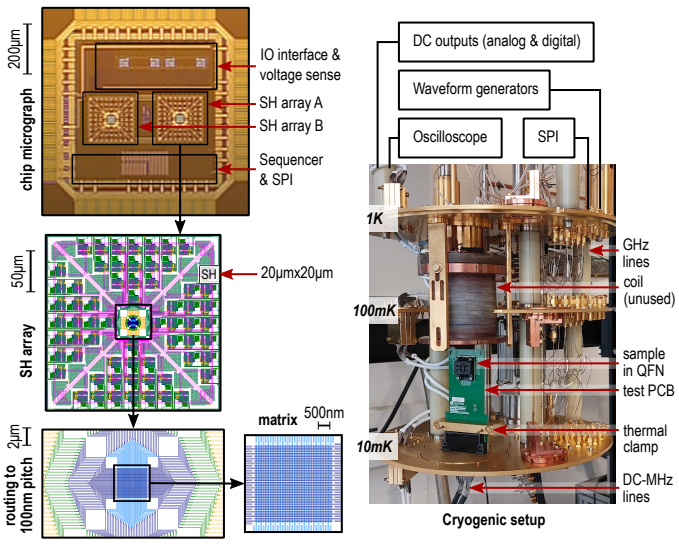

Fig. 10. Circuit layout, SH cells and test setup.

Acknowledgment

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References

[1] L. L. Guevel et al., "A 110mK 295μW 28nm FDSOI CMOS quantum integrated circuit with a 2.8GHz excitation and nA current sensing of an on-chip double quantum dot", 2020 IEEE International Solid-State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2020, pp. 306-308.

[2] C. H. Yang et al., "Operation of a silicon quantum processor unit cell above one kelvin", Nature 580, 350-354 (2020).

[3] M. Urdampilleta et al., "Gate-based high fidelity spin readout in a CMOS device", Nat. Nanotechnol. 14, 737–741 (2019).

[4] M. Veldhorst et al., "An addressable quantum dot qubit with fault-tolerant control-fidelity", Nat. Nanotechnol. 9, 981-985 (2014).

[5] S. J. Pauka et al., "A cryogenic CMOS chip for generating control signals for multiple qubits", Nat. Electron. 4, 64–70 (2021).

[6] L. Enthoven, J. van Staveren, J. Gong, M. Babaie and F. Sebastiano, "A 3V 15b 157μW cryo-CMOS DAC for multiplexed spin-qubit biasing", 2022 IEEE Symposium on VLSI Technology and Circuits, Honolulu, HI, USA, 2022, pp. 228-229.

[7] J. S. Park et al., "A fully integrated cryo-CMOS SoC for qubit control in quantum computers capable of state manipulation, readout and high-speed gate pulsing of spin qubits in Intel 22nm FFL FinFET technology", 2021 IEEE International Solid-State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2021, pp. 208-210.

[8] A. Ruffino et al., "A cryo-CMOS chip that integrates silicon quantum dots and multiplexed dispersive readout electronics", Nat. Electron. 5, 53–59 (2022).

[9] J. R. Petta et al., "Coherent manipulation of coupled electron spins in semiconductor quantum dots", Science 309, 2180 (2005).

[10] P. Vivet et al., "2.3 A 220GOPS 96-core processor with 6 chiplets 3D-stacked on an active interposer offering 0.6ns/mm latency, 3Tb/s/mm2 inter-chiplet interconnects and 156mW/mm2@ 82%-peak-efficiency DC-DC converters", 2020 IEEE International Solid-State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2020, pp. 46-48.

[11] C Thomas et al., "Superconducting routing platform for large-scale integration of quantum technologies", Mater. Quantum. Technol. 2, 035001 (2022).

[12] L. C. Contamin et al., "Methodology for an efficient characterization flow of industrial grade Si-based qubit devices," 2022 International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2022, pp. 22.1.1-22.1.4.