pHGen: A pH-Based Key Generation Mechanism Using ISFETs

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Abstract—Digital keys are a fundamental component of many hardware- and software-based security mechanisms. However, digital keys are limited to binary values and easily exploitable when stored in standard memories. In this paper, based on emerging technologies, we introduce pHGen, a potential-of-hydrogen (pH)-based key generation mechanism that leverages chemical reactions in the form of a potential change in ion-sensitive fieldeffect transistors (ISFETs). The threshold voltage of ISFETs is manipulated corresponding to a known pH buffer solution (key) in which the transistors are immersed. To read the chemical information effectively via ISFETs, we designed a readout circuit for stable operation and detection of voltage thresholds. To demonstrate the applicability of the proposed key generation, we utilize pHGen for logic locking—a hardware integrity protection scheme. The proposed key-generation method breaks the limits of binary values and provides the first steps toward the utilization of multi-valued voltage thresholds of ISFETs controlled by chemical information. The pHGen approach is expected to be a turning point for using more sophisticated bio-based analog keys for securing next-generation electronics.

Index Terms—Hardware security, emerging technologies, logic locking, key generation, ion-sensitive field-effect transistor.

I. INTRODUCTION

Security has recently become particularly important for hardware designs [1]. Especially, due to the high cost of manufacturing and maintaining nanoscale integrated circuit (IC) foundries, a significant portion of chips are designed and fabricated offshore [2]. This globalization of the IC design flow often leaks the vital information of the chips to untrustworthy parties and creates opportunities for intellectual property (IP) theft, overproduction, reverse engineering, counterfeiting, and insertion of hardware Trojans [3]. Techniques to ensure the security of hardware integrity through IC design and fabrication have been one of the emerging areas of information technology in recent years, where hardware security approaches utilize conventional digital keys to offer protection from an attack. However, there remain several ways to attack, such as exploitation of the digital data (e.g., secret keys in cryptographic applications) enabled by the highly vulnerable storage.

In this work, we present pHGen, a pH-based key generation mechanism that utilizes emerging transistor technologies to generate secure keys from (bio)chemical information. The biobased key generation offers multiple advantages over standard, binary keys, including a multi-valued representation, enhanced security in terms of physical key inspection, and a path towards

Fig. 1: The flow of pHGen.

personalized, biochemical digital keys. The main contributions of this paper are as follows (Fig. 1):

- The implementation of pHGen; a pH-based key generation mechanism that manipulates the voltage thresholds of ISFETs immersed into specific pH buffer solutions to extract analog chemical keys.
- The design and development of a stable readout circuit to read the intrinsic voltage threshold shift of ISFETs for integration with field-programmable gate arrays (FPGAs).
- The demonstration of pHGen for the generation of secure analog keys in logic-locked circuits.

II. PHGEN IMPLEMENTATION

A. ISFET- an Emerging Technology

To perform the transition from digital to analog keys, we utilize hydrogen ion (H+) concentration or pH values as they reflect chemical information. Miniaturized ion-selective sensors such as micro and nanoISFETs can be used as rapid analytical devices to detect small variations of free hydrogen and hydroxyl ions [4]. In this work, we use microISFETs as a test-board for well-established, reproducible, clean-room fabrication at wafer-scale, ion-recognition, and circuit-integration possibilities. Sensitive to surface-charge, ISFETs are utilized as chemical and biosensors to analyze solution samples in contact with its gate [5]. In addition, ISFETs offer possibilities for scalable integration using an unmodified CMOS process towards industrial application. ISFETs operate similar to MOSFETs, whose gate is extended with a passivation layer in contact with an external reference electrode (Ag/AgCl) via a sample solution (Fig. 2) also known as electrochemical gate configurations. The output current I_{DS} of an n-type transistor is expressed as follows:

$$
I_{DS} = \mu_n c_{ox} \frac{W}{L} (V_{GS} - V_{TH(ISFET)}) V_{DS} - \frac{1}{2} V_{DS}^2.
$$
 (1)

Fig. 2: (a) ISFET as a modified MOSFET technology and (b) equivalent electrical model.

In comparison to MOSFET, $V_{TH(MOSFET)}$ is replaced by $V_{TH(ISFET)}$ in eq. 1, which is influenced by surface charge changes as a function of the pH value of the solution in contact with the ISFET gate. Thus, ISFETs measure the solution pH in the form of threshold voltage change (V_{TH}) of a corresponding floating-gate MOSFET device. The electrochemical interface ($V_{CHEMICAL}$) consists of a reference built-in potential (V_{ref}) together with the double-layer capacitance known as Gouy–Chapman (C_{Gouy}) and Helmholtz (C_{Helm}) plane [6]. C_{Gouy} and C_{Helm} define the pH potential drop (V_{pH}) at the MOSFET gate and the C_{pass} is the passivation capacitance. The electrochemically induced voltage in the $V_{TH(ISFET)}$ can be defined as follows:

$$
V_{TH(ISFET)} = V_{TH(MOSFET)} - V_{CHEMICAL}, \quad (2)
$$

where $V_{CHEMICAL}$ is defined as:

$$
V_{CHEMICAL} = E_i + \frac{RT}{n_i F} ln(\alpha_i).
$$
 (3)

In eq. 3, E_i is the standard electrode potential, R: gas constant , T: absolute temperature (K) , F: Faraday constant, n_i : charge of ion i, and α_i : activity of ions. The only variable in eq. 3 is α_i . Thereby, to monitor the ion activity it is sufficient to keep V_{DS} and I_{DS} constant. In this case, V_{GS} is proportional to the natural logarithm of ion activity. Hence, the ISFET needs to be connected to a readout circuit to provide this condition.

B. Readout Circuit Design

A constant voltage constant current (CVCC) circuit is implemented as a readout circuit (ROC) to monitor the ion activity in response to an electrolyte solution that is in contact with the ISFET gate. For robustness, the sensor operates in the linear region, and the gate voltage is connected to the ground. Thus, the source voltage serves as the output signal proportional to the internal ISFET's threshold voltage $(V_{TH(ISFET})$. Fig. 3 shows the designed ROC. The voltage across ISFET's drain and source (V_{DS}) is constant and equal to $R1 * I$. In addition, the source current is half to that of the sink current, which according to Kirchhoff's current law, keeps I_{DS} constant and is equivalent to I. A current source circuit is used to generate the current sources. This

Fig. 3: Readout circuit designed for ISFET integration.

circuit includes an instrumentation amplifier (In-amp) and an operational amplifier. Therefore, the CVCC circuit ensures a constant operating current over ISFET's drain-source terminals $(I_{DS} = I = 50 \,\mu\text{A})$. Consequently, R1 constantly maintains V_{DS} = R1 * I = 10 kΩ * 50 µA = 0.5 V. In addition to current source circuits and the R1 resistance, the CVCC circuit comprises one operational amplifier (U1) connected to ISFET's drain providing feedback to the source and ensuring the functionality of the CVCC circuit. A buffer stage is employed to improve driving capability. Drawbacks related to temperature dependency [7] can be addressed by using a temperature sensor to compensate for the temperature effect.

III. DEMONSTRATION

Key-driven countermeasures, such as logic locking, have been proposed to protect the integrity of hardware designs through the IC design and fabrication flow [8]–[10]. Logic locking inserts a locking mechanism that ensures a correct circuit behavior only upon the application of a correct activation key. These inserted key-dependent gates are referred to as key gates. As the key is loaded post-fabrication by the IP owner, the design remains concealed while in the hands of untrusted third parties such as the external design house and foundry. To demonstrate the applicability of pHGen, we present a logic-locked circuit that uses the pH solution as the source of the input key to drive an XOR key gate. The demonstration was implemented with an MSFET 3330- 2 ISFET, which is a commercial ultra-miniature pH ISFET sensor from MICROSENS S.A [11]. It consists of siliconand polysilicon-based materials and a Ta_2O_5 gate as a pHsensitive metal with 4" planar CMOS process technology. The ISFET sensor dimensions are listed in Table I. The voltage

TABLE I: MSFET 3330-2 pH sensor dimensions.

	Width	Height	Length
Chip dimensions	$1.2 \,\mathrm{mm}$	$0.3 \,\mathrm{mm}$	$3 \,\mathrm{mm}$
Packaged sensor	$5 \,\mathrm{mm}$	1 mm	$50 \,\mathrm{mm}$

(a) ISFET pH sensitivity with (Ta_2O_5) gate at the temperature of 30°C.

(b) Reading the pH response and temperature information from the (bio)chemical-system.

Fig. 4: Results for (a) source voltage changes vs. pH solutions, and (b) gate source voltage change over the time at constant drain source voltage of 0.5V.

Fig. 5: Locked circuit schematic and implementation on the FPGA board with an FMC connector.

threshold shift per unit change in pH is defined as a pH sensor sensitivity [12]. With this sensor, we achieved a sensitivity of the conventional Nernst limit of $\Delta V = 59.2 \,\mathrm{mV}/\mathrm{pH}$ at a pH range of 4 to 9 and at the temperature of 30° C (Fig. 4(a)).

The output voltage (the source voltage of the ISFET (V_S)) changes proportionally to the pH value (pH 4 to 9), as presented in Fig. 4(a). The pH and temperature response of the ISFET over time are presented in Fig. 4(b) for two pH (4 and 7) and temperature levels (30°C and 40°C). However, more sensitivity can be attained by enlarging the sensing gate of an extended gate ISFET [13] or double gate ISFET design (front and back oxide capacitance) [14]. To measure the potential developed in the ion-sensitive gate, an ISFET together with a reference electrode (Ag/AgCl) must be immersed into the solution. For the solution, a phosphate buffer is prepared to adjust the pH value well between the pH range of 5.8 to 8.0, the example buffer that we used during the measurements is pH 5.8 with a voltage of 2.07 V (Fig. 4(a)). The reason to stay in the pH range of 5.8 to 8.0 is that many macromolecular properties are pH-dependent and stable within this range [15], thus enabling stable bio-based keys in the next stage. Table II summarizes the specifications of the designed readout circuit for $pH = 5.8$. A microfluidic system can be used to control the flow of the pH solution to drive more logic gates.

Fig. 6: Demonstration of logic locking with pHGen.

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To LO LO demonstrate the integration of the integration of the state of revision of the state of the state of the s a locked circuit was implemented by inserting a key gate (KG) in a selected gate-level netlist, as illustrated in Fig. 5. The pH-based key for the key gate is provided by a pH buffer solution ($pH = 5.8$). The gate of the ISFET was immersed into the buffer solution to read ion activity in the form of a voltage shift. Thus, the CVCC circuit reads the amount of voltage drift and buffers it to isolate the driver from the load. A voltage comparator constantly compares the voltage with the known pH voltage value. Because the IP owner designs the circuit and knows the correct voltage change from the pH-based key. To have a functional circuit, the output voltage obtained from the pH solution needs to be equal to the same designed voltage value. This voltage sets the value of the input pin of the key gate (XOR KG) via an FPGA Mezzanine Card (FMC) connector. The locked circuit was implemented on a ZedBoard Zynq-7000 FPGA board connected to an FMC. Four switches (SW 0-3) are set as input signals to two XOR gates and combined with a NOR gate to implement a pHGen logic locked circuit. An LED is connected to the output pin of a NOR gate to indicate the output signal. The FMC connector is used to bring modularity to change the I/O configuration of the design without FPGA intervention. Hence, a quad 2-input XOR gate IC is placed on the FMC connector. One of the XOR gates is used to establish a connection between the output voltage of the readout circuit and the input pin of the key gate. The FPGA-based test setup is shown in Fig. 6. The pH-driven

TABLE II: Readout circuit characteristics at 24°C, pH: 5.8.

	Typ
Supply voltage (V_{CC})	0.5V
Operating current (I_{DS})	$50 \mu A$
Internal drain voltage (V_D)	0.7V
Internal source voltage (VS)	0.2V
Output voltage (V_{OUT})	2.07V
CVCC circuit power consumption	$50 \,\mu\overline{W}$

TABLE III: Results of the demonstrated locked circuit.

key gate is added to the netlist, through the readout circuit, via the FMC connector. To demonstrate the key generation, the ISFET together with the reference electrode are immersed in the specific pH solution (secret key) to create a particular voltage shift and activate the XOR gate with the dedicated key value. The switches (SW 0-3) are considered as input signals and the results for all input patterns are shown in Table III. The obtained results state that the pH-key generation is feasible, CMOS-compatible, and can produce the same behavior as a conventional binary key in the form of voltage shift. Due to the robustness of the CVCC readout circuit, the ISFET operates in the linear region at a fixed drain-source voltage, independent of temperature and the power supply variation. Under these conditions, the pH solution's ion activity was monitored, and the output voltage was observed as a change in the ISFET threshold voltage. With the presented use case, we demonstrated the feasibility of using chemical information as a source to secure analog keys.

IV. NEXT STEPS

This novel approach of utilizing chemical information for securing ICs is expected to enable the application of nextin-line DNA-based nanoISFETs [16] [17] for personalized, secure systems. The work presented here establishes a basis for exploring the design of such chemically inspired secure ICs. In the next steps, we plan to extend the work to enhance the security aspects of logic locking in the following directions: (1) the design of multi-valued logic, (2) the implementation of massively parallel ISFET arrays to enable more key gates, and (3) the usage of nanoscale ISFETs to deploy super sensitive characteristics combined with high density and CMOScompatible integration. (4) Finally, a microfluidic system will be developed to automatically control the flow of the solution.

V. CONCLUSION

In this work, we presented pHGen, a novel analog key generation approach that can be utilized as an alternative to conventional binary keys. Emerging technologies, such as the ISFETs, ameliorate the change towards the use of analog keys. The key is generated by shifting the intrinsic voltage threshold of the ISFET, which is observed based on the changes in the pH-soluble ion activities. To demonstrate the proposed mechanism, we integrated pHGen with logic locking—a prominent technique to protect hardware designs against manipulations and piracy. According to the results, pHbased analog keys have the ability to substitute conventional digital keys. Hence, pHGen provides a stepping stone to using a chemical-based key with ISFETs.

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