Integrated SWIPT Receiver with Memory Effects: Circuit Analysis and Information Detection

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Abstract—**Wireless power transfer has been proposed as a key technology for the foreseen machine type networks. A main challenge in the research community lies in acquiring a simple yet accurate model to capture the energy harvesting performance. In this work, we focus on a half-wave rectifier and based on circuit analysis we provide the actual output of the circuit which accounts for the memory introduced by the capacitor. The provided expressions are also validated through circuit simulations on ADS. Then, the half-wave rectifier is used as an integrated simultaneous wireless information and power transfer receiver where the circuit's output is used for decoding information based on amplitude modulation. We investigate the bit error rate performance based on two detection schemes: (i) symbol-by-symbol maximum likelihood (ML); and (ii) ML sequence detection (MLSD). We show that the symbol period is critical due to the intersymbol interference induced by circuit. Our results reveal that MLSD is necessary towards improving the error probability and achieving higher data rates.**

Index Terms—**wireless power transfer, half-wave rectifier, circuit analysis, integrated SWIPT receiver.**

I. Introduction

Wireless power transfer (WPT) has been proposed as a key technology for the sixth generation (6G) networks, as a flexible and viable solution for powering up the low demanding devices of the foreseen machine type networks [1]. This is achieved by integrating into a radio frequency (RF) antenna a rectifying circuit which converts the ambient or dedicated electromagnetic radiation into direct current (DC) [2]. A conventional rectifier consists of a single diode and a capacitor which flattens the high output oscillations. This topology is known as half-wave rectifier and it provides high RF to DC conversion efficiency at low input power [3].

The benefits provided by WPT have attracted the interest of the research community where a critical challenge lies in applying a valid model for capturing the energy harvesting (EH) performance of the rectifier circuit. The linear input-output model has been widely used in the past years [4], but it only takes into account the circuit's conversion efficiency while it is independent of the input power level and neglects the non-linear behavior of the rectifier's components.

A more practical approach is presented in [5], where the authors propose a non-linear EH model based on the sigmoidal function, capturing the dynamics of the conversion efficiency for different input power levels. Moreover, the authors in [6], present an analytical model of the rectenna non-linearity through the Taylor expansion of the diode characteristics. Another model is proposed in [7], where the authors take into account both the forward and reverse current of the rectifying diode as well as the matching network and provide an expression for the harvested DC power. Furthermore, the authors in [8], take into account the memory introduced to the system due to the capacitor and model the circuit through a Markov decision process. The state transitions probabilities are obtained through a learning based approach by taking into account all the non-linear effects of the rectifier as well as the impedance mismatch.

Besides, RF signals constitute the fundamental medium for wireless communications and their ability to transfer energy has leveraged a significant interest in simultaneous wireless information and power transfer (SWIPT) systems [9]. The authors in [10], consider the SWIPT receiver utilizing a time-switching method to separate information decoding (ID) and EH modes. Another, well-investigated, approach for employing SWIPT systems, is the power-splitting protocol where a portion of the received signal is used for ID and the remaining part is used for EH [11]. The aforementioned SWIPT receivers implementing the time or power splitting approach, fall under the category of separated circuit architecture where the received signal is split towards EH and ID at the RF antenna front end. Another category, is the integrated SWIPT receiver, first introduced in [12], where the authors suggest to split the signal towards EH and ID at the rectifier's end, avoiding the need for RF to baseband conversion and thereafter reducing the circuit complexity of the SWIPT receiver. A more compact SWIPT solution is introduced by the authors in [13], suggesting to rely on amplitude modulation and exploit the rectifier's circuit to jointly design the EH and ID. Specifically, the authors suggest to apply a biased amplitude shift keying (ASK) where the minimum amplitude is non-zero in order to avoid zero harvested power. The authors extended their work in [14], where they derive an analytical symbol error rate expression for the integrated receiver circuit in the presence of additive white Gaussian noise (AWGN). However, the analytical circuit output is not provided while the memory

effects of the system are not investigated.

Different from previous works, in this paper, we take into account the memory induced by the capacitor and provide a simple yet accurate model to characterize the output voltage. The model, based on a half-wave rectifier, is derived through circuit analysis and its validity is confirmed with Advanced Design System (ADS) simulations. The half-wave rectifier model is then explored in the context of a SWIPT scenario. In particular, we consider an amplitude modulation scheme through which an integrated SWIPT receiver can decode symbols based on the circuit's output. We focus on the achieved bit error rate (BER) in the presence of noise but also on the RF EH. We investigate two detection schemes: (i) symbol-by-symbol maximum likelihood (ML); and (ii) ML sequence detection (MLSD). We show that, with ML detection, the symbol period is critical to the performance since intersymbol interference arises due to the capacitor's memory effects. Therefore, we apply MLSD, which improves the BER and allows for higher data rates. It is also shown that the MLSD converges to the conventional ML when the memory of the circuit is limited.

II. SYSTEM MODEL

Consider a wireless communications antenna which harvests energy through a half-wave rectifying circuit. The circuit is composed of a single diode D, enabling the rectification, a capacitor C, for flattening high output oscillations, and a load R_l. The received signal at the antenna which excites the circuit is modeled as a sinusoidal source with amplitude $\hat{V}_s$, expressed by

$$V_s(t) = \hat{V}_s \sin(\omega t), \quad (1)$$

where ω denotes the radial frequency. The antenna's resistance R_s, is also taken into account, and it is connected to the equivalent circuit as shown in Fig. 1(a).

For the diode's current-voltage characteristic we adopt a piece-wise model [2]. Let $V_D(t)$ and $I_D(t)$ denote the voltage drop and current at the diode, then

$$I_D(t) = \begin{cases} \frac{V_D(t)-V_{\text{on}}}{R_{\text{on}}} & \text{if } V_D(t) \geq V_{\text{on}}, \\ \frac{V_D(t)}{R_{\text{off}}} & \text{if } V_D(t) < V_{\text{on}}, \end{cases} \quad (2)$$

where V_{on} denotes the minimum voltage required for the diode to be switched on, and R_{on} and R_{off} correspond to the diode's resistance when switched on and off, respectively. Note that, the minimum threshold V_{on} is modeled as a DC component in the equivalent circuit. This piece-wise model enables the circuit analysis to be conducted for the individual states of the diode being on and off [2]. The equivalent circuits are depicted in Fig. 1.

In what follows, we first obtain the output voltage of the rectifier and then based on the circuit characteristics we investigate an amplitude modulation scheme such that the rectifier can be used as an integrated SWIPT receiver.
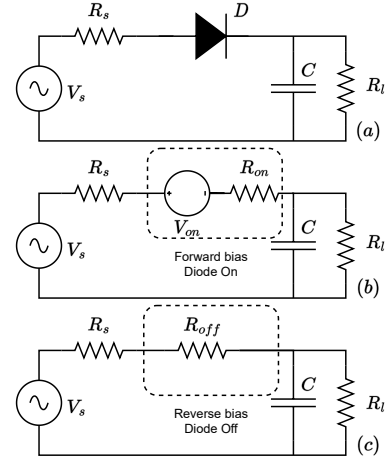

Fig. 1: (a) Half-wave rectifier and equivalent circuits when the diode is on (b) and off (c).

III. HALF-WAVE RECTIFIER'S OUTPUT

In this section, we provide the half-wave rectifier's output voltage as a function of the antenna's input by making use of the piece-wise model for the diode. For this purpose, we first provide the circuit analysis for each of the cases where the diode is forward or reverse biased by using the equivalent circuits depicted in Fig. 1(b) and (c), respectively. Then, we provide the algorithm that is used to obtain the circuit's output voltage.

A. Forward biased diode

We first focus on the case where the diode is on, and the equivalent circuit which is depicted in Fig. 1(b). By applying the Kirchoff's law for voltage we get

$$V_s(t) - (R_s + R_{\text{on}})I_1(t) - V_{\text{on}} - V_C(t) = 0, \quad (3)$$

where $V_C(t)$ denotes the output voltage i.e., the capacitor's voltage, and $I_1(t)$ is given by

$$\begin{aligned} I_1(t) &= I_C(t) + I_{R_l}(t) \\ &= C\frac{dV_C(t)}{dt} + \frac{V_C(t)}{R_l}. \end{aligned} \quad (4)$$

Let $T_{\text{on}} \triangleq C(R_s + R_{\text{on}})$ and $\alpha \triangleq \frac{1}{T_{\text{on}}} + \frac{1}{R_l C}$, then from the expressions in (3) and (4) we get

$$\frac{dV_C(t)}{dt} + \alpha V_C(t) = \frac{V_s(t) - V_{\text{on}}}{T_{\text{on}}}. \quad (5)$$

By considering that the diode switched on at $t_0^{\text{on}} < t$ with $V_C(t_0^{\text{on}}) = V_0^{\text{on}}$, the solution to the differential equation in (5) is given by

$$\begin{aligned} V_C(t) = &-\frac{V_{\text{on}}}{\alpha T_{\text{on}}} - \frac{\hat{V}_s(\omega\cos(\omega t) - \alpha\sin(\omega t))}{T_{\text{on}}(\alpha^2 + \omega^2)} \\ &+ e^{\alpha(t_0^{\text{on}}-t)}\left(V_0^{\text{on}} + \frac{V_{\text{on}}}{\alpha T_{\text{on}}} + \frac{\hat{V}_s(\omega\cos(\omega t_0^{\text{on}}) - \alpha\sin(\omega t_0^{\text{on}}))}{T_{\text{on}}(\alpha^2 + \omega^2)}\right). \end{aligned} \quad (6)$$
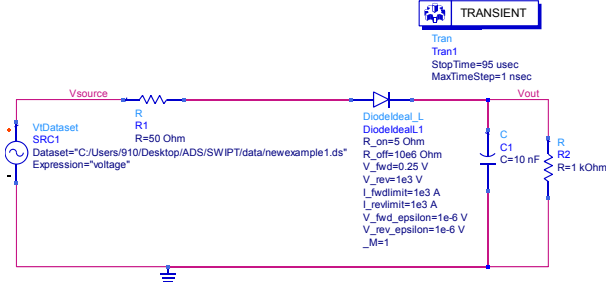
Fig. 2: Half-wave rectifier on ADS.

Note that, eq. (6) defines the rectifier's output up until the following expression becomes true

$$\frac{(V_s(t) - V_C(t) - V_{\text{on}})R_{\text{on}}}{R_s + R_{\text{on}}} < 0, \tag{7}$$

satisfying the condition $V_D(t) < V_{\text{on}}$.

B. Reverse biased diode

We now turn our attention to the case where the diode is switched off and modeled as a high resistance in the equivalent circuit as depicted in Fig. 1(c). By following a similar procedure as in Section III-A, we get the following differential equation

$$\frac{dV_C(t)}{dt} + \beta V_C(t) = \frac{V_s(t)}{T_{\text{off}}}, \tag{8}$$

where $T_{\text{off}} = C(R_s + R_{\text{off}})$ and $\beta = \frac{1}{T_{\text{off}}} + \frac{1}{R_l C}$. By considering that the diode switched off at $t_0^{\text{off}} < t$, with $V_C(t_0^{\text{off}}) = V_0^{off}$, the rectifier's output voltage is given by

$$V_C(t) = -\frac{\hat{V}_s(\omega \cos(\omega t) - \beta \sin(\omega t))}{T_{\text{off}}(\beta^2 + \omega^2)}$$
$$+ e^{\beta(t_0^{\text{off}} - t)}\left(V_0^{\text{off}} + \frac{\hat{V}_s(\omega \cos(\omega t_0^{\text{off}}) - \beta \sin(\omega t_0^{\text{off}}))}{T_{\text{off}}(\beta^2 + \omega^2)}\right). \tag{9}$$

The expression in (9) defines the output voltage until the diode switches on i.e., when

$$(V_s(t) - V_C(t))\frac{R_{\text{off}}}{R_s + R_{\text{off}}} \geq V_{\text{on}}, \tag{10}$$

satisfying the condition $V_D(t) \geq V_{\text{on}}$.

C. Transient Time Analysis

In order to capture the rectifier's output within a time period we make use of the two expressions in (6) and (9) along with the conditions for the diode to switch on (forward biased) or off (reverse biased). The circuit's output is then obtained through a transient time analysis. The pseudo code used for carrying out the transient time output of the circuit is depicted in Algorithm 1, where we consider 100 samples per input period [2]. Moreover, besides obtaining the analytical output, the half-wave rectifier is implemented and evaluated through simulations by using the ADS software as depicted in Fig. 2.

The output of the algorithm and simulation from ADS is illustrated in Fig. 3, for constant $\hat{V}_s$, revealing that the

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Algorithm 1 Rectifier's transient time output

1: $state = 0$ ▷ Diode is off
2: $V_{\text{out}}(t) = 0$ ▷ Output voltage is zero
3: $t_0^{\text{off}} = 0$ ▷ Set initial conditions
4: set $V_0^{\text{off}} = 0$
5: **for** $t \leq T_{sim}$ **do**   ▷ T_{sim}=Total evaluation time
6:     $V_s(t) = \hat{V}_s \sin(\omega t)$
7:     **if** $state = 0$ **then**
8:         $V_{\text{out}}(t) = $ Eq. (9)
9:         **if** $V_D(t) \geq V_{\text{on}}$ **then**
10:            $state = 1$ ▷ Diode turns on
11:            set $t_0^{\text{on}} = t$ ▷ Update initial conditions
12:            set $V_0^{\text{on}} = V_{\text{out}}(t)$
13:     **else if** $state = 1$ **then**
14:         $V_{\text{out}}(t) = $ Eq. (6)
15:         **if** $V_D(t) < V_{\text{on}}$ **then**
16:            $state = 0$ ▷ Diode turns off
17:            set $t_0^{\text{off}} = t$ ▷ Update initial conditions
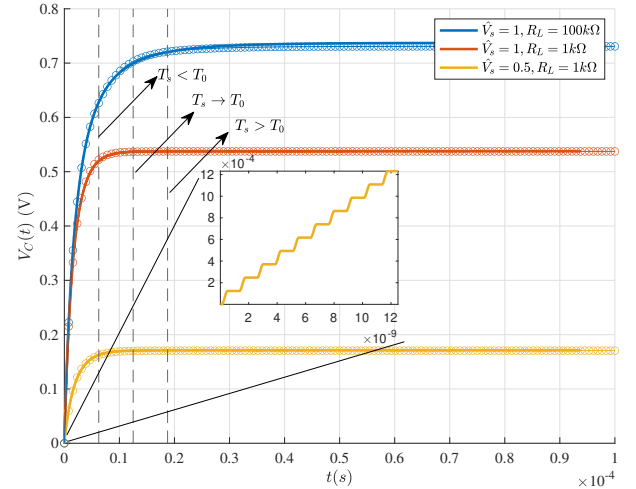18:   set $V_0^{\text{off}} = V_{\text{out}}(t)$

Fig. 3: Rectifier's output voltage $V_C(t)$; Lines and markers correspond to analytical and ADS simulation, respectively; $f = 800$ MHz ($\omega = 2\pi f$), $C = 10$ nF, $R_{\text{on}} = 5\Omega$, $R_s = 50$ Ω, $R_{\text{off}} = 10$ MΩ, $V_{\text{on}} = 0.25$ V and $\hat{V}_s = 1$.

analytical results are matched with the simulation results. In addition, we can observe that the output voltage across the load increases in each period. Moreover, over a long-time period the output of the circuit is captured by an exponential curve reaching a certain steady state. In reality though, the output voltage increases gradually within each period in a non-continuous manner as depicted within the zoomed figure. Also, when the load of the circuit is very large and acts as an open circuit, the capacitor's charge increases rapidly until the voltage across reaches $V_C(t) \approx \hat{V}_s - V_{\text{on}}$. On the other hand, when a load is present at the circuit, the capacitor discharges accordingly and the achieved steady state is at a lower value of $V_C(t)$.

IV. MEMORY-BASED INTEGRATED SWIPT RECEIVER

In this section, we apply the presented half-wave rectifier model to a simple communication setup with an integrated SWIPT receiver. Specifically, by considering amplitude modulation, we investigate the circuit's ability for symbol detection based on its output. The motivation for using amplitude modulation stems from the fact that the rectifier converts the input to one direction current flow [13]. Now, in order to achieve a non-zero harvested power, we consider the following:

(i) A biased M-ASK modulation scheme is applied [13], [14], where the k-th information symbol is mapped to a certain amplitude $\hat{V}_s = A_k$, $k \in \{0, 1, \ldots, M-1\}$.

(ii) A minimum symbol amplitude $A_k \geq A_{min} > V_{\text{on}}$ is set since the charging period of the capacitor starts once the diode's threshold is surpassed.

At the receiver's side, we assume that sampling is performed at the end of each symbol period. By denoting the symbol period by T_s, the i-th symbol can be written as

$$x_i = V_C(t - iT_s). \qquad (11)$$

We assume that the noise due to sampling is an AWGN and thus the i-th symbol to be detected is

$$\begin{aligned} y_i &= x_i + n_i \\ &= V_C(t - iT_s) + n_i, \end{aligned} \qquad (12)$$

where $n_i \sim \mathcal{N}\left(0, \sigma^2\right)$ and σ^2 denotes the variance of AWGN.

As explained in Section III-C, under specific circuit parameters, for each symbol amplitude at the input of the circuit i.e., $V_s(t) = A_k \sin(\omega t)$, the capacitor achieves a specific steady state after a certain time period. Let the steady state achieved with symbol A_k be denoted by a_k. Thus, for $A_k > A_l$, it holds that $a_k > a_l$, where $k \neq l$. Note that, with symbol A_k as the input at the circuit, the capacitor will charge or discharge accordingly from its current state towards reaching a_k. Moreover, to mitigate intersymbol interference, the symbol amplitudes are chosen in such a way so that $||A_k - A_l||$ is large. This results in $||a_k - a_l||$ also being large, which corresponds to the largest euclidean distance that any two symbols would have between them.

In what follows, we provide two detection schemes that can be applied based on the symbol period T_s. More precisely, if T_s is large enough to lead the capacitor to its steady state, then we know that $x_k \approx a_k$. On the other hand, the value of x_k cannot be determined accurately (it depends on the capacitor's memory) and thus there is a higher probability of error. Clearly, the duration needed for reaching the steady state from an arbitrary level varies. However, for the sake of simplicity and brevity, we consider the cases $T_s > T_0$ and $T_s < T_0$, where T_0 is the time interval needed for reaching the steady state from an empty capacitor; for instance, in Fig. 3, $T_0 \approx 15\ \mu s$ for the case $R_L = 1$ kΩ.

A. Maximum-Likelihood Detection

We first consider the conventional symbol-by-symbol ML detection scheme. It is worth mentioning that, the ML detector
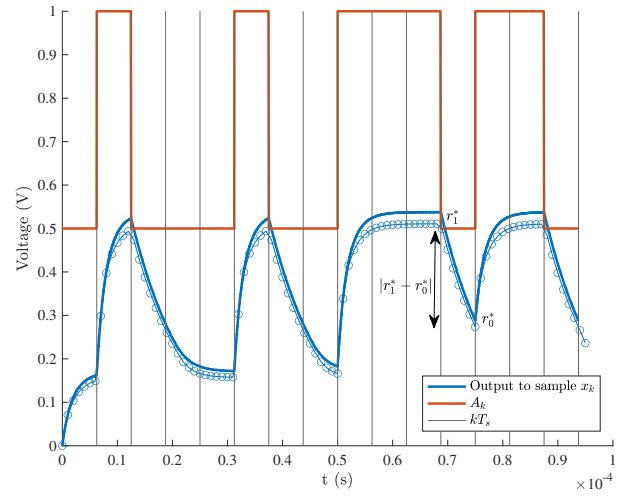

Fig. 4: Transmission of 15 bits with $T_s = 6.25\mu s$; markers correspond to ADS simulation; $f = 800$ MHz, $C = 10$ nF, $R_L = 1$k Ω, $R_s = 50$ Ω, $R_{\text{on}} = 5\Omega$, $R_{\text{off}} = 10$ MΩ, $V_{\text{on}} = 0.25$.

is always applicable in the case $T_s > T_0$, which refers to an interference-free scenario. Specifically, when $T_s > T_0$, then $x_k \approx a_k$ and the i-th detected symbol $\hat{x}_i$ is expressed by

$$\hat{x}_i = \arg\min_{x_j} |y_i - x_j|, \qquad (13)$$

where y_i and x_j are given by (12) and (11), respectively. Let us now focus on a smaller symbol period i.e., $T_s < T_0$. Even though a larger information rate is achieved, a smaller symbol period does not guarantee that the circuit reaches a steady state. In fact, for a given symbol period smaller than T_0, it is not possible to determine where exactly the level of the capacitor is. However, it is possible to provide a range for the output values for each symbol input. In the case where these ranges do not overlap, we can exploit them to form a decision rule and provide an upper bound for the theoretical performance. Specifically, let $r_k^{\min}$ and $r_k^{\max}$ denote the minimum and maximum output, respectively, of the k-th symbol when adjacent symbols are transmitted; these can be obtained with Algorithm 1. Then, the decision region for the k-th symbol is $\rho_1 \leq y_i \leq \rho_2$, where $\rho_1 = (r_k^{\min} - r_{k-1}^{\max})/2$ and $\rho_2 = (r_{k+1}^{\min} - r_k^{\max})/2$. On the other hand, if these ranges overlap, the symbols cannot be distinguished between them. This effect can be avoided through the proper design of the circuit, that is, through its parameters such as minimum input, maximum transmitted power, etc. This allows a constellation with sufficiently large euclidean distance between the symbols such that the decision regions are non-overlapped.

In what follows, we provide a specific example for the binary ASK (BASK) modulation. When $T_s > T_0$, the decision bound for detecting symbol A_1 is $y_i \geq \rho$ and for A_0 is $y_i < \rho$, where $\rho = |a_0 + a_1|/2$. Then, since the two symbols are equiprobable, the error probability over AWGN is given by

$$\mathcal{P}_e = Q\left(\frac{a_1 - a_0}{2\sigma}\right), \qquad (14)$$

where $Q(\cdot)$ is the Q-function. Now, when $T_s < T_0$, the rectifier's output alternates in specific ranges for each symbol. Let r_1^* and r_0^*, denote the minimum and maximum output of symbols with mapping amplitudes A_1 and A_0. These output values would result in the minimum euclidean distance between the sampled symbols i.e., $\min\{||x_1 - x_0||\} = ||r_1^* - r_0^*||$. An example is depicted in Fig. 4, indicating the closest values of two consecutive and adjacent symbols with $A_1 = 1$ and $A_0 = 0.5$. In this example, $T_s < T_0$ and we can observe the symbol duration relative to the steady state in Fig. 3. Following from the aforementioned, for the symbol detection, ML can be applied by assuming that $x_j = r_j^*$, where $j \in \{0, 1\}$. Recall that, as the symbol period increases, then $x_j \to a_j$ and $r_j^* \to a_j$. In this case, the theoretical upper bound captures the actual error probability.

B. Maximum Likelihood Sequence Detection

A general detection scheme which is optimal for any symbol period T_s, is the maximum likelihood sequence detection. In this case, the input at the detector consists of K received symbols forming a sequence of length K which is denoted by $\mathbf{y}$. Then, a sequence is detected according to

$$\hat{\mathbf{x}} = \arg\min_{\mathbf{x}_m} ||\mathbf{x}_m - \mathbf{y}||^2, \qquad (15)$$

where $\mathbf{x}_m$ denotes the m-th sequence of K consecutive symbols. In order to obtain all the possible sequences, transient time analysis of the circuit is used over M^K sequences. Note that, since the capacitor induces memory to the system M^K sequences should be obtained for all the possible output levels. For ease of comparison, we assume that the system has a finite memory of L symbols. This corresponds to sequential transmission of L symbols followed by an artificial replacement of the charged capacitor with an empty capacitor. Note that, the sequence detection becomes necessary when the symbol period is small relative to reaching the steady state due to the memory effects of the capacitor.

C. Energy Harvesting Performance

In order to capture the energy harvesting performance we measure the instantaneous power at the load at the end of each symbol period. The instantaneous power at the load is given by

$$P_l(t) = \frac{V_C(t)^2}{R_l}. \qquad (16)$$

For a sequential transmission of length L we evaluate the average power of a sequence by

$$P_L = \frac{1}{L} \sum_{i=1}^{L} P_l(t - iT_s). \qquad (17)$$

V. NUMERICAL RESULTS

In this section we provide the SWIPT receiver's performance in terms of both, ID and EH. For this purpose we use transient time analysis as explained in Section III-C. Unless otherwise stated, we use $f = 800$ MHz ($\omega = 2\pi f$), $C = 10$ nF, $R_L = 1k\ \Omega$, $R_s = 50\ \Omega$, $R_{on} = 5\Omega$, $R_{off} = 10$ MΩ,
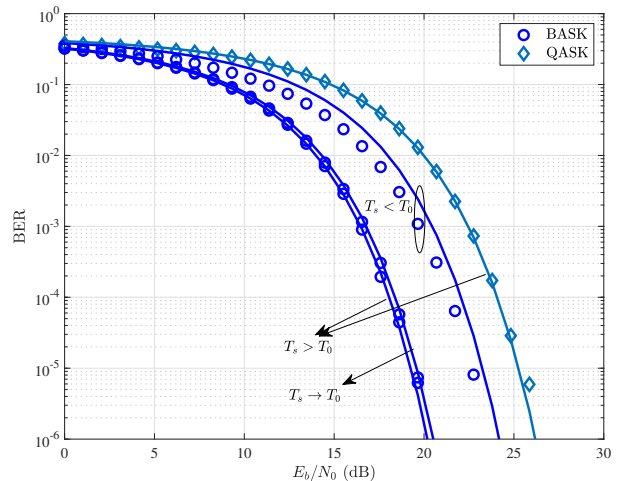

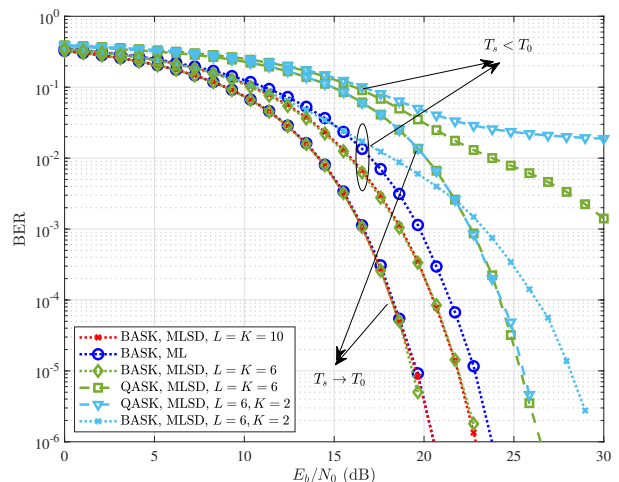Fig. 5: Bit error rate performance with respect to SNR with symbol-by-symbol ML detection.

Fig. 6: Bit error rate performance with respect to SNR with MLSD.

$V_{on} = 0.25$. For the BASK modulation scheme we consider $A_{min} = 0.5$ hence the amplitudes $A_0 = 0.5$ and $A_1 = 1$ are used. The normalized σ is obtained based on the transmitted symbol power as follows. The $m-$th symbol's power is given by $P_m = \frac{1}{2T_s} \int_{-T_s}^{T_s} |A_m \sin(\omega_0 t)|^2\, dt = A_m^2/2$, and the average symbol power is given by $P_{av} = \frac{1}{4} \sum_{m=0}^{1} A_m^2$. Then, since $\frac{E_b}{N_0} = \frac{P_{av}}{2\sigma^2}$, it occurs that $\sigma = \sqrt{\frac{P_{av}}{2E_b/N_0}}$, where in this case $P_{av} = \frac{5}{16}$. Moreover, for a fair comparison with the quadrature ASK (QASK) modulation, we keep the average symbol power constant as well as the same minimum symbol amplitude i.e., $A_{min} = 0.5$ and set $A_m = A_{min} + md_s$, where $d_s = (1/14)(\sqrt{30}-3)$ and $m \in \{0, \dots, 3\}$. The corresponding normalized σ in this case is given by $\sigma = \sqrt{\frac{P_{av}}{4E_b/N_0}}$, since two bits per symbol are transmitted. For the sake of comparison we consider three symbol periods, $T_s < T_0 = 6.25\mu s$ and $T_s \to T_0 = 12.5\mu s$ and $T_s > T_0 = 18.75\mu s$ which are indicated in Fig. 3 to depict the symbol period's selection with respect to the steady state output.

In Fig. 5, we plot the BER performance based on symbol-by-symbol ML detection with respect to the signal to noise ratio per bit E_b/N_0. We plot BASK and QASK for the case where $T_s > T_0$, i.e., each symbol is sampled at its corresponding steady state. As can be seen, in both cases the transient time analysis matches with the theoretical error probability obtained by utilizing the steady state values. Furthermore, for the BASK modulation we compare the performance over three different symbol periods. For the cases where $T_s \leq T_0$, in order to define the decision regions for each symbol, we first obtain r_0^* and r_1^* which are then used for the defining the symbols' detection regions. Clearly, when a smaller symbol period is used, a worse performance occurs as the boundary between the symbols becomes smaller. This is due to the fact that there is not enough time for the capacitor to reach the corresponding symbol's steady state. Moreover, the theoretical $\mathcal{P}_e$, in these cases correspond to an upper bound as it captures the closest euclidean distance it might occur. As T_s increases $r_k^* \approx a_k$ and the theoretical $\mathcal{P}_e$ captures the actual performance which is better compared to applying a smaller T_s, since a larger euclidean distance between the symbols occurs. For the QASK modulation, a smaller T_s results in a more severe intersymbol interference which imposes the use of MLSD in order to achieve higher data rate.

In Fig. 6, we consider sequential transmission i.e., a finite memory of length $L = 6$ symbols. We plot the BER with respect to E_b/N_0 for BASK and QASK where MLSD is applied with $T_s \in \{6.25, 12.5\}$ μs. As expected, when the symbol period and the sequence length K, increase, a better performance is achieved. Moreover, for the BASK we also compare the MLSD performance with the symbol-by-symbol ML. Clearly, when $T_s < T_0$, the MLSD detection outperforms ML. However, when $T_s \rightarrow T_0$, the MLSD converges to the ML detection since the effect of the memory in the system is eliminated and there is no intersymbol interference. Moreover, when $L = K$, the performance is the same even for higher L i.e., the same performance is achieved when $L = 10$.

Finally in Fig. 7, we plot the average sequence output power for three different symbol periods when BASK is applied. Interestingly, the best performance is achieved when a lower T_s is used. This occurs from the fact that a lower symbol period does not allow the capacitor to discharge enough towards the lower steady state that a low amplitude symbol would result.

VI. Conclusions

This paper proposed an accurate and simple-to-use model to characterize the output voltage of an EH circuit based on the half-wave rectifier topology. The validity of the analytical expressions was confirmed with ADS simulations. The proposed model was further explored in the context of a SWIPT scenario under the memory effects introduced by the capacitor. We showed that, with ML detection, the symbol period is critical to the BER performance due to intersymbol interference. Therefore, we also applied MLSD, which improves the BER and allows for high data rates.
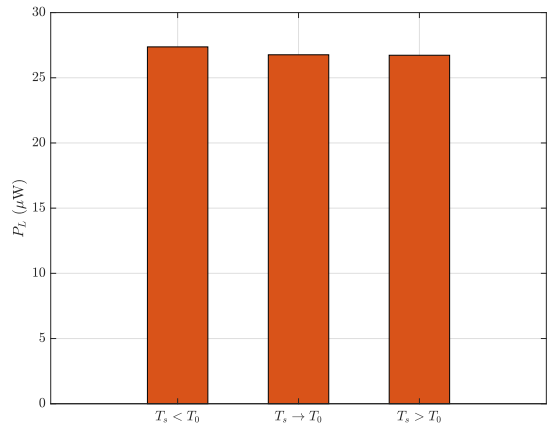

Fig. 7: Average sequence power for BASK, $L = 6$.

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