On the influence of strong magnetic field on MOS transistors

Luc Hebrard, Duc-Vinh Nguyen, Dorian Vogel, Jean-Baptiste Schell, Chrystelle Po, Norbert Dumas, Wilfried Uhring, Joris Pascal

On the influence of strong magnetic field on MOS transistors

L. Hébrard, D. V. Nguyen, D. Vogel, J.-B. Schell,
C. Po, N. Dumas, W. Uhring
ICube – Université de Strasbourg / CNRS
23, rue du Loess – Strasbourg, France

J. Pascal
University of Applied Sciences and Arts Northwestern
Switzerland FHNW, Muttenz, Switzerland

***Abstract*— This paper presents a study on the influence of strong magnetic field on NMOS transistors' electrical characteristics. Experiments have been carried out in a small animal 7T MRI scanner, and have shown that up to 7T the influence exists but remains manageable. It is demonstrated that it depends on the transistor size, on the orientation of the chip inside the field, and on the V_{GS} voltage. A theoretical analysis in good agreement with experiments has been developed. Extrapolation to ultra-high field, i.e. above 10T, shows that at such a field magnitude the influence may be challenging, asking for specific design techniques to devise in order to make the circuit immune to the strong magnetic field.**

Keywords—MOS transistors, strong magnetic field

I. INTRODUCTION

Although the static magnetic field of clinical Magnetic Resonance Imaging (MRI) scanners for human body are till now limited to 1.5T or 3T, high-field small animal 7T MRI scanners are already widely used for diseases study on animal models, and for the assessment of potential drugs aimed at fighting these diseases. In addition, a few dozens of human body 7T MRI scanners are also installed worldwide for clinical research [1], as well as a few units with a static field of 9.4T [2]. Projects targeting 10.5T and even 11.7T human body scanners are under progress [3], and small animal 14.1T MRI scanners are also available [2]. This trend in increasing the MRI magnetic static field is driven by a higher MR signal allowing a much better Signal-to-Noise Ratio (SNR) and high resolution images. As a consequence, potential capabilities of ultra-high-field MRI (7T and above) are expected to be wide [1], especially for the brain study. In practice, the MR signal is sensed with an inductive coil and transferred to a signal processing box placed outside the strong magnetic field area. However, it is well known that better SNR is achieved when the processing electronics is close to the coil, i.e. inside the strong magnetic field area. In addition, since the best signal is achieved when the coil size is similar to the sample to analyse [4], the best way to sense MR signals from small tissue volume, typically 1 µL, is to co-integrate on a single chip, or in a multi-chip specific design, the sensing coil and its electronics in order to build a minimally-invasive MR micro-probe [5] [6] that will be implanted into the body. However in such a system, the electronics has to work under the strong magnetic field, which may be very challenging. Although integrated systems working under 1.5T and 3T for magnetic tracking within human body MRI scanners have been recently demonstrated [7], as well as integrated circuits working under 7T for NMR micro-imaging [8], no deep study has been provided yet on the influence of strong magnetic field on electronics. However, engineers who develop electronic systems for MRI instrumentation know that electronic circuits may exhibit curious behaviour in such environment, and a few experiments carried out twenty years ago have already reported strong influences of high magnetic field on commercial Field Effect Transistors [9] [10]. In contrast a recent study carried out on CMOS transistors integrated in the X-FAB 0.35µm CMOS technology concludes that MOS transistors working under subthreshold seem to be quite immune to high magnetic field, up to 12T [11]. However, in this recent experiment, long-length transistors have been used, and the conclusion is not readily relevant for circuit designers since wide-and-short transistors, i.e. transistors with a high W/L, are generally used in circuits to have a high transconductance (W and L denote respectively the width and the length of the transistor).

This paper provides a new study on the influence of strong magnetic field on MOS transistors' characteristics, and shows that the influence exists, as expected, but depends subtly on the transistor biasing. The next section describes the experiment carried out in a small animal 7T MRI scanner. Then section III provides a theoretical analysis which explains the experimental results. Finally, before conclusion section IV extrapolates the expected influence under ultra-high-field, i.e. up to 14.1T, and gives some design guide rules to minimize the magnetic field influence on the circuit behaviour.

II. EXPERIMENTS

A. Experimental setup

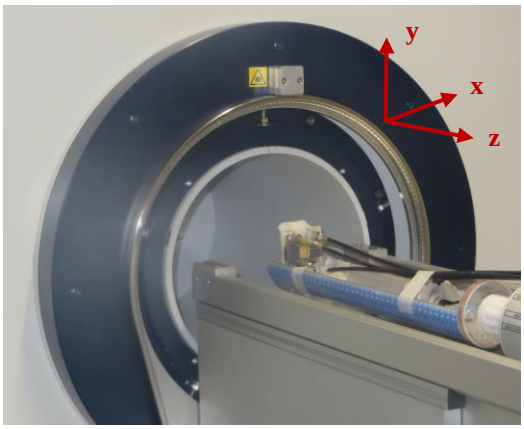

Fig. 1. Chip under test in the MRI scanner, just before entering inside the scanner bore where a 7T field holds. The NMOS channel plate, i.e. the chip plane, is perpendicular to the magnetic field which is aligned with the scanner bore z-axis.

To perform our study, a chip which integrates various NMOS transistors has been fabricated in the AMS 0.35µm CMOS technology. In this paper, we will focus on two of these

transistors. Both are interdigitated with two legs, the first one, M0, with W/L = 20/20, and the second one, M1, with W/L = 20/0.35. It means that each leg of M0 has a 10/20 size, while each leg of M1 has a 10/0.35 size. The chip was encapsulated in a DIL ceramic package whose metallic cap was removed since it was slightly attracted when placed in the strong magnetic field. It means that it should contain a small concentration of ferromagnetic components (Fe, Ni, or Co) and would have deviated the magnetic field from its expected direction. The chip was thus placed on a small printed circuit board (PCB) featuring BNC connectors in order to connect an Agilent 4156C Semiconductor Parameter Analyzer to the transistors. The PCB was designed to fit into the small animal cradle in order to be easily moved inside the bore of a 7T Bruker BioSpec 70/30 MRI scanner (see Fig. 1). The Agilent 4156C was placed outside the shielded room where is located the MRI scanner, and was connected to the chip through coaxial cables.

B. Measurements

For several positions of the chip the I_{DS}-V_{GS} and I_{DS}-V_{DS} characteristics of both NMOS transistors were recorded. First the chip was outside the scanner room, i.e. under the low earth magnetic field. We will named this position P_0, the earth magnetic field being negligible. Then the characteristics were recorded (i) with the chip perpendicular to B_0 = 7T (position $P_\perp$), i.e. with the chip placed vertically as shown in Fig. 1, B_0 being aligned along the z-axis (see Fig. 1), and (ii) with the chip placed horizontally (position $P_{//}$), i.e. with its plane parallel to B_0. In position $P_{//}$ the chip was also rotated by 90°, as well as flipped upside down, and whatever the $P_{//}$ position, no influence of the magnetic field was observed. On the contrary, in the $P_\perp$ position, a no negligible influence was recorded. In addition, this influence has the same magnitude when the chip is flipped, i.e. rotated by 180° along the x-axis (see Fig. 1 for axis definition). Finally, from its $P_\perp$ position, the chip was also rotated by roughly 30° along the y-axis, as shown in Fig. 2. We will named this position $P_{\perp 30}$. In this last position, a B_0 influence was also registered, but lower than in position $P_\perp$. Since influences were only observed in position $P_\perp$ and $P_{\perp 30}$, only the measurements in these two positions, as well as in position P_0, will be reported.

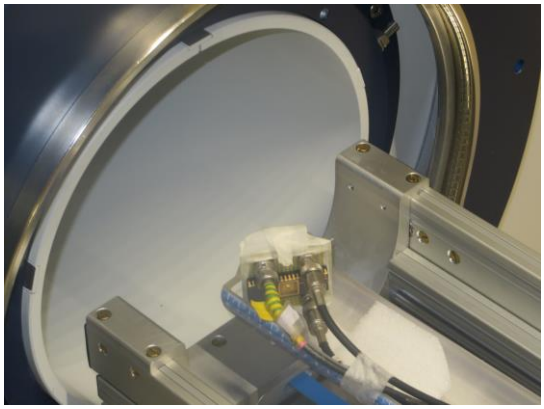

Fig. 2 : Chip in position $P_{\perp 30}$.

B.1. I_{DS}-V_{GS} characteristic

The I_{DS}-V_{GS} characteristic was recorded for V_{DS} = 10 mV and V_{GS} varying from 0V to 2V. Such a measurement is reported in Fig. 3 for M1 in position $P_\perp$. The different regimes of the transistor, i.e. *OFF*, *ON* in saturation, and *ON* in linear, are also shown in the figure.

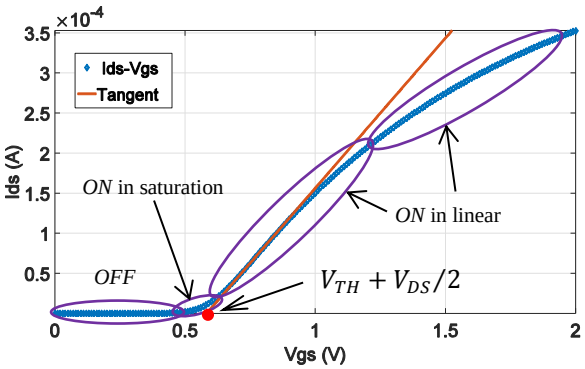

Fig. 3: Measured I_{DS}-V_{GS} characteristic of transistor M1 in position $P_\perp$. V_{DS} has a constant value of 10 mV. The red straight line is the tangent to the I_{DS}-V_{GS} curve at maximum slope.

Using the well-known SPICE LEVEL 1 analytical MOS model, the I_{DS}-V_{GS} characteristic in the linear regime reads [12-p.17]:

$$I_{DS} = \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot \left(V_{GS} - V_{TH} - \frac{V_{DS}}{2}\right) \cdot V_{DS} \qquad (1)$$

where μ_n is the electron mobility in the transistor channel, C_{ox} the gate oxide capacitance per unit area, and V_{TH} the threshold voltage. This equation is only valid in the linear regime (see Fig. 3). Taking the derivative dI_{DS}/dV_{GS} gives the slope:

$$\alpha = \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot V_{DS} \qquad (2)$$

When V_{GS} increases the electrons are pushed towards the oxide-silicon interface and the carrier mobility is reduced due to surface scattering [13 – p. 142]. This well-known phenomenon explains why the slope α is not constant over the whole linear region. As seen in Fig. 3, it decreases when V_{GS} increases. Drawing the tangent to the I_{DS}-V_{GS} curve with the maximum α slope (red straight line in Fig. 3) we can determine [13 – p. 156] (i) the transistor threshold voltage V_{TH} by extrapolating the tangent till I_{DS} = 0, and (ii) the usual maximal transconductance parameter $KP_n = \mu_n \cdot C_{ox}$, generally provided by the CMOS design kit, and used by the designer to determine by hand calculation the transistors' sizes once the biasing current is chosen. Note that such a value for KP_n is only valid for small V_{GS}, i.e. small $V_{GS} - V_{TH}$, which is generally the case because designers bias the transistors close to the moderate inversion in order to maximize the transistor transconductance without too much biasing current. Instead of considering the usual maximum value of α, we determined α for different values of V_{GS}, i.e. V_{GS} = 0.6V, 0.8V, 1V, 1.2V, and 1.5V. Results are summarized in Table 1 for M0 and M1 in positions P_0, $P_\perp$, and $P_{\perp 30}$.

It is worth to notice that $V_{TH} \approx 560$ mV was not influenced by the strong magnetic field. On the contrary, α is reduced. This is very clear for M1, and this reduction is stronger on the short transistor, M1, than on the long one, M0. In addition, for a given biasing, the reduction of α is smaller when the transistor is in position $P_{\perp 30}$ than in $P_\perp$. The slight increase observed for M0 in $P_{\perp 30}$ when V_{GS} = 1V and 1.2V is not relevant. Indeed, α being a derivative, the error on its computation is amplified by the measurement noise. So, in position $P_{\perp 30}$, where the reduction of

α is small, the computation noise is certainly higher than the magnitude of α change, i.e. close to ±1%, which explains why the deviations on α observed for M0 are not relevant. We will thus now focus our study on M1, the reason for the lower magnetic sensitivity of M0 being discussed in section III.

V_{GS} (V)	α (µA/V) M0 in P_0	M0 in $P_\perp$		M0 in $P_{\perp 30}$	
		α (µA/V)	$\alpha(P_\perp)$ versus $\alpha(P_0)$	α (µA/V)	$\alpha(P_{\perp 30})$ versus $\alpha(P_0)$
0.6	8.40	8.18	-2.62%	8.36	-0.48%
0.8	8.39	8.13	-3.10%	8.32	-0.83%
1	8.11	7.98	-1.60%	8.16	+0.62%
1.2	7.70	7.57	-1.69%	7.79	+1.17%
1.5	6.86	6.68	-2.62%	6.86	-0.07%

Table 1: Slope α for M0 (W/L = 20/20) versus V_{GS} for relevant positions of the chip

V_{GS} (V)	α (µA/V) M0 in P_0	M1 in $P_\perp$		M1 in $P_{\perp 30}$	
		α (µA/V)	$\alpha(P_\perp)$ versus $\alpha(P_0)$	α (µA/V)	$\alpha(P_{\perp 30})$ versus $\alpha(P_0)$
0.6	401	374	-6.73%	381	-4.99%
0.8	396	370	-6.57%	378	-4.55%
1	330	313	-5.15%	317	-3.94%
1.2	271	259	-4.43%	263	-2.95%
1.5	199	193	-3.02%	196	-1.51%

Table 2: Slope α for M1 (W/L = 20/0.35) versus V_{GS} for relevant positions of the chip

B.2. I_{DS}-V_{DS} characteristic

The I_{DS}-V_{DS} characteristic was recorded for V_{DS} varying from 0V to 2V, at V_{GS} = 1V, 1.5V, and 2V. Relevant values for V_{GS} = 1V, and $V_{DS} \geq$ 0.5V, i.e. when the NMOS is in saturation and strong inversion, are summarized in Table 3.

V_{DS} (V)	I_{DS} (µA) M1 in P_0	M1 in $P_\perp$		M1 in $P_{\perp 30}$	
		I_{DS} (µA)	$I_{DS}(P_\perp)$ versus $I_{DS}(P_0)$	I_{DS} (µA)	$I_{DS}(P_{\perp 30})$ versus $I_{DS}(P_0)$
0.5	708	674	-4.80%	684	-3.39%
1.0	748	713	-4.68%	724	-3.11%
1.5	772	737	-4.53%	748	-3.25%
2.0	793	757	-4.54%	768	-3.15%

Table 3: I_{DS} in M1 (W/L = 20/0.35) for V_{GS} = 1V and relevant values of V_{DS}, in positions P_0, $P_\perp$, and $P_{\perp 30}$.

We notice that, as expected, the saturated I_{DS} current is reduced, and this reduction does not depend on V_{DS}. Interestingly, the relative reduction of I_{DS} in saturation at V_{GS} = 1V is similar to the relative reduction of α for V_{GS} = 1V in linear region, i.e. around 5%. The same observation was done for V_{GS} = 1.5V, i.e the relative variation of I_{DS} in saturation is around -3%, close to the -3.02% observed in Table 2.

III. THEORY AND RESULTS ANALYSIS

The transistor channel is simply a resistor, and thus can be seen as a Hall plate. However, in magnetic Hall plate sensor, we always chose to have a long resistor, typically 3 times longer than wide (see Fig. 4-a), in order to avoid the Hall voltage short circuit through the biasing contacts [14]. As seen in Fig. 4-b, when the Hall plate is short, the Hall voltage cannot be established and the biasing current lines are tilted by an angle θ, increasing the sensor input resistance, i.e. the resistance across the basing contacts.

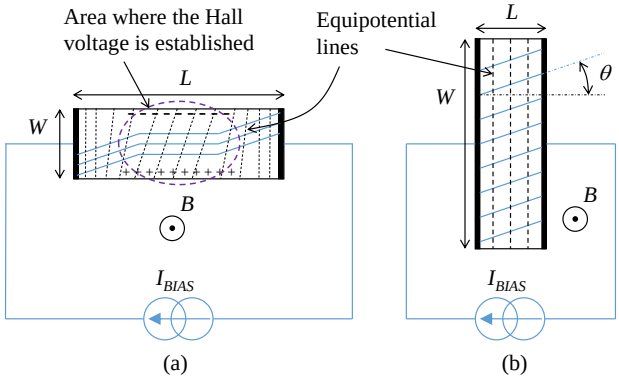

Fig. 4: (a) In a long Hall plate, $L/W \geq 3$, the Hall voltage has room to be established and the current lines remain undeviated, at least in the center of the plate, (b) In a short plate, $L/W \leq 1$, the Hall voltage is shorted by the biasing contacts, and the current lines are tilted, increasing the resistance of the plate.

Using the galvanomagnetic equations, one can show that the tilt angle is given by [15]:

$$\tan\theta = r_H \cdot \mu_n \cdot B \quad (3)$$

where r_H is the Hall scattering coefficient, close to 1 in highly doped n-type silicon [16], and B is the magnetic component perpendicular to the plane of the chip. Assuming r_H = 1 in the channel (high carrier concentration), and μ_n close to 500 $cm^2 \cdot V \cdot s^{-1}$, a typical value for surface mobility in a n-type channel, then $\tan\theta \leq 0.35$ for $B \leq 7$T, and we can assume with a good approximation that $\tan\theta \approx \theta$ up to B = 7T. As shown in Fig. 4-b, under magnetic field, the carriers flow on a longer distance than under zero-field, leading to an increase of the input resistance by a factor of $1/\cos\theta \approx 1 + \theta^2/2$. The same phenomenon arises for short transistor where the effective transistor length increases, leading to a current in linear regime given by:

$$I_{DS-B} = \mu_n \cdot C_{ox} \cdot \frac{W}{L \cdot (1+\theta^2/2)} \cdot \left(V_{GS} - V_{TH} - \frac{V_{DS}}{2}\right) \cdot V_{DS} \quad (4)$$

which can be approximated to:

$$I_{DS-B} \approx I_{DS-0} \cdot \left(1 - \frac{(r_H \cdot \mu_n \cdot B)^2}{2}\right) \quad (5)$$

where I_{DS-0} denotes the current under zero-field, given by eq. (1). The same way, the current in saturation is given by:

$$I_{DS-B} \approx \frac{1}{2} \cdot \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH})^2 \cdot \left(1 - \frac{(r_H \cdot \mu_n \cdot B)^2}{2}\right) \quad (4)$$

It means that whatever the regime of the transistor, linear or saturation, the current relative reduction factor (RRF) reads:

$$RRF = (I_{DS-B} - I_{DS-0})/I_{DS-0} = (r_H \cdot \mu_n \cdot B)^2/2 \quad (5)$$

The same RRF applies for the slope α of equation (2). Taking the above values for μ_n and r_H, we get a reduction factor of 6.1%, which has to be compared with the 6.73% reduction measured for V_{GS} = 0.6V and 6.57% for V_{GS} = 0.8V (Table 2), as well as with the roughly 5% reduction for V_{GS} = 1V (Tables 2 and 3). Theory is thus in good agreement with experiments, the lower RRF for V_{GS} = 1V being explained by the reduction of the carrier mobility which starts for V_{GS} above 0.8V (see Fig. 3).

The above comparison between experiment and theory is debatable since we do not know the exact value of r_H and μ_n. So, an interesting way to look at the results while getting rid of these values is to compute the ratio of the reduction factor in position $P_{\perp 30}$ to the reduction factor in position $P_{\perp}$, i.e. $RRF(P_{\perp 30})/RRF(P_{\perp})$. Since transistors should be sensible only to the magnetic field component which is perpendicular to the plane of the chip, whatever the values of r_H and μ_n, such a ratio should be equal to $(\cos\beta)^2$, where β is the angle by which the chip was tilted along the y-axis to be placed in position $P_{\perp 30}$. This ratio has been computed from Tables 2 and 3, leading to Tables 4 and 5, and an average value of 0.68 for $(\cos\beta)^2$ .It gives $\beta = 35°$, in good agreement with the experiment.

V_{GS} (V)	$\frac{RRF(P_{\perp 30})}{RRF(P_{\perp})}$
0.6	0.74
0.8	0.69
1	0.77
1.2	0.67
1.5	0.50

Table 4: Computation of $(\cos\beta)^2$ from Table 2, i.e. for M1 in linear (V_{DS} = 10 mV)

V_{DS} (V) V_{GS} = 1V	$\frac{RRF(P_{\perp 30})}{RRF(P_{\perp})}$
0.5	0.71
1.0	0.66
1.5	0.72
2.0	0.69

Table 5: Computation of $(\cos\beta)^2$ from Table 3, i.e. for M1 in saturation and V_{DS} = 1 V

Finally the lower reduction factor observed for transistor M0 is due to its length. Being of 20 µm, it means that the channel size of each leg of the transistor is L × W = 20µm × 10µm, and the Hall voltage has enough room to be established along the channel [14], reducing the deviation of the current lines, at least at half-way of the channel, as shown in Fig. 4-a. This results in a lower reduction of the physical magneto-resistivity of the channel, and thus in a transistor more immune to the magnetic field effect.

IV. DISCUSSION

Given biasing voltages V_{GS} and V_{DS}, we have shown that a strong magnetic field perpendicular to the chip plane may have a no negligible influence on the biasing current flowing in the transistor, especially when *W*/*L* is higher than 1, which is typically the case in integrated circuits. It induces a deviation of the current lines leading to an increase of the channel resistance, and a lowering of the current. Such a lowering leads also to a reduction of the transistor transconductance g_m…, and may thus have an influence on the circuit behaviour. However, the current reduction is proportional to $(\mu_n \cdot B)^2$ where B is the magnetic field perpendicular the chip plane. Since μ_n decreases when V_{GS} increases, it is better to bias the transistors with a high overdrive voltage $V_{GS} - V_{TH}$. Although such a biasing means a low g_m/I_{DS} ratio, asking for a high consumption to get a given g_m, this helps in minimizing the influence of the magnetic field on the circuit behaviour. Measurements have shown that the biasing current reduction may reach almost 7% under 7T for a conventional overdrive voltage of 100 mV. Such a reduction, which depends on the chip orientation in the magnetic field, is easily manageable. In addition, it should be technology independent, at least if the carrier mobility remains the same from one technology node to the other one. However, since the biasing current reduction is also proportional to B^2, it means that under 14.1T, a possible field for small animal MRI scanner, the current deviation may reach 28%, a value which could be an issue for development of 14.1T MRI compatible instrumentation.

V. CONCLUSION

This paper has studied the influence of strong magnetic field on MOS transistors. Although new experiments are still required to confirm our predictions, especially at very high field, we have experimentally shown that the influence is moderate up to roughly10T. However above 10T, the magnetic field may lead to biasing current variation above 15%, which could ask for specific design techniques to make circuits immune to magnetic field. A few design recommendations to lower the magnetic field influence have also been given.

REFERENCES

[1] O. Kraff, A. Fische, A. M. Nagel, C. Mönninghoff, and M. E. Ladd, "MRI at 7 Tesla and Above: Demonstrated and Potential Capabilities", Journal of Magnetic Resonance Imaging, vol. 41, 2015, pp. 13-33

[2] Private discussion with Pr. Klaus Scheffler, Max Planck Institute for Bilogical Cybernetics, Tübingen, Germany

[3] E. Moser, and al., "7-T MR – from research to clinical applications?, NMR in Biomedicine, vol. 25, 2012, pp. 695-716

[4] D. Hoult, R. Richards, "The signal to noise ratio of the nuclear magnetic resonance experiment", Journal of Magnetic Resonance, 1976, pp. 24-71

[5] N. Baxan, A. Rengle, G. Pasquet, J.-F. Château, A. Briguet, P. Morin, and L. Fakri-Bouchet, "Investigation of NMR limits of detection for implantable microcoils", Proc. of IEEE EMBS, 2007, pp. 4194-4197

[6] J. Trejo Rosillo, "Contribution à l'amélioration de la sensibilité d'un micro-récepteur RMN implantable", PhD. Thesis, n° 264-2014, Nov. 2014, Université Claude Bernard – Lyon I

[7] J.-B. Schell, and al., "Hall effect magnetic tracking device for Magnetic Resonance Imaging", IEEE Sensors Conference, 2013, pp. 1382-1385

[8] J. Anders, J. Handwerker, M. Ortmanns, and G. Boero, "A fully-integrated detector for NMR microscopy in 0.13 µm CMOS", IEEE Asian SSC Conference, 2013, pp. 437-440

[9] J. R. Bodart, and al., "The effect of high magnetic fields on junction field effect transistor device performance", Review of Scientific Instruments, 1998, pp. 319-320

[10] P. Phothimat, M. Awipi, "Effect of High Magnetic Field on Transistor Characteristics With Applications to SEU Testing", Proc. of IEEE Southeastcon'98, 1998, pp. 338-339

[11] J. Höfflin, and al., "Subthreshold CMOS Transistors are Largely Immune to Magnetic Field Effects When Operated Above 11T", Concepts in Magnetic Resonance Part B (Magnetic Resonance Engineering), 2015, DOI: 10.1002/cmr.b

[12] B. Razavi, "Design of Analog CMOS Integrated Circuits", Mc Graw Hill Ed., 2001

[13] Y. P. Tsividis, "Operation and Modeling of the MOS transistor", Mc Graw Hill Ed., 1988

[14] J.-B. Kammerer, and al., "Hall effect sensors integrated in standard technology and optimized with on-chip circuitry", The European Physical Journal – Applied Physics, vol. 36, 2006, pp. 49-64

[15] R. S. Popovic, "Hall Effect Devices", Second Ed., Institute of Physics Publishing, 2004

[16] I. G. Kirnas, P. M. Kurilo, P. G. Litovchenko, V. S. Lutsyak, and V. M. Nitsovich, *Phys. Status Solidi (A)* vol. 23, 1974, K123-K127.