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***Abstract*—A detailed analysis of Off-state gate-oxide breakdown (BD) mode and its location under non-uniform electric field is performed in 28nm FDSOI N-MOSFET devices. We show that hard breakdown (HBD) occurs exclusively from the middle of the channel to the drain overlap extension for Off-state TDDB. HBD is characterized under DC stress with different gate-length L_G as a function of drain voltage V_{DS} and temperature. We check that the leakage current is the better monitor for TDDB dependence precursor to HBD under Off-mode stress by using the proper modeling and discussing the different possible origin of the higher form factor β value under Off mode stressing.**

Index Terms--CMOS, charge trapping, hard breakdown, interface traps, Off-state damage, soft breakdown.

I. INTRODUCTION

TDDB remains a key reliability concern in ultra-short channel CMOS nodes with the guaranty of speed performance and low consumption requirements. Even if Off-state stress generally degrades device at a smaller rate than On-state stress, it can become a limiting factor with HBD under RF operation in the millimeter wave domain (5G) **[1-3]**, where supply voltage V_{DD} may be usually doubled with respect to the one used for logic application. Thus, device parameter drifts might become significant in correlation to soft breakdown that may trigger hard breakdown into the gate-drain region once a critical density of localized defects is generated. Many papers discuss from lateral profiling of interface damage during Off-state stress that the peak degradation occurs outside of the gate-edge. Breakdown spot is then estimated to occur in the spacer region, collocated with peak interface damage **[4-5]**. Although a reasonable consensus has been reached on Off-state breakdown mechanism, drain and gate leakage currents after BD were found to coincide, confirming that percolation path in dielectric stack was created at drain edge **[6-8]**.

Recently Off-state hot-carrier degradation (HCD) has been associated to broken ≡Si─O bonds at the interface **[4]** with a bond dispersion model showing higher time exponent (n=0.7 – 0.8), extending the findings to a universal modeling to On-state degradation **[5]**. Classical HCD On-state has been historically associated with broken ≡Si─H bonds at Si/SiO_2 interface. However, recent reports deal with interaction between On and Off modes **[9-11]** and show that gate-oxide degradation can indeed occur during HCD On-state **[12-13]**. The V_{GS} dependence between Off-mode and V_{Gmax} was studied revealing HC injection efficiency that enables new sensitive criteria to prevent from HBD events. Degradation in short-channel transistors can occur in Off mode and under subthreshold conditions due to impact-ionization (II) and non-conducting HC where this latter is related to different leakage current components as surface band-to-band tunneling (BTBT) and gate-induced drain leakage (GIDL).

Usually, BD under Off mode is modeled by TDDB in accumulation in the overlap region due to creation of excessive damage to oxide integrity. This is indeed a relevant failure mode that enables to stress device symmetrically using both source and drain overlap or using voltage splitting technique **[14-15]**. However, in this paper the competing Off-state TDDB is induced by HC mainly for ultra-short channel transistors, depending highly on channel-length L_G and I_{DS} current. This becomes subsequently challenging for middle-of-the-line (MOL) dielectrics reliability. Not only poly to contact BD can reduce the intrinsic reliability margin, but it can also be the origin of extrinsic failures due to slight control of poly to contact space. Therefore, it's important to build accurate model to optimize design rules of high voltage applications at which spacer dielectrics are submitted. A dedicated Off-state HBD model and location analysis is presented for first time. It is critical to determine the sensitivity to Off-state TDDB and deeply understand the wear out mechanisms at device level, as the dielectric HBD strongly depends on spot position that we determined along the channel-length direction. **Figs.1a,b** summarize the observation about BD path location from On and Off modes analyzed from literature and our previous experiments **[6]**. Therefore, several BD scenarios have been considered to occur inside oxide (at center or edge), between drain and bulk junction or finally in the spacer region between gate and drain.

After the description of experimental setup and devices used in this work in Section II, we present a dedicated gate-oxide breakdown study under Off-state TDDB in Section III, in comparison to On-state and MOL BD. Then, we propose in Section IV a TDDB modelling under Off mode stressing based on measurement of the initial leakage currents.

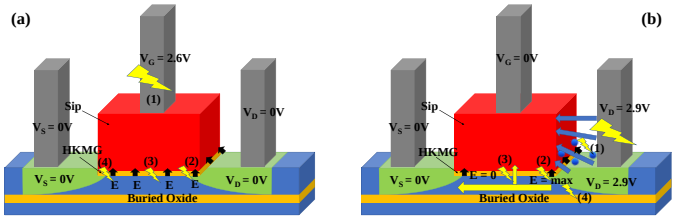


Figure 1. Schematic device representations under TDDB stress without serial protection resistances showing main location of breakdown regions. Gate and drain contacts failure are due to significant power dissipation. **(a)** On-state BD occurs simultaneously in gate contact (1) and different regions of gate-dielectric (2- nearby drain, 3- in channel or 4- nearby source). **(b)** Under Off-state, BD occurs simultaneously in drain contact (1), in dielectric (2- drain side or 3- middle of channel) or between drain and BOX insulator due to high impact-ionization.

II. Experimental Description

TDDB is evaluated in 28nm FDSOI N-FET devices fabricated with HKMG (EOT = 1.5nm) and different gate channel length L_G (30nm, 34nm, 40nm, 46nm) issued from STMicroelectronics CMOS SOI technologies. Samples are submitted to Constant Voltage Stress (CVS) applied either on drain-side for Off-state and gate-side for On-state and MOL, between 125°C and 25°C while other terminals were grounded. Poly to contact BD is measured on structures landing on STI **Fig.2** rather than CMOS structure for which gate dielectric BD would occur before spacer BD **[16]**. For the purpose of this paper, TDDB was performed on all devices with V_{DS} = 2.9V for Off-state, V_{GS} = 2.6V for On-state, and very high voltage for MOL BD (up to 20V). An 1kΩ external series resistance was connected to devices in **Fig.3** to limit power dissipation in drain/gate contact and to guarantee a stable and reproductible post-breakdown I-V characteristics. The voltage drop over serial protection resistance was corrected for all devices with (**1a)** and **(1b**) in order to mimic TDDB stress condition without any external resistance. The experiment methodology consists in the following successive steps: 1) initial current-voltage I-V characterization to obtain fresh device current and eliminate early failures probability (**Fig.4**), 2) TDDB stress with or without external series resistance as shown respectively in **Figs. 5,6** and **3**) final post TDDB stress I-V characterization (**Figs.7** and **8**) for BD path location and resistance estimation. The experimental results will be discussed in Sections III and IV.

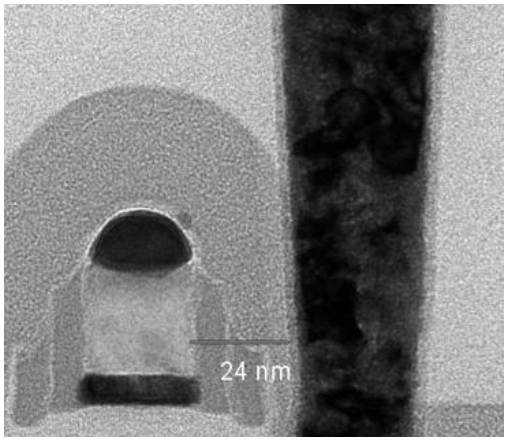


Figure 2. Transmission Electron Microscopy (TEM) cross section of poly to contact test structure on STI used for spacer breakdown.

$$V_{DR_{D-series}} = V_D - R_{D-series} \cdot I_D \qquad (1a)$$

$$V_{GR_{G-series}} = V_G - R_{G-series} \cdot I_G \qquad (1b)$$

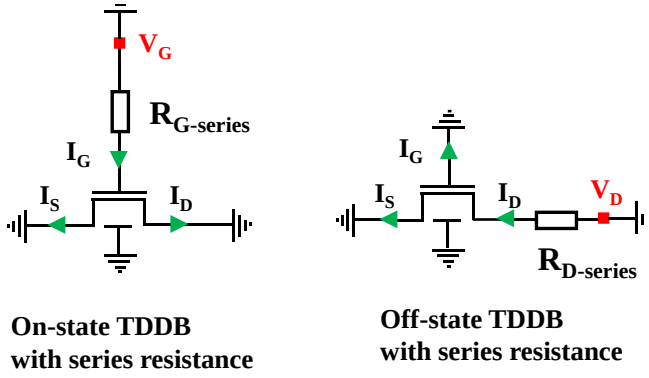


Figure 3. Measurement set-up of TDDB stress illustration with external protection series resistors. The voltage drop due to resistances has to be compensated with respect to drain **(1a)**, and gate currents **(1b)**.

This paper is organized as follows, first, MOL and dielectric BD mode and location were investigated on more than 700 transistors, using current-ratio technique **[17-18]** and comparing voltage acceleration factor (VAF). Then, Off-state TDDB dependence is analyzed under DC stress with variation of V_{DS}, L_G and temperature on several dies and plotted as min and max HBD time values (T_{BD}). Finally, the dielectric BD is modeled as a function of non-uniform vertical electrical field component E_{max} and the leakage currents induced by the accelerating stressing drain bias (V_{DS}).

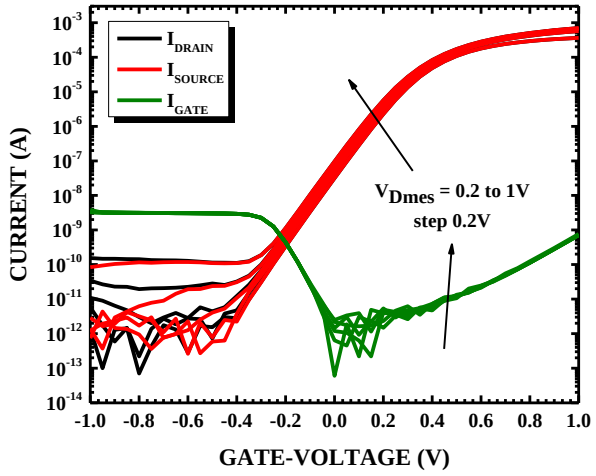


Figure 4. Fresh I-V characteristics obtained in three terminals transistor (28nm FDSOI N-FETs with W_G = 1µm and L_G = 30nm). Drain (black lines) and source (red lines) currents are similar and overlapping before dielectric breakdown. Gate saturating current in Off-mode results from dielectric leakage and mostly from MOS protection diode.

III. BREAKDOWN POSITION DETERMINATION

A. Device characterization before and after BD

CVS are commonly used to monitor T_{BD} dependencies and to build up the complete TDDB distribution functions by using different stress voltages and device areas. For this purpose, the recent investigations on Off-state BD mode **[6]** are further extended to determine the location of HBD under CVS in thin gate-oxide (GO1) FDSOI N-FET with L_G defined from 30 to 46 nm.

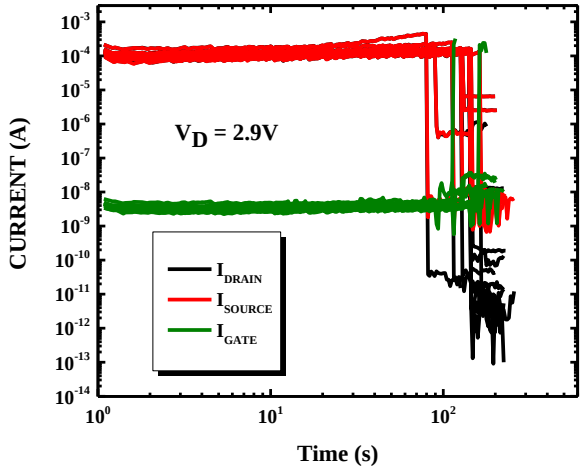


Figure 5. Off-state leakage currents until HBD in FDSOI N-FET W_G/L_G = 1µm/30nm as function of cumulative stress time in configuration without external series resistance. This generates an open circuit. Source (red lines) and drain (black lines) currents are overlapping.

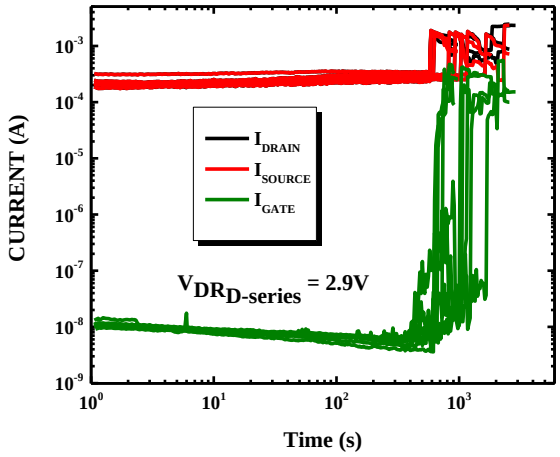


Figure 6. Off TDDB leakage currents until BD with connected series protection resistor. Voltage drop has been compensated to reproduce the same stress condition as **Fig.5**. Drain (black lines) and source (red lines) currents are overlapping.

Fig.4 shows dielectric integrity test by measuring gate, drain and source currents on fresh device without any series resistance in the range V_{GS} = -1V to 1V and V_{DS} = 0.2V up to 1V. TDDB without external series resistance causes an open circuit and a dysfunctional device since it exhibits an abrupt downwards jump of currents as observed under Off-state stress on current versus time curves in **Fig.5** on drain and source side. After BD the series resistance was removed, gate, drain and source currents were measured in the range V_{GS} = -1V to 1V and V_{DS} = 0V to 1V (**Figs.7-8**). The post-breakdown behavior of an open circuit on drain side is shown in **Fig.7** with very low noisy drain current due to the melting of drain contact. By adding a protection series resistance, the devices remain functional despite dielectric BD (**Figs.6** and **8**).

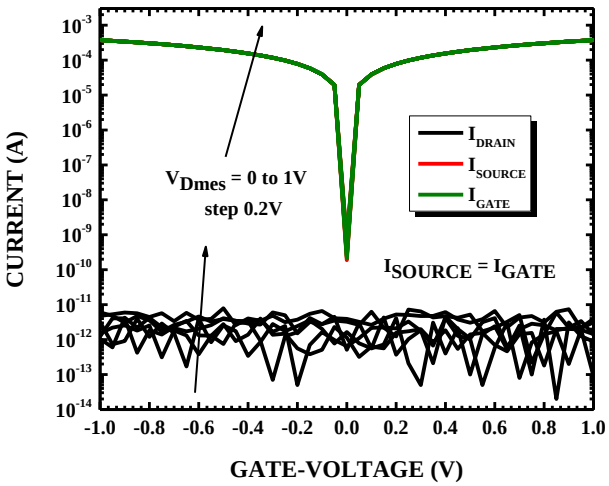


Figure 7. Three terminals transistor I-V characteristics after Off-state TDDB without protection resistor in **Fig.5**. A very low noisy current is measured on drain terminal. Gate (green lines) and source (red lines) currents are overlapping.

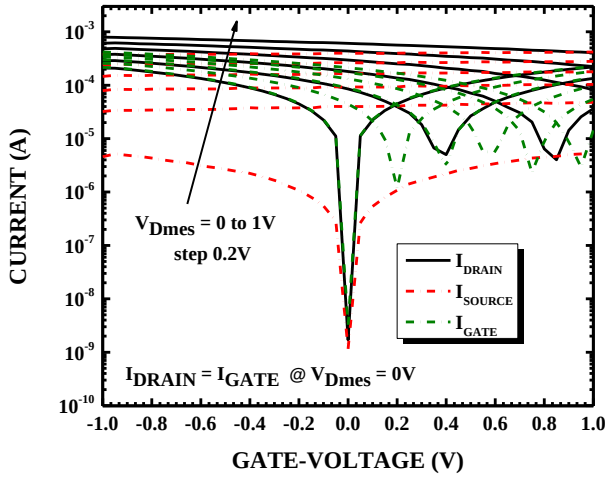


Figure 8. I-V characteristics after Off-state TDDB with external series resistance in **Fig.6**. Devices are still functional after BD.

B. Location of breakdown spot

HBD nature quantification methodology consists in the measurement of post-breakdown gate resistance R_{Gate} for positive gate voltage V_G = 1V **(2)**. HBD spot position can be precisely obtained with ratio ***s*** **(3)** (**Figs.9-10**) at negative gate bias V_G = -1V **[17-21]**. Under these conditions, electrons are

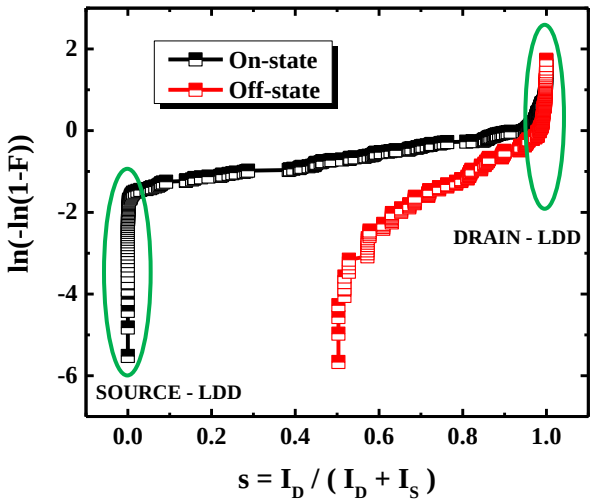


Figure 9. Weibit distribution plots for sorted ratio ***s*** showing multi-modal behavior of BD in LDD diffusion (vertical) and channel (central) region.

$$R_{Gate} = \frac{V_G}{I_G} \quad (2)$$

$$s = \frac{I_D}{I_D + I_S} = \frac{x_{BD}}{L_G} \quad (3)$$

injected from the gate through the BD path and collected to the source when ratio ***s*** is close to 0, otherwise to the drain when ratio ***s*** is close to 1. ***s*** values obtained in On-mode (black plot in **Fig.9**) which are relating a linear BD spot position in the channel, outside of the lightly doped-drain (LDD) regions, are approximatively equidistant and equiprobable (**Fig.10**).

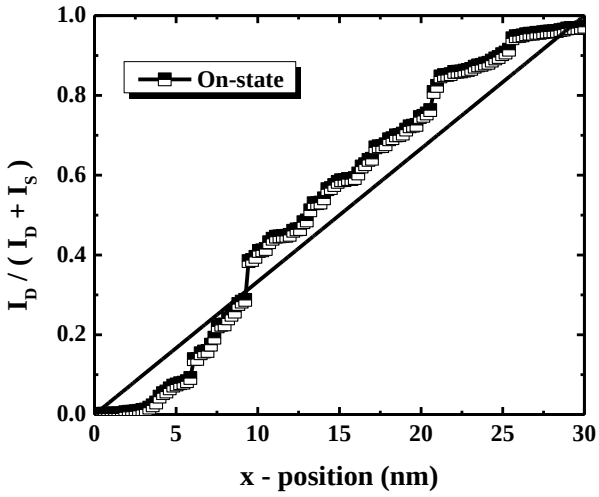


Figure 10. On-state gate-oxide BD spot position sorted according to ratio **s** showing a linear relationship between ***s*** and BD location distributed equidistantly.

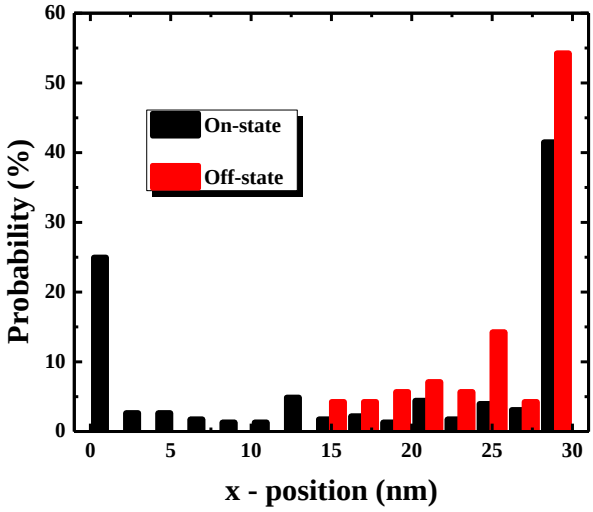


Figure 11. BD spot positions classified by regions of BD occurrence in the 30nm gate-length transistor. Higher BD probability is obtained for LDD regions.

Therefore, the current partitioning method can also be applicable to Off-mode BD. **Fig.10** demonstrates the proportional relationship between ***s*** ratio and BD spot position x_{BD}, determined by sorting the ***s*** values obtained on a sufficiently large number of tested devices (**Fig.9**). For On-state TDDB, HBD is observed to occur close to source/drain extension while soft breakdown (SBD) is observed from the channel region (**Figs.11-12**). Under Off-state, only HBD is distinguished in **Figs.11-12** from the middle of the channel until drain extension. The higher breakdown probability observed in LDD regions (**Fig.11**) can be explained by electric

field non uniformity related to charges in spacers (significant on drain side) and channel depolarization due to oxide leakage. The distribution of R_{Gate} is plotted in **Fig.13** where HBD path resistance is below 3.5MΩ and the soft one above this value.

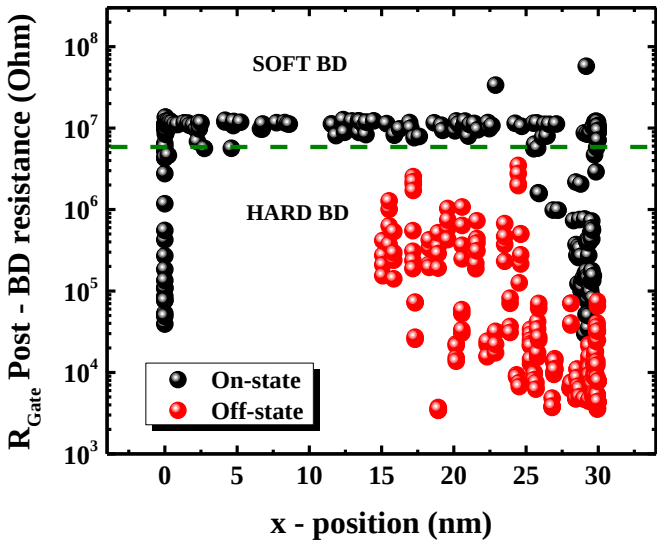


Figure 12. Breakdown path resistance plotted as a function of position along the channel. Hard breakdown is exclusively identified for Off-state TDDB.

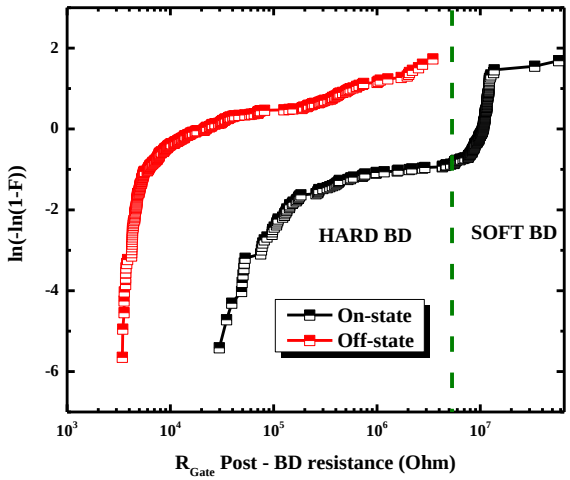


Figure 13. R_{GATE} distribution plot for Off-mode and On- mode TDDB showing multi-modal behaviors between hard BD and soft BD.

C. Breakdown statistics

Weibull distributions for TDDB under On and Off modes are plotted in **Fig.14** showing no sensitivity to the external series resistance. Processes were simulated thanks to Sentaurus Process tool **[22]**. The electrical outputs are computed by solving the Poisson equation and current continuity equations coupled with drift-diffusion transport model in Sentaurus Device module **[23]**. Impact-ionization coefficients are calculated from Chynoweth law **[24-25]**. Off-state TDDB simulations result in higher impact-ionization generation close to drain (**Fig.15.a**) induced by a stronger lateral electric field with a peak value at gate to drain edge and spacer (**Fig.15.b**). TDDB slope value can be related to $Si/SiO_2/HfO_2$ gate stack,

$$\boldsymbol{\beta} = \frac{\boldsymbol{n}\,.\,(\boldsymbol{T_{HK}} + \boldsymbol{T_{IL}})}{\boldsymbol{a_0}} \qquad (4)$$

with $\boldsymbol{n}$ the T_{BD} time exponent, T_{HK} is high-K thickness, T_{IL} is the interface layer thickness with defect cell size as:

$$\boldsymbol{a_{0-On} > a_{0-Off}} \qquad (5)$$

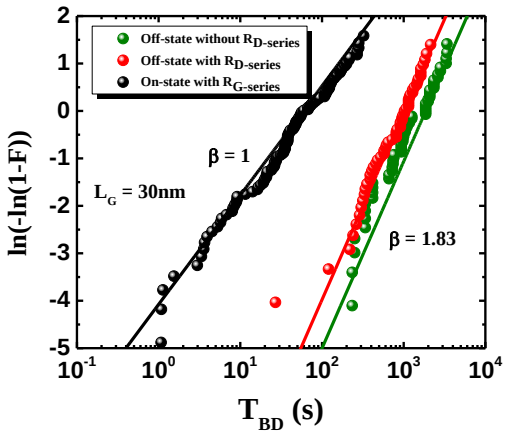


Figure 14. Comparative cumulative distribution plots for GO1 W_G/L_G = 1µm/30nm 28 FDSOI N-FETs with lower Weibull slope obtained for On-state TDDB. External series resistance has no effect on β.

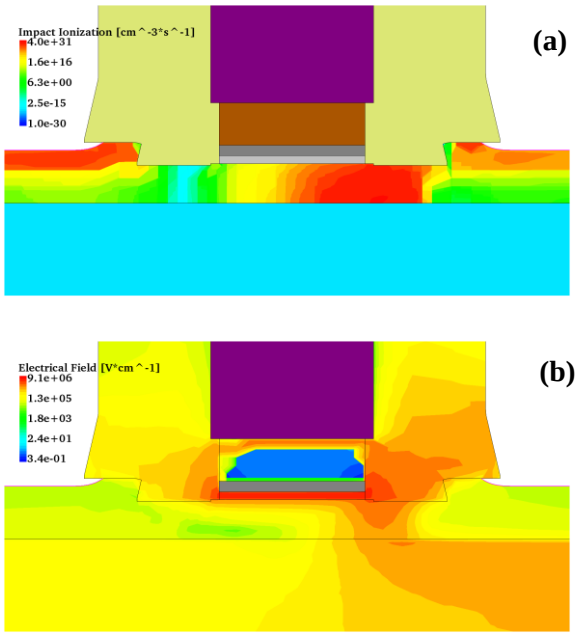


Figure 15. TCAD simulations during Off-state TDDB on N-Fet device in logarithmic scale. (a) Impact ionization showing its peak value at drain junction. (b) Electical field profile in channel, $Si/SiO_2/HfO_2/TiN$ gate stack and the regions around.

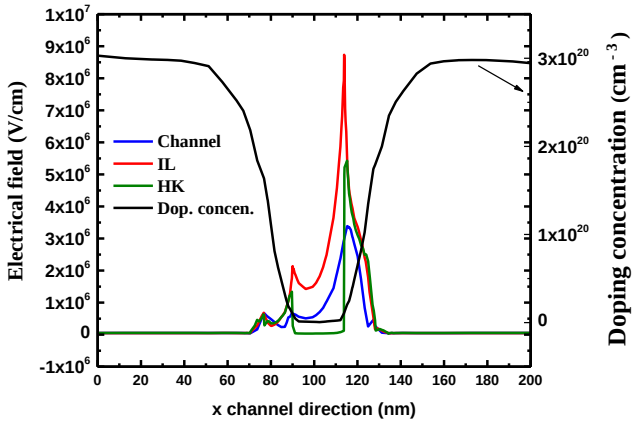


Figure 16. Lateral profile of electrical field during Off-state TDDB in channel, interface layer and high-K showing located peak values into gate to drain edge with higher damage generation rate in IL and HK than into the channel.

Gate stack is the most sensitive region to failure under Off- and On modes with a higher generation rate and electric field into the interface layer (IL) and high-K (HK) [26] as shown in **Fig.16**. Thus, a bimodal distribution behavior may be observed and different β values could be extracted from IL and high-K, respectively [27]. We show that β slope is found larger under Off-state TDDB (**Fig.14**) compared to the one expected from standard percolation model under On-state. This higher β value in **(4)** can be explained by different defect cell size a_o [28] with **(5)** [29]. This might be explained by the effect of a longer percolation path from the gate-drain region [30] and distinct oxide defects (Si-O) than interface traps (Si-H as P_b0) [4]. This possibly suggests **Figs.17a,b** that the generated defects under Off mode are tinier and induce longer percolation paths.

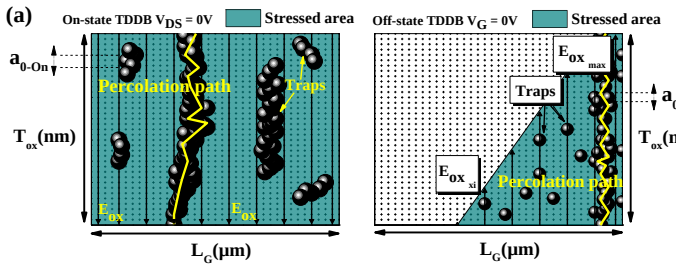


Figure 17. Schematic illustration of BD triggering through percolation paths showing defect generation into dielectric with On-state TDDB cell size $a_{0\text{-}On}$ larger than Off mode one $a_{0\text{-}Off}$. **(a)** On-state TDDB uniform stress and **(b)** Off-state non-uniform stress.

Fig.18 compares the voltage acceleration factor (VAF) corresponding to MOL dielectric BD and gate-oxide BD (T_{BD} at 63%) characterized under On- and Off- state TDDB. The results differ significantly as a function of stress voltage. As matter of fact, MOL TDDB follows a square-root VAF dependence, while On-state TDDB follows a gate-voltage power law. Therefore, it indicates that BD mechanism under Off-state does not correspond to spacer BD but rather to gate-oxide dielectric breakdown at the drain- edge.

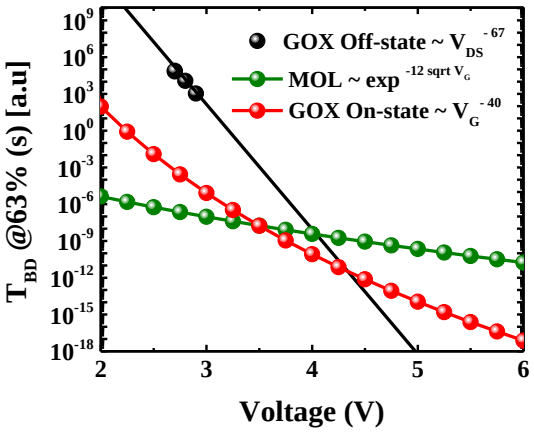


Figure 18. Average T_{BD} at 63% comparison between gate oxide TDDB stress under Off, On modes and middle of line for FDSOI N-FET L_G = 30nm. Voltage acceleration factor VAF obtained under Off-state is different from the spacer dielectric VAF. Off-state T_{BD} voltage range is extremely tight. MOL and On-state T_{BD} data are projected.

IV. Off-mode T_{BD} modelling from E_{LAT} to $IG_{OFF}(T_0)$

To investigate the potential role of hot-carrier injection under Off-state BD, we independently modelled TDDB in (6)-(7) as a function of V_{DS}, L_G and temperature in **Figs.19** and **Figs.20a-c**. We show that T_{BD} increases with L_G (**Fig.19**) without changing markedly β, VAF (**Fig.20.a**), and gate-length acceleration factors (LAF) (**Fig.20.b**). We further extracted temperature activation E_a (**Fig.20.c**) which is used in (6)-(7):

$$T_{BD} = A \,.\, L_G^{LAF} \,.\, V_D^{-VAF} \,.\, \frac{1}{W_G}^{\frac{1}{\beta}} \,.\, e^{\left(\frac{\ln(-\ln(1-F))}{\beta}\right)} \,.\, e^{\left(\frac{E_a}{KT}\right)} \quad \textbf{(6)}$$

$$T_{BD63\%} = B \,.\, I_{g,Off}^{\ p} \,.\, exp^{\left(\frac{Ea}{KT}\right)} \quad (7)$$

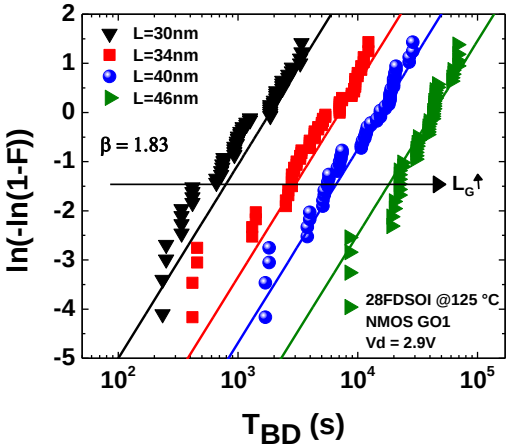


Figure 19. TDDB time to failure distribution for various L_G = 30 to 46nm from FDSOI N-FETs (W_G = 1µm) at fixed drain voltage V_{DS}=2.9V. Breakdown occurs later for longer devices.

From experimental data, VAF and LAF are found to follow different dynamics. The strong effects of L_G and V_{DS} (**Figs.19-**

20) suggest that Off-state TDDB damage is highly correlated to carrier energy and the amount of injected HC into the gate-oxide induced by impact-ionization from the drain junction. Plotting the results as a function of the average lateral field is given in **Figs.21.a.** A simplified peak value $E_{max} \cong V_{DS}/L_G$ at the gate-drain edge does not give satisfactory results, due to L_G and temperature dependencies, since curves are shifted for devices with various L_G stressed at equivalent electric field. Under On-state stressing, charge trapping and scatterings lead to band diagram deformation modifying the electrical field profile which becomes non-uniform while the currents remain roughly

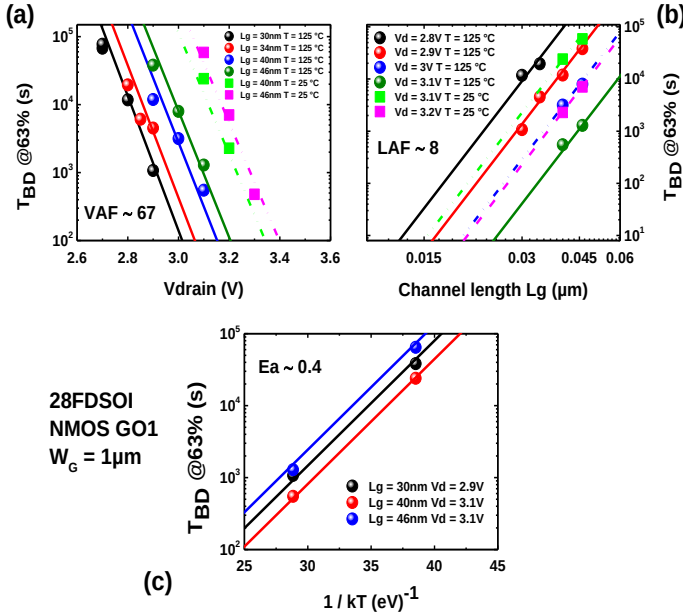


Figure 20. T_{BD} time to failure acceleration factors extracted for GO1 28nm FDSOI under Off-state stressing at 125°C (solid lines) and 25°C (dash line). **(a)** T_{BD} obtained at 63% *vs.* drain voltage V_{DS} with various gate-length L_G. **(b)** T_{BD} plotted at 63% *vs.* L_G with various V_{DS}. **(c)** Temperature dependence gives small thermal activation. Common VAF **(a)**, LAF **(b)** and E_a **(c)** are obtained independently to L_G and stressing drain bias V_{DS}.

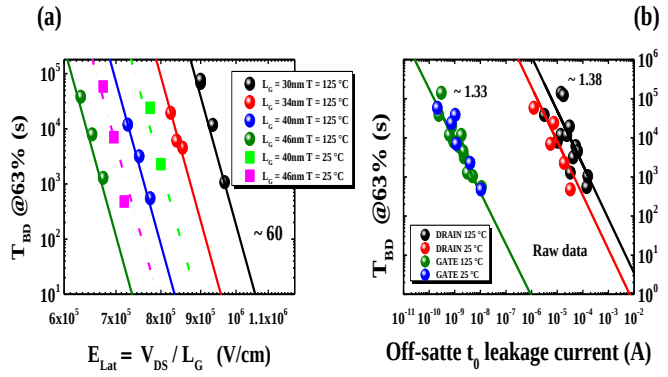


Figure 21. Lifetime plots as T_{BD} at 63% for 28nm N-FET **(a)** *vs.* electrical field Emax $\cong V_{DS}/L_G$ enlightening L_G dependence between 25°C (dash lines) and 125°C (solid lines) and **(b)** *vs.* drain and gate oxide initial leakage current overcoming L_G dependence between 25°C and 125°C. This shows better lifetime monitoring using gate leakage and slightly more dispersion on drain side in 28nm N-FETs.

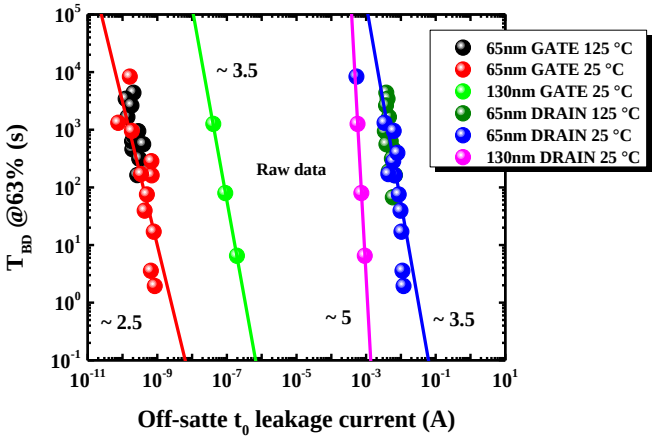
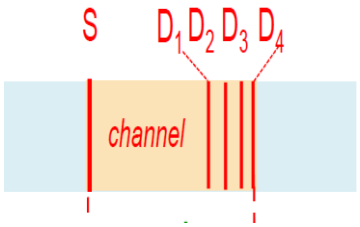


Figure 22. T_{BD} at 63% lifetime model as a function of initial (t_0) leakage current in 65nm and 130nm N-FETs gate current and drain current monitors between 25°C and 125°C.

constant (**Fig. 17.a**). Under Off-state, the electrical field is far less uniform (**Fig.16**, **Fig. 17.b**). Hence TDDB results are analyzed as a function of drain leakage current $I_{D,Off}(V_{GS}= 0)$ corresponding to the bias point of $I_{g,Off}$ **[6]**. We found in **Fig.21.b** with **(7)** that T_{BD} results for various V_{DS}, L_G and temperature lie on the same dependence with initial gate current $I_{G,Off}$ (t_o) with p= -1.3, for same level of drain leakage current. The same trend and co-modality are shown in **Fig.22** for different technologies (65nm and 130nm CMOS nodes). Longer devices are exposed to reduced electric field into the channel **Fig.23** and $Si/SiO_2/HfO_2$ stack at a fixed (half) position during Off-state TDDB. This explains the difference in T_{BD} results observed for various channel length in **Fig.19** and **Fig.21b.** Indeed, in the existing literature only few investigations are given on the dependencies between Off-state effective electric field and current with V_{DS} and L_G. Thus, in our previous work we modelled the Off current characteristics **[6]**, similarly to a diode-like framework. We believe that leakage Off currents at drain and gate sides represent relevant figure of merits for HC injection and nonconducting HC under Off-state stressing. Leakage can be used as a main monitor for BD characterization and put in a global framework for Off-state T_{BD} modelling. Due to the straight correlation between TDDB and initial leakage current I_0, this brings benefits for a fast reliability monitoring of process robustness against HBD, since initial leakage currents can be easily implemented with measurement tools.



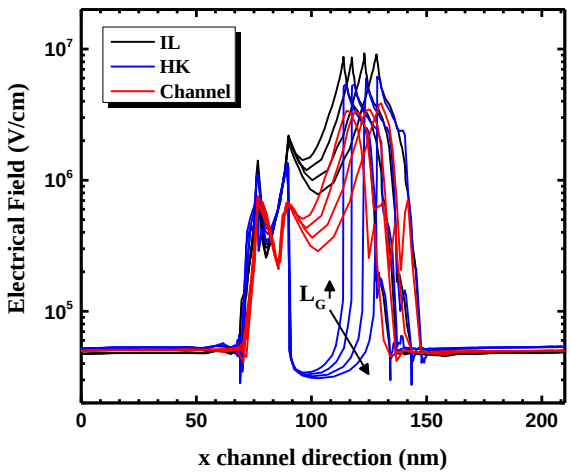


Figure 23. Lateral profile of electrical field during Off-state TDDB in channel, interface layer and high-K for different gate channel length L_G (30nm, 34nm, 40nm, 46nm). Average electrical field is higher for shorter device although the peak value at drain edge is approximately the same for all devices.

V. CONCLUSION

Breakdown location during Off-state TDDB degradation in HKMG 28nm FDSOI was studied in detail for relevant conditions related to RF millimeter wave applications. We demonstrated the importance of the localized BD events from the middle of the channel to the gate-drain edge in HKMG 28nm FDSOI node where the role of non-conducting HC has been clearly evidenced. A compact device lifetime model based on leakage currents $I_{G,Off}$ (or $I_{D,Off}$) power-laws in a diode-like framework has been successfully applied. It simultaneously accounts for drain bias V_{DS}, channel length L_G and temperature dependencies in comparison to the peak lateral field E_{max} modelling.

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