

# On Path Memory in List Successive Cancellation Decoder of Polar Codes

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**Abstract**—Polar code is a breakthrough in coding theory. Using list successive cancellation decoding with large list size  $\mathcal{L}$ , polar codes can achieve excellent error correction performance. The  $\mathcal{L}$  partial decoded vectors are stored in the path memory and updated according to the results of list management. In the state-of-the-art designs, the memories are implemented with registers and a large crossbar is used for copying the partial decoded vectors from one block of memory to another during the update. The architectures are quite area-costly when the code length and list size are large. To solve this problem, we propose two optimization schemes for the path memory in this work. First, a folded path memory architecture is presented to reduce the area cost. Second, we show a scheme that the path memory can be totally removed from the architecture. Experimental results show that these schemes effectively reduce the area of path memory.

**Index Terms**—Polar codes, List successive cancellation decoding, Path memory, Partial-sums

## I. INTRODUCTION

Polar codes [1] are the first kind of forward error correction code that is proved to achieve channel capacity. The basic decoding scheme of polar codes is called successive cancellation decoding (SCD) [1]. The decoding is sequential in nature as the decoding of a new bit has dependency on the already decoded bits. Specifically, the data dependency comes from the partial-sums which are obtained by encoding some of the already decoded bits. These partial-sums are used as the inputs of the subsequent computations. List successive cancellation decoding (LSCD), proposed in [2], includes  $\mathcal{L}$  parallelly-decoded SCDs and keeps  $\mathcal{L}$  partial decoded vectors during decoding. By using a large list size and selecting a decoded vector satisfying the cyclic redundancy check (CRC) [3], [4] at the end of decoding, the error correction performance of polar codes is greatly improved.

The hardware architecture of LSCD [5]–[10] implements  $\mathcal{L}$  SCD kernels to support the parallel calculations of  $\mathcal{L}$  paths, indicating the hardware complexity is at least  $\mathcal{L}$  times that of the single SCD. To achieve a moderate hardware complexity, the semi-parallel architecture [11] and the folded partial-sum network (PSN) [12] originally proposed for a single SCD are also adopted in the LSCD architecture [5]–[9] due to their low complexity. Several  $\mathcal{L} \times \mathcal{L}$  crossbars are used for the permutations of log-likelihood ratios (LLRs), partial-sums and partial decoded vectors among different memories according to the results of list management. In [5], pointers are used to access the corresponding LLRs for computation instead of directly copying the LLRs during update.

The path memory with  $\mathcal{L} \cdot N$  memory bits is implemented to store the  $\mathcal{L}$  partial decoded vectors in the existing LSCD architecture [5]–[7]. It updates the contents when a new bit is decoded. The partial decoded vector of a path is duplicated if both its expanded paths are kept. After this duplication, an  $N$ -bit crossbar is needed for the permutation of the updated partial decoded vectors, which has a very high complexity and takes a large area when the code length and list size are large. Moreover, the path memory needs to be implemented with registers which usually have a larger area than SRAMs.

In this work, to optimize the complexity of the path memory, we first propose a folded path memory by mimicking the architecture of the folded PSN. Then we present a method to recover the decoded bits from the partial-sums which are already available in the folded PSN and hence the path memory can be omitted. It is shown that the latency of this recovery can be hidden in the decoding process, therefore will not cause any latency overhead in most conditions.

*Notation:* In this paper, matrices and row vectors are denoted in boldface uppercase and lowercase letters, respectively.  $\mathbf{X}_M$  represents a square matrix of order  $M$  and  $\mathbf{x}_M$  represents an  $M$ -dimensional vector.  $x_i$  is the  $i^{\text{th}}$  element of a vector  $\mathbf{x}$ .

## II. MISCELLANEOUS

### A. Introduction of Polar Codes

Polar codes [1] are a kind of linear block codes whose code length is denoted as  $N$ . Its generator matrix is Kronecker matrix  $\mathbf{F}^{\otimes n}$ , where  $\mathbf{F} = \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix}$  and  $n = \log_2 N$ . A codeword  $\mathbf{x}_N$  can be encoded from a source word  $\mathbf{u}_N$  by  $\mathbf{x}_N = \mathbf{u}_N \cdot \mathbf{F}^{\otimes n}$ , where  $\mathbf{u}_N, \mathbf{x}_N \in \{0, 1\}^N$ . Figure 1(a) shows an encoding signal flow graph of  $\mathbf{F}^{\otimes 3}$  in which each “ $\oplus$ ” node executes an XOR operation and each “.” node split its input.

LSCD of polar codes can be represented by a scheduling tree shown in Figure 1(b). It includes two parts. The upper half is a full binary tree with  $n+1$  stages, representing  $\mathcal{L}$  identical SCDs for  $\mathcal{L}$  paths. The stage indices are in descending order from the root to the leaf nodes. Two kinds of nodes, denoted as F-nodes and G-nodes, exist in this tree. The number of functions executed in each node is also marked in Figure 1(b). The functions in G-nodes depend on the partial-sums which are encoded from the already decoded bits. Specifically, the partial-sums for the  $j^{\text{th}}$  node from the left on stage  $\lambda$  are calculated as

$$[\hat{s}_{(j-1)\cdot\lambda}^\lambda, \dots, \hat{s}_{j\cdot\lambda-1}^\lambda] = [\hat{u}_{(j-1)\cdot\lambda}, \dots, \hat{u}_{j\cdot\lambda-1}] \cdot \mathbf{F}^{\otimes \lambda}, \quad (1)$$

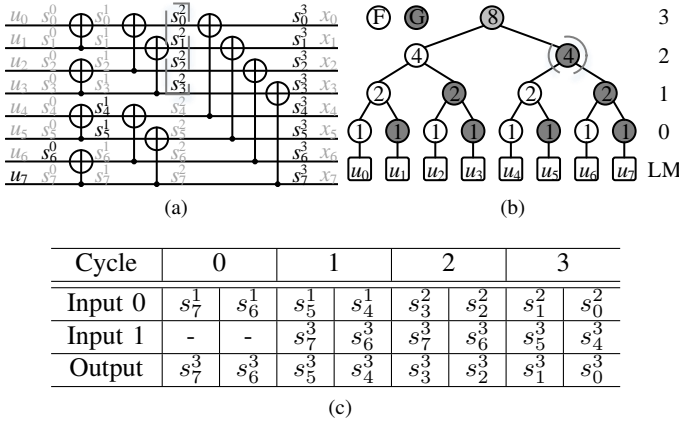


Figure 1. (a) Encoding signal flow graph and (b) LSCD scheduling tree of polar codes and (c) the steps of partial-sum update in a folded PSN ( $\Lambda = 8$  and  $P = 2$ ).

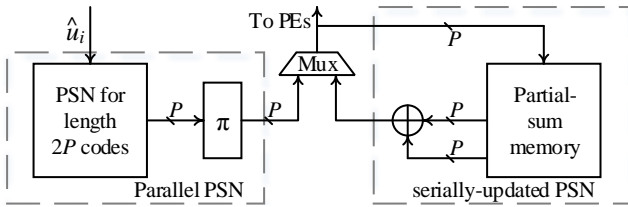


Figure 2. The block diagram of folded partial-sum network.

where stage index  $\lambda \in [0, n-1]$  and  $j \in [0, 2^{n-\lambda}-1]$ ,  $\Lambda = 2^\lambda$  is the bit width of partial-sums at stage  $\lambda$  and  $\hat{u}$  and  $\hat{s}$  are the decoded bits and partial-sums, respectively<sup>1</sup>. For example, the G-node at stage 2 ( $j = 1$ ) in Figure 1(b) needs the partial-sums generated from  $[\hat{u}_0, \dots, \hat{u}_3]$  in Figure 1(a).

The source bits are decoded in an ascending order. At each leaf node, a source bit is decoded. For each path in LSCD, either possibility that the decoded bit is 0 or 1 is considered and the number of paths is doubled. If the number of paths exceeds the list size  $\mathcal{L}$ , list management operations, denoted by the squares in the scheduling tree, are executed to keep the best  $\mathcal{L}$  decoding paths in the list and discard the others.

### B. Folded Partial-sum Network

In SCD,  $2^\lambda$  F- or G-functions can be calculated in parallel at stage  $\lambda$ , so  $\frac{N}{2}$  processing elements (each is used to calculate one function) should be implemented if we want to maximize the parallelism. However, the area cost will be very high. To reduce the hardware complexity, semi-parallel architecture [11] was proposed to limit the computational parallelism to  $P = 2^p (\ll N)$ , i.e., at most  $P$  functions are calculated in one clock cycle and a node is calculated in  $\lceil 2^{\lambda-p} \rceil$  clock cycles. The complexity of PSN in this kind of semi-parallel architecture can also be reduced. In [12], an folded PSN architecture is proposed, which generates at most  $P$  partial-sum bits in one clock cycle. Its block diagram is shown in Figure 2. The partial-sums for the nodes at stages not higher than  $p$  are updated by a parallel PSN and stored in a  $P$ -bit

<sup>1</sup>For simplicity, the hats in  $\hat{u}$  and  $\hat{s}$  are omitted in the rest of this paper

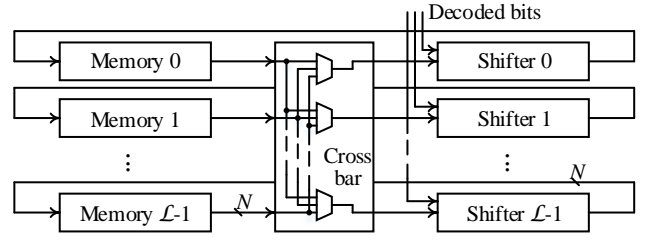


Figure 3. The block diagram of the traditional path memory.

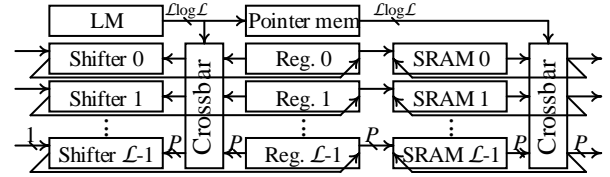


Figure 4. The block diagram of the proposed folded path memory.

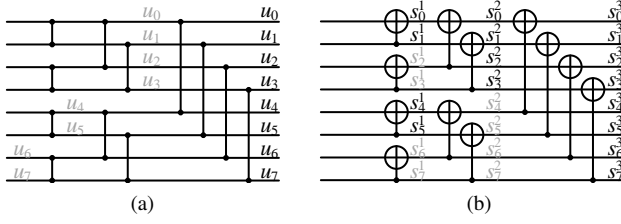
register bank. The partial-sums at higher stages are serially updated in a word of  $P$  bits and stored in an  $\frac{N}{2}$ -bit SRAM. The encoding signal flow graph in Figure 1(a) can be used to illustrate how to generate  $\Lambda = 8$  bits of partial-sums for G-node at stage 3. Supposing that the parallelism  $P = 2$ , the partial-sums already generated are  $\{[s_0^2, s_1^2, s_2^2, s_3^2], [s_4^1, s_5^1], s_6^0\}$  and the newly decoded bits is  $u_7$ . First,  $[s_6^1, s_7^1]$  are parallelly updated from  $s_6^0$  and  $u_7$ . Then, the required partial-sums  $[s_3^3, \dots, s_7^3]$  are generated according to the schedule shown in Figure 1(c) within 4 clock cycles. According to the synthesis results in [12], the folded PSN has a much smaller area than other fully-parallel PSN architecture, such as the partial-sum update logic [11] and the feed forward architecture [13].

### C. Problems of the Existing Path Memory

The block diagram of the traditional path memory architecture for LSCD [5]–[7] is shown in Figure 3.  $\mathcal{L}$  blocks of memories are implemented to store the partial decoded vectors of  $\mathcal{L}$  paths. Each memory includes  $N$  bits of registers. After the list management operation is executed, some paths are pruned while other paths are kept and duplicated, and the contents in the path memory are updated. First, the crossbar permutes the paths according to the list management results. Then the newly decoded bit of each path is appended to the corresponding permuted partial decoded vector by a shifter. Finally, the updated paths are stored in the path memory. According to the synthesis results, the crossbar used in this architecture, which has a quadratic complexity with respect to the list size, takes a very large area when large code length and list size are used and this becomes a significant issue of the existing architecture. The registers also take a large area and are expected to be substituted with other hardware-friendly memory elements.

## III. FOLDED PATH MEMORY

As discussed in Section II-C, in the traditional path memory, the area overhead is mainly due to the  $N$ -bit crossbar when the list size is large. Consequently, the key to reduce the complexity of the path memory is to reduce the crossbar size.



Cycle	0	1	2	3
Input 0	$s_0^3$	$s_1^3$	$s_2^3$	$s_3^3$
Input 1	$s_4^3$	$s_5^3$	$s_6^3$	$s_7^3$
" $\oplus$ "	$s_0^2$	$s_1^2$	$s_2^2$	$s_3^2$
"."	$s_4^2$	$s_5^2$	$s_6^2$	$s_7^2$

(c)

Figure 5. The signal flow graph of (a) folded path memory and (b) decoded bits recovery and (c) the recovery schedule ( $\Lambda = 8$  and  $P = 2$ ).

As presented in Section II-B, the folded PSN updates at most  $P$  partial-sum bits in one clock cycle. If this architecture is used in an LSCD, the crossbar size is only  $P$  bits, which is much smaller than that of the  $N$ -bit crossbar in a parallel path memory. According to Section II-B, the partial-sums and decoded bits have the same bit width and are always updated at the same time during the decoding. Based on these observations, we propose an architecture called folded path memory which mimics the architecture of the folded PSN, as shown in Figure 4.

The left part of the folded path memory includes  $\mathcal{L}$   $P$ -bit register banks,  $\mathcal{L}$  shifters and a  $P$ -bit crossbar. After the list management operation, the crossbar read the  $P$ -bit partial decoded vectors from the register banks and update them in the same way as the parallel path memory shown in Figure 3. When each register bank in the left part is full with  $P$  bits, these bits are sent to the right part.

The right part uses  $\mathcal{L}$  blocks of SRAMs to store the partial decoded vectors. The port width of each SRAM is  $P$  bits and its total size equals to  $N$  bits. The stored vectors are not permuted for update. Instead, we can use  $\frac{N}{P}$  pointers to store the block indices of the SRAM in which each  $P$  bits are stored. However, to update the pointers, we still need extra hardware. To use as few pointers as possible, we still use a crossbar to permute the decoded bits which have the same indices with the partial-sums that are being updated. Take an example with  $\Lambda = 8$  and  $P = 2$ , whose signal flow graph shown in Figure 5(a) can be obtained by changing the " $\oplus$ " nodes in Figure 1(a) to "." nodes. During the four clock cycles when the partial-sums at stage 3,  $[s_0^3, \dots, s_7^3]$ , are generated, the corresponding  $[u_0, \dots, u_3]$ ,  $[u_4, u_5]$  and  $[u_6, u_7]$  of this path but previously stored in different blocks of memories are permuted through the crossbar and stored in the SRAM of this path in these four cycles. By doing so,  $[u_0, \dots, u_7]$  of each path can be pointed by a pointer instead of three pointers. For a polar code with code length equal to  $N$ , the partial decoded bits are store in  $n - p + 1$  groups with their length  $\Lambda \in \{\frac{N}{2}, \frac{N}{4}, \dots, 2P, P, P\}$ . This means only  $n - p + 1$  pointers are enough for each path.

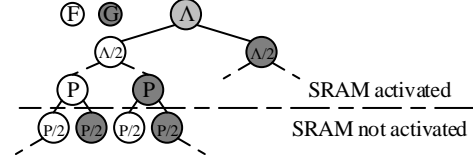


Figure 6. The scheduling tree of recovering the decoded bits.

Finally, as the two crossbars are never activated simultaneously, only one crossbar is implemented in the final architecture. Comparing with the existing architectures, the folded path memory uses a much smaller crossbar while it is adaptive to LSCD with any code length and list size and also easy to implement.

#### IV. RECOVERING DECODED BITS FROM PARTIAL-SUMS

In this section, based on the fact that the partial-sums are encoded from the decoded bits, we introduce a scheme to directly recover the decoded bits from the partial-sums stored in a folded PSN. We also show that the proposed scheme do not introduce any extra latency comparing with the traditional semi-parallel decoding schedule. By doing so, the folded PSN and the path memory are merged and the path memory can be omitted.

We rewrite (1) in the form of block matrices, i.e., we divide the vectors into  $P$ -dimensional sub-vectors and the generator matrix into sub-matrices of order  $P$  and we have

$$[(\mathbf{s}_P^\lambda)_0, \dots, (\mathbf{s}_P^\lambda)_{\frac{\Lambda}{P}-1}] = [(\mathbf{u}_P)_0, \dots, (\mathbf{u}_P)_{\frac{\Lambda}{P}-1}] \cdot (\mathbf{F}^{\otimes P} \otimes \mathbf{F}^{\otimes \Lambda-P}) \quad (2)$$

where  $(\mathbf{s}_P^\lambda)_j = [s_{j \cdot P}^\lambda, \dots, s_{(j+1) \cdot P-1}^\lambda]$  and  $(\mathbf{u}_P)_j = [u_{j \cdot P}, \dots, u_{(j+1) \cdot P-1}]$  ( $j \in [0, \frac{\Lambda}{P} - 1]$ ). Each  $P$ -bit sub-vector  $(\mathbf{s}_P^\lambda)_j$  is the content stored in one address in the SRAM of the folded PSN and is a linear combination of  $(\mathbf{u}_P)_j \cdot \mathbf{F}^{\otimes P}$ . Consequently, to recover the decoded bits from the partial-sums, we first calculate all the intermediate values  $(\mathbf{u}_P)_j \cdot \mathbf{F}^{\otimes P}$  from the partial-sums, then we encode the intermediate values to get the corresponding decoded bits because  $(\mathbf{u}_P)_j \cdot \mathbf{F}^{\otimes P} \cdot \mathbf{F}^{\otimes P} = (\mathbf{u}_P)_j \cdot \mathbf{I}_P = (\mathbf{u}_P)_j$ , where  $\mathbf{I}$  is an identity matrix.

Next, we derive the equations of  $(\mathbf{u}_P)_j \cdot \mathbf{F}^{\otimes P}$ . From the mixed-product property<sup>2</sup> of Kronecker product, we can get

$$(\mathbf{F}^{\otimes P} \otimes \mathbf{F}^{\otimes \Lambda-P}) \cdot (\mathbf{I}_P \otimes \mathbf{F}^{\otimes \Lambda-P}) = \mathbf{F}^{\otimes P} \otimes \mathbf{I}_{\frac{\Lambda}{P}}. \quad (3)$$

Multiply both sides of (2) by  $(\mathbf{I}_P \otimes \mathbf{F}^{\otimes \Lambda-P})$ , we can get

$$[(\mathbf{s}_P^\lambda)_0, \dots, (\mathbf{s}_P^\lambda)_{\frac{\Lambda}{P}-1}] \cdot (\mathbf{I}_P \otimes \mathbf{F}^{\otimes \Lambda-P}) = [(\mathbf{u}_P)_0, \dots, (\mathbf{u}_P)_{\frac{\Lambda}{P}-1}] \cdot (\mathbf{F}^{\otimes P} \otimes \mathbf{I}_{\frac{\Lambda}{P}}). \quad (4)$$

Take an numerical example of (4) with  $\frac{\Lambda}{P} = 4$ , by using the multiplication of block matrices, we can get

$$\begin{cases} (\mathbf{u}_P)_0 \cdot \mathbf{F}^{\otimes P} &= (\mathbf{s}_P^\lambda)_0 + (\mathbf{s}_P^\lambda)_1 + (\mathbf{s}_P^\lambda)_2 + (\mathbf{s}_P^\lambda)_3 \\ (\mathbf{u}_P)_1 \cdot \mathbf{F}^{\otimes P} &= (\mathbf{s}_P^\lambda)_1 + (\mathbf{s}_P^\lambda)_3 \\ (\mathbf{u}_P)_2 \cdot \mathbf{F}^{\otimes P} &= (\mathbf{s}_P^\lambda)_2 + (\mathbf{s}_P^\lambda)_3 \\ (\mathbf{u}_P)_3 \cdot \mathbf{F}^{\otimes P} &= (\mathbf{s}_P^\lambda)_3 \end{cases} \quad (5)$$

<sup>2</sup> $(\mathbf{A} \otimes \mathbf{B})(\mathbf{C} \otimes \mathbf{D}) = (\mathbf{AC}) \otimes (\mathbf{BD})$ , if  $\mathbf{AC}$  and  $\mathbf{BD}$  exist.

Table I  
THE SRAM SIZE IN ALL THE MENTIONED ARCHITECTURES

	Port width	SRAM size
Folded PSN	$2P$	$\frac{N}{2}$
Folded path memory	$P$	$N$
Merged memory	$2P$	$N$

The left hand side are the  $(\mathbf{u}_P)_j \cdot \mathbf{F}^{\otimes p}$  we want to calculate, and the right hand side are the  $P$ -bit sub-vectors of the partial-sums. So (4) can be regarded as encoding  $P$  groups of  $\frac{\Lambda}{P}$ -bit sub-codes. With the  $P$  XOR gates in the folded PSN, one XOR calculation in each of the  $P$  groups of encoding is executed in one clock cycle. This indicates that for a sub-code whose length equals to  $\Lambda$ , its latency for recovery equals to the number of the “ $\oplus$ ” nodes in the encoding signal flow graph of a  $\frac{\Lambda}{P}$ -bit polar code. Consequently, the latency to recover  $\Lambda$  decoded bits from the corresponding partial-sums is  $\frac{\Lambda}{2P} \log_2 \frac{\Lambda}{P}$  clock cycles. For example, to recover the  $\Lambda = 8$  decoded bits in an LSCD with  $P = 2$  in Figure 5(b), we encode two 4-bit sub-codes,  $[s_0^3, s_2^3, s_4^3, s_6^3]$  and  $[s_1^3, s_3^3, s_5^3, s_7^3]$ , whose schedule is shown in Figure 5(c) and the total latency is 4 clock cycles. Finally, an extra  $P$ -bit encoder for each path is used to encode  $(\mathbf{u}_P)_j \cdot \mathbf{F}^{\otimes p}$ .

For an  $N$ -bit polar code,  $n-p+1$  groups of partial decoded bits with their length  $\Lambda \in \{\frac{N}{2}, \frac{N}{4}, \dots, 2P, P, P\}$  need to be recovered from the folded PSN. The size of the SRAM is  $N$  bits, which is twice that of a traditional folded PSN as the  $\frac{N}{2}$ -bit partial-sums for stage  $n-1$  are not stored in a traditional folded PSN [12]. The corresponding decoded bits can be recovered after the right most G-node at stage  $\lambda$  is calculated because these memory bits are never used to store or update partial-sums in the subsequent decoding. By using the cycles in which the folded PSN is idle, the latency can be hidden in the decoding process. Specifically, as shown in Figure 6, all the clock cycles used to calculate the nodes below stage  $p$  before the beginning of the next recovery of  $\frac{\Lambda}{2}$  bits can be used to recover the  $\Lambda$  bits because the SRAMs in the folded PSN are not activated. By calculation, the number of cycles in these stages is  $\Lambda(1 - \frac{1}{P})$  and it should be larger than the latency for the recovery of  $\Lambda$  decoded bits which is  $\frac{\Lambda}{2P} \log_2 \frac{\Lambda}{P}$  cycles. Thus, the relationship between  $\Lambda$  and  $P$  where no extra latency is introduced can be derived as

$$\Lambda < P \cdot 2^{2P-2}. \quad (6)$$

With practical parallelism  $P = 64$  which is used in most of the existing architecture [5]–[9], (6) is satisfied for the LSCD with code length even equal to  $N = 2^{20}$ .

For simplicity, we call the folded PSN which can recover the decoded bits the merged memory.

## V. IMPLEMENTATION RESULTS

To show the area saving achieved by the proposed path memory architectures, we synthesize folded PSN, traditional path memory, folded path memory and merged memory in the LSCD with different combinations of list size and code length

Table II  
THE SYNTHESIS RESULTS WITH UMC 90NM TECHNOLOGY (UNIT:  $mm^2$ )

Code length	$2^{10}$			$2^{13}$		
	List size	8	16	32	8	16
(1) Folded PSN	0.416	0.894	2.018	0.826	1.713	3.655
(2) Traditional path memory	0.521	1.692	6.158	4.251	15.83	54.72
(3) Folded path memory	0.228	0.526	1.279	0.696	1.462	3.151
(4) Merged memory	0.511	1.056	2.288	1.165	2.365	4.905
(1) + (2)	0.937	2.586	8.176	5.077	17.54	58.38
(1) + (3)	0.644	1.420	3.297	1.522	3.175	6.806
Only (4)	0.511	1.056	2.288	1.165	2.365	4.905

with UMC 90 nm technology. The timing constraint for all the designs is 1ns and  $P = 64$  for a fair comparison. All the SRAMs used in these architectures are summarized in Table I. All of them have two ports so that they can read and write data at the same time. The synthesis results are shown in Table II. The area of pointer memory is not included as the pointers for LLR memory are valid and can be reused for these memories.

Comparing with the traditional path memory, the folded path memory achieves an area saving of more than 50% for all different list size and code length combinations. It also has a smaller area than the folded PSN and the merged memory as the read port width of the SRAM is  $P$  bits instead of  $2P$  bits.

For the merged memory, all the combinations satisfy (6), indicating the decoded bits can be recovered without any latency overhead comparing with the traditional schedule. Each merged memory is slightly larger than its corresponding folded PSN because of the extra encoders and SRAM bits.

For the storage of both partial-sums and decoded bits, we can use either a folded PSN and a folded path memory (“(1)+(3)”) or just a merged memory (“Only (4)”). The sum of the area of a folded PSN and a traditional path memory (“(1)+(2)”) is used as a benchmark for comparison. The larger the list size and the code length are, the more saving we can get from the proposed architecture. The merged memory brings us the most saving as the path memory is no more needed. Regarding to the area saving with respect to the whole LSCD, the area of an LSCD with  $N = 2^{10}$  and  $\mathcal{L} = 16$  is  $7.47 mm^2$  according to [6], which means about 20% of the total area can be saved if a merged memory is used in an LSCD.

## VI. CONCLUSION

In this paper, we propose two methods to optimize the hardware complexity of the path memory in the LSCD of polar codes. The folded path memory mimics the architecture of the folded PSN to reduce the bit width of the crossbar. It is easy to implement and can be used in any semi-parallel LSCD architecture. The merged memory can recover the decoded bits from the partial-sums stored in the folded PSN in almost all the practical LSCD and hence the path memory can be omitted. Synthesis results show that a large area saving can be achieved.

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