Session 8 Overview: *Ultra-High-Speed Wireline*

WIRELINE SUBCOMMITTEE

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As data center and telecommunication infrastructure bandwidth requirements continue to increase, networking products with 112Gb/s electrical and optical transceivers are beginning to ramp up to support 400GE and beyond. At the same time, the industry is starting to explore paths of scaling high-speed links with data rates greater than 200Gb/s.

This session starts with two papers describing the design of ≥200Gb/s PAM-4 transmitters, one using a DSP/DAC approach in 10nm CMOS and another using an analog approach in 28nm CMOS. Another paper pushes the energy efficiency and chip area of a 112Gb/s DSP/DAC-based transmitter. Three papers in this session describe complete 112Gb/s PAM-4 electrical transceivers with emphasis on reconfigurability, power efficiency improvements, link robustness over voltage/temperature variations, and new techniques to support higher channel loss. One paper addresses DAC and ADC design for 400Gb/s coherent optical links. The session concludes with a paper describing a method to implement a large number of DFE taps in an ADC/DSP-based 112Gb/s PAM-4 receiver.

8:30 AM

8.1 A 224Gb/s DAC-Based PAM-4 Transmitter with 8-Tap FFE in 10nm CMOS

Jihwan Kim, Intel, Hillsboro, OR

In Paper 8.1, Intel demonstrates a 224Gb/s 4-way interleaved 7b DAC-based PAM-4 transmitter with 8-tap reconfigurable FFE in 10nm CMOS. Using a low-noise on-chip LC-PLL, inductive clock distribution network, two-stage 4:1 MUX with active peaking, and group-delay-optimized output matching network, it achieves 65fs$_{rms}$ random jitter and RLM/SNDR of 0.99/33.3dB at 1.88pJ/b energy efficiency.

8:38 AM

8.2 An Output-Bandwidth-Optimized 200Gb/s PAM-4 100Gb/s NRZ Transmitter with 5-Tap FFE in 28nm CMOS

Minsoo Choi, University of California, Berkeley, CA

In Paper 8.2, University of California, Berkeley presents a 200Gb/s PAM-4 transmitter in 28nm CMOS. The design incorporates pull-up current sources to improve output bandwidth and swing, achieving >52.9mV eye height, 0.36UI eye width, and ~99% RLM under ~6dB channel loss at 50GHz.

8:46 AM

8.3 An 8b DAC-Based SST TX Using Metal Gate Resistors with 1.4pJ/b Efficiency at 112Gb/s PAM-4 and 8-Tap FFE in 7nm CMOS

Marcel A. Kossel, IBM Research, Rüschlikon, Switzerland

In Paper 8.3, IBM describes a 112Gb/s PAM-4 SST transmitter with 8b DAC driver in 7nm CMOS with up to 16-tap digital FFE in NRZ mode. Using metal gate resistors, a DSP equalizer with gated FFE LUT logic, and reference DAC weight scaling for clock power reduction, it occupies 0.032mm^2 and consumes 1.4pJ/b.

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8:54 AM

8.4 A 116Gb/s DSP-Based Wireline Transceiver in 7nm CMOS Achieving 6pJ/b at 45dB Loss in PAM-4/Duo-PAM-4 and 52dB in PAM-2

Marc-Andre LaCroix, Huawei Technologies, Ottawa, Canada

In Paper 8.4, Huawei presents a reconfigurable PAM-4/Duo-PAM-4/NRZ ADC/DSP-based long-reach transceiver. It achieves BER ≤1E-05 at 112Gb/s in PAM-4 or Duo-PAM-4 across a 45dB loss channel, and <1E-15 at 56Gb/s PAM-2 over a 52dB loss channel without FEC, while consuming <6pJ/b.

8

9:02 AM

8.5 A Scalable Adaptive ADC/DSP-Based 1.25-to-56Gbps/112Gbps High-Speed Transceiver Architecture Using Decision-Directed MMSE CDR in 16nm and 7nm

Danfeng Xu, eTopus Technology, San Jose, CA

In Paper 8.5, eTopus demonstrates a fully integrated, adaptive 1.25-to-56/112Gb/s PAM-4 ADC/DSP-based transceiver in 16nm and 7nm CMOS. Using Decision-Directed MMSE CDR, it achieves CDR lock at 2E-2 BER at 56.25Gb/s PAM-4 over 51.9dB channel loss. With architecture fast temperature tracking capability, the link BER test performance of 53.125Gb/s PAM-4 at 35dB channel loss meets IEEE specifications with sufficient margin when temperature varies from -15°C to 125°C with 10°C/minute.

9:10 AM

8.6 A Highly Reconfigurable 40-97GS/s DAC and ADC with 40GHz AFE Bandwidth and Sub-35fJ/conv-step for 400Gb/s Coherent Optical Applications in 7nm FinFET

R. L. Nguyen, Inphi, Irvine, CA

In Paper 8.6, Inphi presents reconfigurable 40-to-97GS/s 8b DACs and ADCs which are fully integrated in a 7nm FinFET DSP chip targeting 400Gb/s coherent optical links. It achieves 40GHz AFE bandwidth and a Walden FOM <35fJ/conv-step.

9:18 AM

8.7 A 112Gb/s ADC-DSP-Based PAM-4 Transceiver for Long-Reach Applications with >40dB Channel Loss in 7nm FinFET

P. Mishra, Inphi, San Jose, CA

In Paper 8.7, Inphi presents a 112Gb/s ADC/DSP-based PAM-4 transceiver in 7nm FinFET. Incorporating a 64-way time-interleaved SAR ADC, it consumes 6.51pJ/b including analog and digital power while operating over a channel with >40dB insertion loss.

9:26 AM

8.8 A 112Gb/s PAM-4 Low-Power 9-Tap Sliding-Block DFE in a 7nm FinFET Wireline Receiver

James Bailey, Huawei Technologies, Toronto, Canada

In Paper 8.8, Huawei presents a 112Gb/s PAM-4 ADC/DSP-based receiver in 7nm FinFET with 9 DFE taps in the DSP. The DSP uses a method for pipelining DFE operations which allows the implementation of a large number of DFE taps, improving link performance beyond the traditional many-tap FFE + 2-tap DFE while simultaneously reducing power and area.