Highlights of the ISSCC 2013 Processors and High Performance Digital Sessions

I. Introduction

THE IEEE International Solid-State Circuits Conference (ISSCC) is the foremost global forum for presenting advances in solid-state circuits and systems-on-a-chip. Every year since its first issue, the IEEE JOURNAL OF SOLID-STATE CIRCUITS has highlighted some well-received papers from the most recent ISSCC in special issues. This special issue covers the ISSCC conference held in San Francisco, CA, USA, on February 17–21, 2013. Session chairs and co-chairs initially recommended papers for publication, with final decision for inclusion based on peer review.

This January issue includes the topics from the low power and high performance digital, memory, and technology directions as well as imagers, medical and sensors.

II. Processors and Digital PLLs

Five papers were selected from this year's ISSCC sessions on Processors and Digital PLLs. The first four papers describe state-of-the-art processor technology, circuits, and methodologies implemented at the 28 nm and 32 nm process nodes. A fifth paper from the Digital PLLs session presents an innovative injection-locked all-digital PLL from the Tokyo Institute of Technology.

The first paper, by Warnock *et al.*, describes technology, circuit, and physical design innovations in the IBM zEnterprise EC12 system. A 5.5 GHz processor chip with 2.75 B transistors contains 6 CPU cores, each with 2 MB dedicated L2 cache, shared 48 MB eDRAM L3 cache, and DDR3 and I/O controllers. A 192 MB eDRAM level-4 cache chip doubles L4 cache size over a prior 45 nm design in about the same chip area and latency. Six of the processor chips and two L4 cache chips are mounted on a high-performance multi-chip module using a glass-ceramic substrate with 102 layers.

The second paper, by Hart *et al.*, presents a 3.6 GHz SPARC 16-processor SoC from Oracle with 1.5 B transistors in TSMC's 28 nm CMOS process. The SoC contains an 8 MB 3rd-level cache shared among the 16 cores through an on-chip high-bandwidth cross-bar. The 8-threaded cores feature advanced power management including a frequency-locked loop (FLL) which modulates clock frequency during di/dt events, allowing for robust operation and reducing average chip power by about 5%.

The third paper, by Kan *et al.*, describes a 3.0 GHz SPARC 16-processor SoC from Fujitsu in a 28 nm HKMG CMOS process with 13 levels of interconnect. The design contains 16 superscalar OOO-issue 2-way SMT cores, 24 MB shared L2 cache, 14.5 Gb/s coherency SerDes, eight DDR3 ports, and implements significant circuit design improvements for performance, area reduction, and high reliability. The die contains 3 B transistors and occupies 588 mm^2.

The fourth paper, by Yang *et al.*, presents a 1.5 GHz 8-processor MIPs SoC from the Chinese Academy of Sciences in 32 nm and 28 nm low-power bulk CMOS processes. The 1.14 B transistor design includes eight 4-issue out-of-order CPUs, shared 8 MB L3 cache, two-levels of on-chip interconnect, DDR controller, four core supplies, and on-board power management. The paper describes design challenges and methodology used in scaling the design from a 65 nm bulk technology to 32 nm and 28 nm processes.

The fifth paper, by Musa *et al.*, describes an all-digital dual-VCO injection locked PLL in 65 nm CMOS from the Tokyo Institute of Technology. The dual-loop configuration contains two VCOs: a replica VCO in a TDC-less all-digital FLL, and a main injection-locked VCO placed outside the loop to overcome timing problems associated with conventional injection-locked PLLs. The proposed PLL has a tuning range of 0.5–1.6 GHz, occupies 0.022 mm^2, and has low-jitter and low-power characteristics.

III. Energy Efficient Digital

Four highly innovative papers were selected from the Energy Efficient Digital sessions at ISSCC 2013. These papers detail some of the leading-edge advancements in energy-efficient digital circuit techniques. The first paper describes a video decoder design of the new HEVC standard. The second paper presents a novel analog processing technique in time domain. The third and fourth papers describe state-of-the-art results in the Razor technique and non-volatile logic SoC.

The first paper, by Tikekar *et al.*, describes a high-throughput HEVC video decoder chip developed for 4 K UHD applications. By using a variable-sized split system pipeline and a DRAM-latency-aware cache, the architecture reduces the memory bandwidth requirements for the HEVC decoding and achieves 67% bandwidth savings.

The second paper, by Miyashita *et al.*, highlights a novel time-domain analog computing scheme for area and energy efficiency. The digital-to-time converter (DTC) and time-to-digital converter (TDC) are proposed to exploit the time-domain processing in mixed-signal computing. An LDPC decoder chip is designed based on this scheme and achieves the best reported efficiencies.

The third paper, by Whatmough *et al.*, demonstrates a high-throughput Razor FIR accelerator. It achieves a peak throughput of 1 GS/s and 37% improvement of energy efficiency by using a Razor latch for error detection and deferred correction of timing violations by means of the time borrowing between successive pipeline stages.

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The last paper, by Khanna *et al.*, describes an FRAM based MCU for ULP applications. By distributing non-volatile storage elements within the core logic in a fine-grained manner, the MCU demonstrates zero standby leakage and less than 400 ns wake-up latency.

IV. Memory

From this year's Memory sessions, five papers spanning SRAM, DRAM, and nonvolatile memory were selected to capture significant innovations in the field, including new concepts for power reduction as well as demonstration and commercialization of new technologies.

The first paper, by Sinangil *et al.*, leverages application-specific techniques to reduce bit-line switching activity in an SRAM to reduce power dissipation. By targeting applications such as video and imaging, which have highly correlated data patterns, predictive techniques can be introduced in both the bit-cell and sensing network. This concept is demonstrated to achieve up to a 1.9× reduction in energy/access for a prototype 65 nm SRAM.

The second paper, by Tachibana *et al.*, describes new circuit techniques to reduce both active and standby power in SRAMs. The paper focuses on adjustment of the cell supply voltage to reduce power by utilizing a bit-line power calculation scheme to minimize active power and a digitally controllable scheme to minimize standby power in the retention state. Hardware results from a 28 nm SRAM with a 0.12 μm^2 bit-cell demonstrate 27% active and 85% standby mode power reduction.

The third paper, by Bucher *et al.*, presents a 6.4 Gb/s transceiver for dual-rank memory interface systems that uses single-ended low-swing near-ground signaling to minimize power. The paper describes architecture and circuit techniques to achieve fast power-mode transitions and tight timing control. Measurement results demonstrate a link that achieves 9.1 pJ/bit power efficiency.

The fourth paper, by Liu *et al.*, demonstrates a 32 Gb ReRAM test chip developed in a 24 nm process utilizing a cross-point architecture with a diode selection device and multiple memory layers stacked above supporting circuitry. Specific circuit techniques are presented to improve die efficiency, performance, and power consumption.

The final paper, by Kono *et al.*, details 40 nm embedded flash macros developed for automotive applications using a split-gate MONOS cell with charge-trapping storage. Fast and robust read, programming, and erase operations are achieved through several new control schemes while area efficiency is improved by the use of stacked capacitors. A 2 MB code macro achieves 160 MHz random read operation while a 64 kB data macro achieves 10 million cycle endurance at 170°C.

V. Technology Directions

This section includes six papers from the Technology Directions session of ISSCC 2013. The first three papers present emerging medical and sensor technologies, while the next three papers describe emerging memory and wireless technologies.

In the first paper, Song *et al.*, demonstrates a 110 nm, 5.5 mm^2, 2.2 mW, 87 mA · min isotophoresis smart controller IC with dual-mode impedance sensors for a patch-type transdermal drug delivery system. It can measure skin temperature and contact/tissue impedance to adapt the stimulation allowing real-time monitoring of the delivered drug dosage. An iontophoresis stimulator front-end provides programmable stimulation current in the range of 16–512 μA amplitude, DC-500 Hz frequency, and 3–100% duty cycle for controllable drug delivery. The dual-mode impedance sensor measures load and tissue impedances in the range of 5 kΩ–50 kΩ and 5 Ω–1 kΩ, respectively. The proposed iontophoresis system is successfully verified by both in-vitro and in-vivo tests.

The second paper, by Maruyama *et al.*, presents a 30 mm^2, 1024×8 time-gated SPAD line sensor for time-resolved laser induced Raman spectroscopy. Two different chip geometries are implemented and characterized. A type I sensor has a maximum photon detection efficiency of 0.3% and median dark count rate of 80 Hz at 3 V of excess bias. A type II sensor offers a maximum photon detection efficiency of 19.3% and a median dark count rate of 5.7 kHz at 3 V of excess bias. Both chips have 250 ps temporal resolution, and fast gating capability, with a minimum gate width of 1.8 ns for type I and 0.7 ns for type II. Raman spectra are successfully observed from natural minerals, such as calcite and willemite. With the use of sub-nanosecond gating, background fluorescence is significantly reduced.

The third paper, by Shulaker *et al.*, unveils a fully digital capacitive sensor interface built entirely using carbon nanotube FETs and implemented in a VLSI compatible fashion. It is the first demonstration of a complete system implemented with such a technology. This is made possible by a digitally-oriented interface architecture, as well as the imperfection-immune design paradigm, which combines design and processing techniques to successfully overcome CNT imperfections and variations. In addition to electrical measurements, they demonstrate correct operation of their CNFET circuitry by interfacing it with a sensor used to control a handshaking robot. The sensor interface based on a sensor-controlled oscillator consumes 336 μW from a 3 V supply while achieving a 1.83% nonlinearity.

Qazi *et al.* present a nonvolatile D-flip-flop (NVDFF) with ferroelectric capacitor based non-volatile storage, enabling logic pipelines to be suspended and power-cycled without losing the state. The paper demonstrates a save-restore energy budget of just 3.4 pJ/b. Correct operation is verified over power cycle intervals from 4.8 μs to 1 day. Statistical measurements across 21,000 NVDFFs validate the capability of the circuit to achieve the requisite 10 ppm failure rate for embedded system applications.

The next paper, by Ruffieux *et al.*, introduces and demonstrates with high yield a novel concept for the packaging under vacuum of tuning fork quartz XTALs on top of a silicon interposer equipped with TSVs. A novel timing micro-system achieves sub-microwatt power consumption in real-time clock mode. The module achieves 0.4 μW power dissipation and ±2 ppm stability over −40 to 85 °C in RTC mode and can deliver on-demand programmable clocks between 1–50 MHz. The latter are obtained either with a RC PLL or after division of the signal obtained from a 2 GHz BAW DCO at a power dissipation of 100 μW and 5.3 mW, respectively.

The final paper, by Kosuge *et al.*, resents a 0.15-mm-thick non-contact connector for Mobile Industry Processor Interface (MIPI) applications. A vertical directional coupler enables

simultaneous two-link communication with one coupler without performance degradation. A fully balanced pulse transmitter fabricated in 90 nm CMOS technology consumes 1.5 pJ/b and significantly suppresses EMI, allowing simultaneous two-channel communications. An experimental LCD interface system reaches the maximum data rate of 2.3-Gb/s/link at a bit error rate of less than 10–12. The timing margin of single link is 320 ps (= 64% U.I.) and of two links is 305 ps (= 61% U.I.) at 2.0 Gb/s.

VI. Sensors, Imagers, and Medical

Seven papers have been selected from this year's sessions on Sensors, Imagers and Medical Circuits and Systems. These papers describe significant advances in the field, including a neural-prosthetic system-on-chip (SoC) for epileptic seizure control, an implantable CMOS neural probe with 455 active electrodes, a fully-differential EMI-insensitive accelerometer, a low-power heart-rate sensor, and three special-purpose imagers: a CMOS image sensor with an embedded feature-extraction algorithm, a fully-digital silicon photomultiplier array for PET applications, and a SoC for a time-of-flight depth sensor.

In the first paper, Chen *et al.* describe a neural-prosthetic SoC for the suppression of epileptic seizures. The SoC, implemented in 0.18 μm CMOS, features eight low-power input channels, a delta-modulated SAR ADC and a configurable bio-signal processor to acquire neural signals and extract epileptic features. It also includes a high-voltage-tolerant stimulator circuit for closed-loop seizure suppression, as well as a wireless transceiver for power and data transmission, and consumes 2.8 mW. The paper reports results of in-vivo experiments in rats showing a seizure detection accuracy better than 92%.

The second paper, by Mora Lopez *et al.*, reports the first CMOS neural probe equipped with active electrodes. The probe, implemented in a standard 0.18 μm CMOS technology with post-processing, contains 455 active electrodes in a 10-mm-long 100-μm-wide probe shank and 52 readout channels in the probe body. In-situ amplification is used to reduce crosstalk. In-vivo experiments in rats are reported that demonstrate the capability of this probe to simultaneously record neural activity of many individual cells.

In the third paper of this section, Petkov *et al.* describe an accelerometer for electronic stability control in automotive applications. The sensor combines a fully-differential signal path with a pseudo-random chopping scheme to improve immunity to electromagnetic interference (EMI). The dual-axis design occupies 1.1 mm^2 in 0.18 μm CMOS, and achieves 380 $\mu g/\sqrt{\text{Hz}}$ noise floor and 84 dB dynamic range while consuming 1.6 mW. The paper includes experimental results demonstrating the effectiveness of the applied techniques in improving stability and reducing susceptibility to EMI.

The fourth paper, by Alhawary *et al.*, reports on a 0.5 V light-to-digital converter capable of detecting the heart rate signal from a finger pressed against an off-chip photodiode using only ambient light. The converter, implemented in 0.18 μm CMOS, consumes less than 4 μW. It uses a feedback topology in which a wide-range logarithmic resistance-to-digital converter is used to keep the voltage across the photodiode constant, allowing it to handle a photocurrent range of three orders of magnitude. The feedback loop is built around a Laddered Inverter Quantizer/Amplifier/Filter (LIQAF), a new circuit block that is analyzed in detail in the paper.

The final three papers relate to imaging. The paper by Choi *et al.* describes a CMOS image sensor with an embedded feature-extraction algorithm for motion-triggered object-of-interest imaging. The sensor wakes up when motion is detected and extracts features from the captured image for the detection of objects-of-interest. Full images are captured only when such objects are found, which significantly reduces power consumption. The 0.18 μm CMOS chip operates at 0.22 μW/frame in motion-sensing mode and at 3.4 μW/frame in feature-extraction mode.

The second imaging paper, by Braga *et al.*, reports on a fully-digital silicon photomultiplier (SiPM) array for time-of-flight PET applications, implemented in a 0.13 μm CMOS imaging technology. It employs a total of 92 k single-photon avalanche diodes (SPADs) arranged in 8×16 pixels. The pixels are capable of determining the energy and arrival time of incoming gamma photons, and contain four mini-SiPMs and two 12-bit 64 ps time-to-digital converters each. A distributed adder provides 100 MHz histogramming of total counts for discriminating asynchronous events. An overall system timing resolution of 266 ps is achieved.

In the final paper, Niclass *et al.* present a 0.18 μm CMOS SoC that performs time-correlated single-photon counting and complete digital signal processing for a time-of-flight depth sensor. Under the challenging conditions of strong solar illuminance and a low-reflectivity target, the prototype sensor achieves an impressive repeatability of 14 cm throughout a distance range of 100 m.

Timothy Fischer
Oracle Corporation
Broomfield, CO 80021 USA
tcf@mesanetworks.net

Byeong-Gyu Nam
Chungnam National University
Daejeon, 305-764 Korea
bgnam@cnu.ac.kr

Leland Chang
IBM T. J. Watson Research Center
Yorktown Heights, NY 10598 USA
lelandc@us.ibm.com

Tadahiro Kuroda
Keio University
Yokohama, 108-8345 Japan
kuroda@elec.keio.ac.jp

Michiel A. P. Pertijs
Delft University of Technology
Delft, 2628 CD The Netherlands
M.A.P.Pertijs@tudelft.nl

Timothy Fischer received the M.S. degree in computer engineering from the University of Cincinnati, Cincinnati, OH, USA, in 1989.

He has worked in high-speed digital circuit design for 24 years. He worked for Digital Equipment, Hudson, MA, USA, until 1998, designing VAX and Alpha CPUs. From 1998 to 2006, he worked on Itanium CPU design, circuit methodology, and clocking with Hewlett-Packard and Intel in Fort Collins, CO, USA. From 2006 to 2013, he was with Advanced Micro Devices in Fort Collins, CO, USA, leading circuit design and circuit methodology teams for several high-performance microprocessors. In May 2013, he joined Oracle Corporation in Broomfield, CO, USA, where he is currently involved with circuit design and methodologies for next-generation server processors.

Mr. Fischer was a member of the ISSCC technical program committee from 2010 to 2013, served as tutorial speaker on power-delay tradeoffs in 2011, and served as JSSC guest editor during 2012–2013. He has published more than 15 technical papers and holds 12 patents.

Byeong-Gyu Nam (M'10–SM'13) received the B.S. degree from Kyungpook National University, Daegu, Korea, in 1999, and the M.S. and Ph.D. degrees from KAIST, Daejeon, Korea, in 2001 and 2007, respectively. His Ph.D. work focused on low-power GPU design for wireless mobile devices.

In 2001, he joined Electronics and Telecommunications Research Institute (ETRI), Daejeon, Korea, where he was involved in a network processor design for InfiniBandTM protocol. From 2007 to 2010, he worked for Samsung Electronics, Giheung, Korea, where he worked on world first low-power 1-GHz ARM CortexTM microprocessor design.

Dr. Nam is currently with Chungnam National University, Daejeon, Korea, as an assistant professor. He is serving as a vice director of the System Design Innovation and Application Research Center (SDIA), KAIST and a member of steering committee of the IC Design Education Center (IDEC), KAIST. His current interests include mobile GPU, embedded microprocessor, low-power SoC design, and embedded software platforms. He co-authored the book *Mobile 3D Graphics SoC: From Algorithm to Chip* (Wiley, 2010) and presented tutorials on mobile processor design at IEEE ISSCC 2012 and IEEE A-SSCC 2011. He is a member of the TPC for IEEE ISSCC, IEEE A-SSCC, IEEE COOL Chips, VLSI-DAT and ISOCC.

Leland Chang (S'99–M'03–SM'12) received the B.S., M.S., and Ph.D. degrees in electrical engineering and computer sciences in 1999, 2001, and 2003, respectively, from the University of California, Berkeley, CA, USA.

He joined the IBM Thomas J. Watson Research Center, Yorktown Heights, New York, NY, USA, in 2003 and is now manager of Design and Technology Solutions. His work focuses on power efficiency in high-performance systems, spanning the development of new technology elements and the design of high-performance memory and power management circuits. Key contributions have included early demonstration of the FinFET structure for CMOS scaling, 8T-SRAM for embedded memory scaling, double-pumped register files for high-speed access, and voltage converter circuits based on dense, high-Q trench capacitor devices. He is the author of more than 70 technical articles and 60 patents and is currently a member of the ISSCC technical program committee.

Tadahiro Kuroda (M'88–SM'00–F'06) received the Ph.D. degree in electrical engineering from the University of Tokyo, Tokyo, Japan, in 1999.

In 1982, he joined Toshiba Corporation, where he designed CMOS SRAMs and ASICs. From 1988 to 1990, he was a Visiting Scholar with the University of California, Berkeley, where he conducted research in the field of VLSI CAD. In 1990, he was back to Toshiba, and engaged in the research and development of BiCMOS/ECL ASICs, high-speed CMOS LSIs for telecommunications and low-power CMOS LSIs for mobile applications. He invented a Variable Threshold-voltage CMOS (VTCMOS) technology to control VTH through substrate bias, and applied it to a DCT core processor in 1995. He also developed a Variable Supply-voltage scheme to control VDD by an embedded DC-DC converter, and employed it to a microprocessor core and an MPEG-4 chip in 1997. In 2000, he moved to Keio University, Yokohama, Japan, where he has been a Professor since 2002. He was a Visiting MacKay Professor at the University of California, Berkeley, in 2007. His research interests include low-power, high-speed CMOS design, proximity communications using inductive/EM-coupling and image recognition. He has published more than 200 technical publications, including 34 ISSCC papers, 21 VLSI Symposia papers, 19 CICC papers, and 16 A-SSCC papers. He has written 22 books/chapters and filed more than 100 patents.

Dr. Kuroda served as the General Chairman for the Symposium on VLSI Circuits and A-SSCC, the Vice Chairman for ASP-DAC, sub-committee chairs for A-SSCC, ICCAD, SSDM and VLSI-DAT, and TPC members for ISSCC, the Symposium on VLSI Circuits, CICC, DAC, ASP-DAC, ISLPED, SSDM, ISQED, and other international conferences. He was a recipient of the 2005 P&I Patent of the Year Award, the 2007 ASP-DAC Best Design Award, the 2009 IEICE Achievement Award, and the 2011 IEICE Society Award. He was an elected AdCom member and a Distinguished Lecturer for the IEEE Solid-State Circuits Society. He is an IEEE Fellow and an IEICE Fellow.

Michiel A. P. Pertijs (S'99–M'06–SM'10) received the M.Sc. and Ph.D. degrees in electrical engineering (both *cum laude*) from the Delft University of Technology, Delft, The Netherlands, in 2000 and 2005, respectively.

From 2000 to 2005, he was a researcher with the Electronic Instrumentation Laboratory of Delft University of Technology, working on high-accuracy CMOS smart temperature sensors. From 2005 to 2008, he was with National Semiconductor, Delft, where he designed precision operational amplifiers and instrumentation amplifiers. From 2008 to 2009, he was a Senior Researcher with the IMEC/Holst Centre, Eindhoven, The Netherlands. In 2009, he joined the Electronic Instrumentation Laboratory of Delft University of Technology, where he is now an Associate Professor. He heads a research group working on integrated circuits for medical ultrasound and energy-efficient smart sensors. He has authored or co-authored one book, three book chapters, 10 patents, and over 50 technical papers. His research interests include analog and mixed-signal electronics and smart sensors.

Dr. Pertijs is a member of the technical program committees of the International Solid-State Circuits Conference (ISSCC), the European Solid-State Circuits Conference (ESSCIRC), the IEEE Sensors Conference, and the IEEE PRIME Conference. He received the ISSCC 2005 Jack Kilby Award for Outstanding Student Paper, the IEEE JOURNAL OF SOLID-STATE CIRCUITS 2005 Best Paper Award, and the 2006 Simon Stevin Gezel Award from the Dutch Technology Foundation STW.