## Comments and Corrections

## Correction to "A 70 dB DR 10 b 0-to-80 MS/s Current-Integrating SAR ADC With Adaptive Dynamic Range"

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In the above paper [1], the authors regret that the paper [3] was not mentioned in the reference list, since it has introduced the parametric amplification using a MOS transistor; this technique is called the passive amplification in Section III-B of [1]. While being listed in the original ISSCC publication [2], this reference was unintentionally left out in the extended JSSC manuscript.

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## REFERENCES

- [1] B. Malki, T. Yamamoto, B. Verbruggen, P. Wambacq, and J. Craninckx, "A 70 dB DR 10 b 0-to-80 MS/s current-integrating SAR ADC with adaptive dynamic range," *IEEE J. Solid-State Circuits*, vol. 49, no. 5, pp. 1173–1183, May 2014.
- [2] B. Malki, T. Yamamoto, B. Verbruggen, P. Wambacq, and J. Craninckx, "A 70 dB DR 10 b 0-to-80 MS/s current-integrating SAR ADC with adaptive dynamic range," in 2012 IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 19–23, 2012, pp. 470–472.
- [3] S. Ranganathan and Y. Tsividis, "Discrete-time parametric amplification based on a three-terminal MOS varactor: Analysis and experimental results," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2087–2093, Dec. 2003