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Laser Fault Injection Attacks against Radiation Tolerant TMR Registers

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Security requirements for the Internet of things (IoT), wireless sensor nodes, and other wireless devices connected in a network for data exchange are high. Confidentiality, data integrity, availability of the services, and authentication of communicated devices are the main security goals usually implemented with cryptographic approaches. Their secrecy is based on the used keys. Theoretically, the cryptographic approaches are secure. This changes dramatically if an attacker has physical access to the attacked device. The execution time of cryptographic operations, current drawn from the power supply, electromagnetic radiation and many other physical effects, called side-channel effects, can be measured and later analysed using statistical or machine learning methods. Many attacks concentrate on the analysis of registers' activity. Some attacks exploit the key-dependent hamming weight of the data, stored in registers, and require usually many traces for the analysi[s \[1\].](#page-2-0) Other attacks exploit the distinguishability of the registers addressing and can be successful when analysing many traces [\[2\]](#page-2-1) as well as a single trace only [\[3\],](#page-2-2) [\[4\].](#page-2-3) The sensitivity of cryptographic chips to the environmental and operating parameters – temperature, voltage, frequency, light, EM pulses, radiation, etc. – can be successfully exploited to reveal the cryptographic key too. A fluctuation of the environment and working parameters can cause fault(s). Cryptographic keys can be revealed by analysing such faults, whereby the mostly attacked blocks of cryptographic designs are the registers. Optical FI attacks using lasers belong to the class of semi-invasive attacks. This type requires to perform a chip decapsulation and exploits the sensitivity of semiconductors to the visible light. The pioneering work regarding optical FI attacks was published already in 2002 [\[5\].](#page-2-4)

During our previous works we successfully attacked different standard logic gates manufactured in IHP's technologies [\[6\],](#page-2-5) [\[7\].](#page-2-6) Additionally, we investigated the resistance of Resistive Random Access Memory (RRAM) cells [\[13\]](#page-2-7) and radiation hard Junction Isolated Common Gate (JICG) FF [\[8\].](#page-2-8) A short overview of the optical FI attacks and used equipment is given in [\[9\].](#page-2-9) A common approach to increase resistance against FI attacks is to implement countermeasures based on redundancy techniques. In this work, we investigate the robustness of the Triple Modular Redundancy (TMR) shift registers against optical FI attacks on example of the TMR shift registers based on standard TMR architecture, designed and manufactured in the IHP's CMOS 130 nm technology [\[14\].](#page-2-10) TMR flip-flops attacked have been originally designed for space application, have been evaluated in single event effect measurements, and have been verified as very radiation tolerant. Each attacked TMR circuit is a 1024 bit long register, i.e. it contains 1024∙3= 3072 standard library flip-flops and 1024 voters. The block diagram of the attacked TMR-FF is shown in **[Fig. 1](#page-1-0)**.

Fig. 1. Block diagram of attacked TMR-FF.

The IHP TMR-FF has two delay elements denoted in **[Fig.](#page-1-0) [1](#page-1-0)** as δ and 2δ. These delay elements have to filter possible transient faults caused by a particle at the inputs of the FFs. Detailed discussion of the chosen delay value can be found in [\[14\].](#page-2-10) According to the block diagram of TMR-FF, a FI attack can be successful if a fault will be injected into any two FFs of the same TMR-FF simultaneously, or if a fault will be injected into logic gates of the voter (and it is longer then the timing filter limits). Due to the technology requirements the chips have metal fillers atop.

To attack the IHP radiation hard TMR shift registers we used a setup that consists of: a modified Riscure Diode Laser Station (DLS) [\[11\],](#page-2-11) a VC glitcher, a PC with the Riscure Inspector software, a stable power supply, a generator and an oscilloscope. The setup for optical FI attacks is shown in **[Fig.](#page-1-1) [2](#page-1-1)** schematically.

The modified FI setup can be used with two multi-mode lasers: red (808 nm) and near-infrared (1064 nm) laser [\[11\]](#page-2-11) and with a single-mode red (808 nm) laser from Alphanov [\[12\].](#page-2-12) Detailed description of the setup, including the applied laser parameters, can be found i[n \[6\]](#page-2-5)[–\[8\].](#page-2-8) Due to the fact that the attacked chip was manufactured by the IHP, we did not perform a decapsulation and we decided to attack the register from the front-side of the chips.

A triplicated flip-flop and its voter in attacked registers are placed in one row. Details about placement of gates and distances between them can be found i[n \[10\]](#page-2-13) and [\[14\].](#page-2-10) Due to the specific placement of the gates, we have three possible attack scenarios:

Scenario1: Attack illuminating logic gates of the voter: successful injection of a fault into any logic gate of the voter can lead to a faulty logic state at voters' output that is the output of the TMR-FF. This scenario is technically possible using both red lasers available in the setup.

Scenario2: Attack illuminating FF1 and FF2 simultaneously: this scenario is possible using the multimode laser with $20 \times$ or $5 \times$ magnification objectives only.

Scenario3: Attack illuminating the whole TMR-FF, i.e. illuminating 3 FFs and the voters simultaneously: the scenario is technically possible using the multi-mode laser with $5\times$ magnification objective only. We did not verify this scenario due to the possible simultaneous influence on FFs and voter that leads to a fault-free state.

To observe a successful fault injection we sent a constant input to the attacked shift register during an experiment, i.e. the input of the shift register was set to '1' or to '0'. We obtained the following results:

- In *Scenario1* all our FI attacks illuminating the voter of different FFs were not successful despite successful injection of faults into standard library FFs [\[7\].](#page-2-6) This result can be explained due to the difference regarding laser parameters between experiments described in [\[7\]](#page-2-6) and here: in previous work we used a standard DLS from Riscure, after then the DLS was modified by Opto GmbH to allow using the Alphanov single-mode laser. We assume that the modification reduced the laser beam power.
- In *Scenario2* we were able to inject faults using the multi-mode laser with a $20\times$ and $5\times$ magnification objectives. We observed transient repeatable faults in flip-flops in logical state '0' and logical state '1', i.e. bit-set (' $0 \rightarrow$ '1') and bit-reset (' $1 \rightarrow$ '0') faults. We assume that we influenced on both FFs simultaneously. Please note that not all TMR-FFs attacked where successfully influenced. This can be due to the metal fillers placed over the sensitive areas of TMR-FFs. In our experiments, we did not observe any permanent (change of logic state is no more possible) or stuck-at (change of logic state cannot be changed before the device shutdown) faults, even when applying maximum laser beam power and pulse duration. After the successful injection of faults, the TMR shift register is fully functional, i.e. the internal structure of the chip is intact and its surface was not damaged. T[ABLE](#page-2-14) I gives a quantitative overview of our attacks for *Scenario2*.

Generally, redundancy is a means to increase the resistance of a design to faults and may be a promising approach against registers manipulations by cryptographic devices. But in our experiments, we were able to inject different transient faults into TMR registers using a single laser beam. Performing attacks against FFs we were able to inject transient repeatable *bit-set* as well as *bit-reset* faults into the IHP TMR shift registers using the multi-mode laser.

a. POWER MEASUREMENT UNIT IN RISCURE SOFTWARE. b.
THE FAULT IS NOT FULLY REPEATABLE.

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